Statistical Description of Process Variability

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Abstract

- IC variability has a hierarchical/hybrid character
  - Its hierarchy reflects the nature of production (device, chip, field, wafer, and wafer-lot levels)
  - It is *hybrid*, because at each levels variability consists of spatial, deterministic and random components.
  - Variability originates from interacting layout components, modeling and manufacturing imperfections, and randomness at the atomistic scale.

- Capturing variability requires a coordinated test pattern design, data collection and TCAD simulations.
  - A complete, yet *parsimonious* statistical model, which can provide suitable design guidance in order to ensure optimal balance between yield and performance.

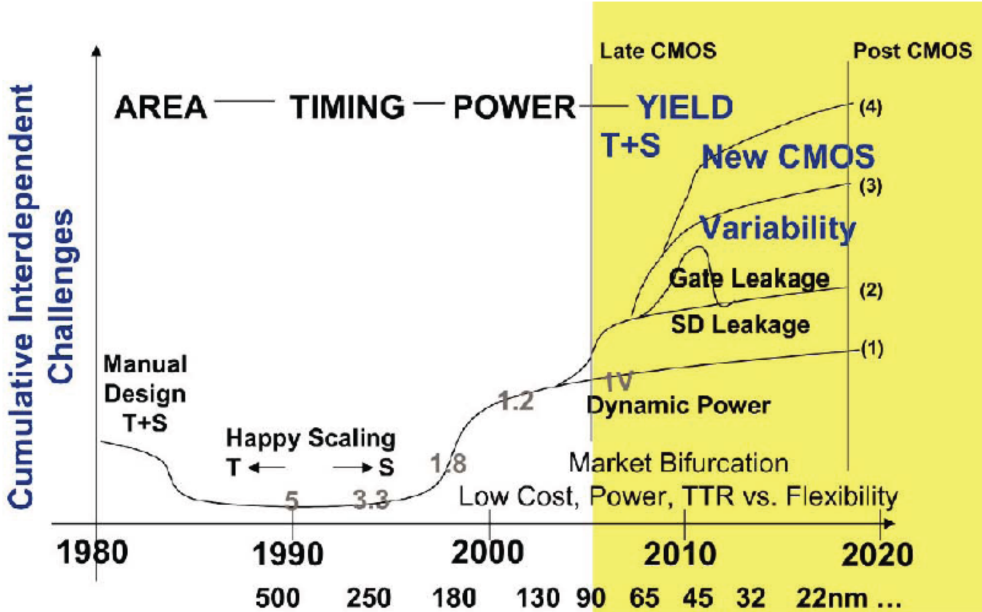
- This presentation will focus on the structure, characterization and use of such a comprehensive IC variability model.

Outline

- Background
- Approaches
  - Global Empirical Model (Hierarchical / Spatial)
  - Wafer-to-wafer systematic variability
  - LER modeling and impact assessment
  - Entering the design flow
- Future

Variability Through Time

Variability has become a major challenge to scaling and design

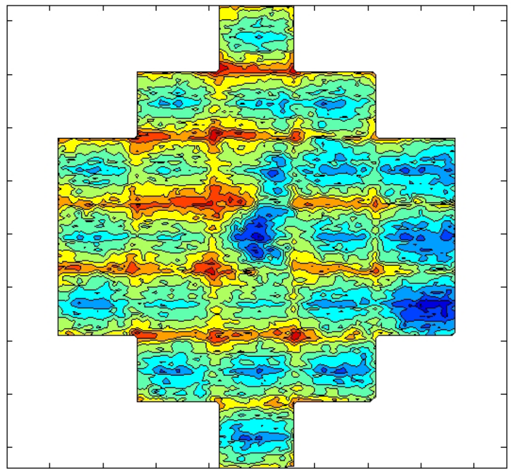


G. Declerck, Keynote talk, VLSI Technol. Symp. 2005

IEEE/ACM Workshop on Variability Modeling and Characterization
ICCAD 2009
Scott Roy (Univ. of Glasgow): *Atomistic Simulation of Variability*

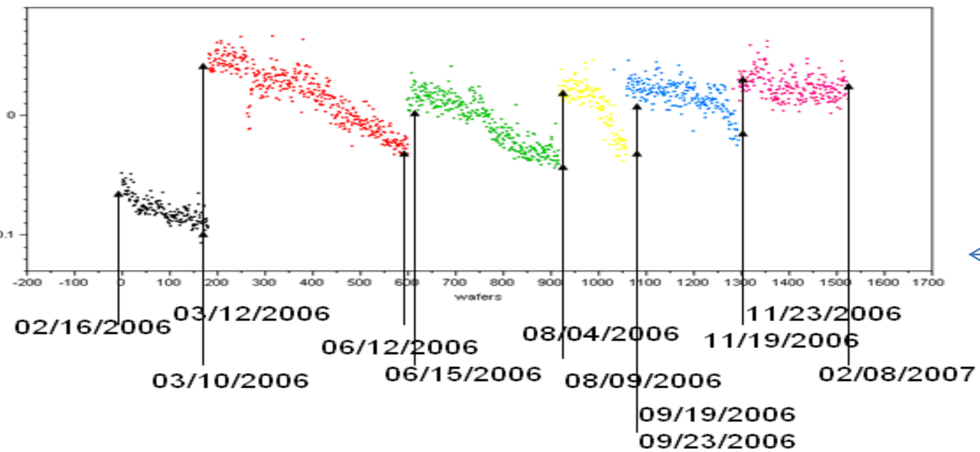
Manufacturing & Systematic Variability

- Across Wafer non-uniformities
- Wafer-to-wafer, lot-to-lot variability
- Across-field systematic
  - Mask induced
  - Focus, exposure induced
  - Layout (stress, optical, etch, RTA, CMP…)



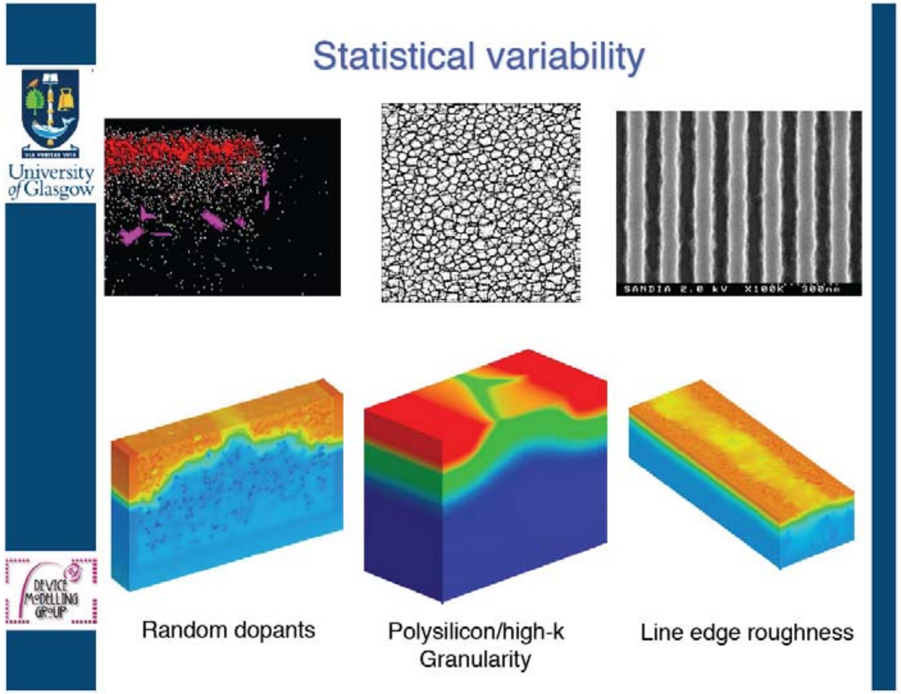
Modeling Spatial Gate Length Variation in the 0.2 μ m to 1.15mm Separation Range , Paul Friedberg, Spanos et al, SPIE 2008

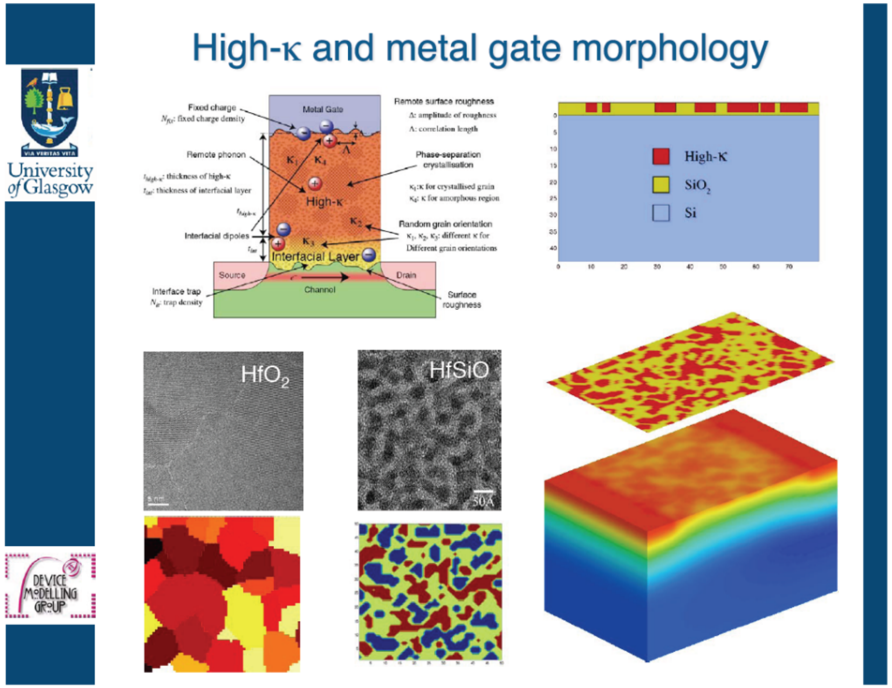
Long Term Process Drift in Plasma Etch operations



Virtual Metrology Modeling for Plasma Etch Operations, Dekong Zeng , Spanos et al, ISSM 2008

Native (Random) Variability





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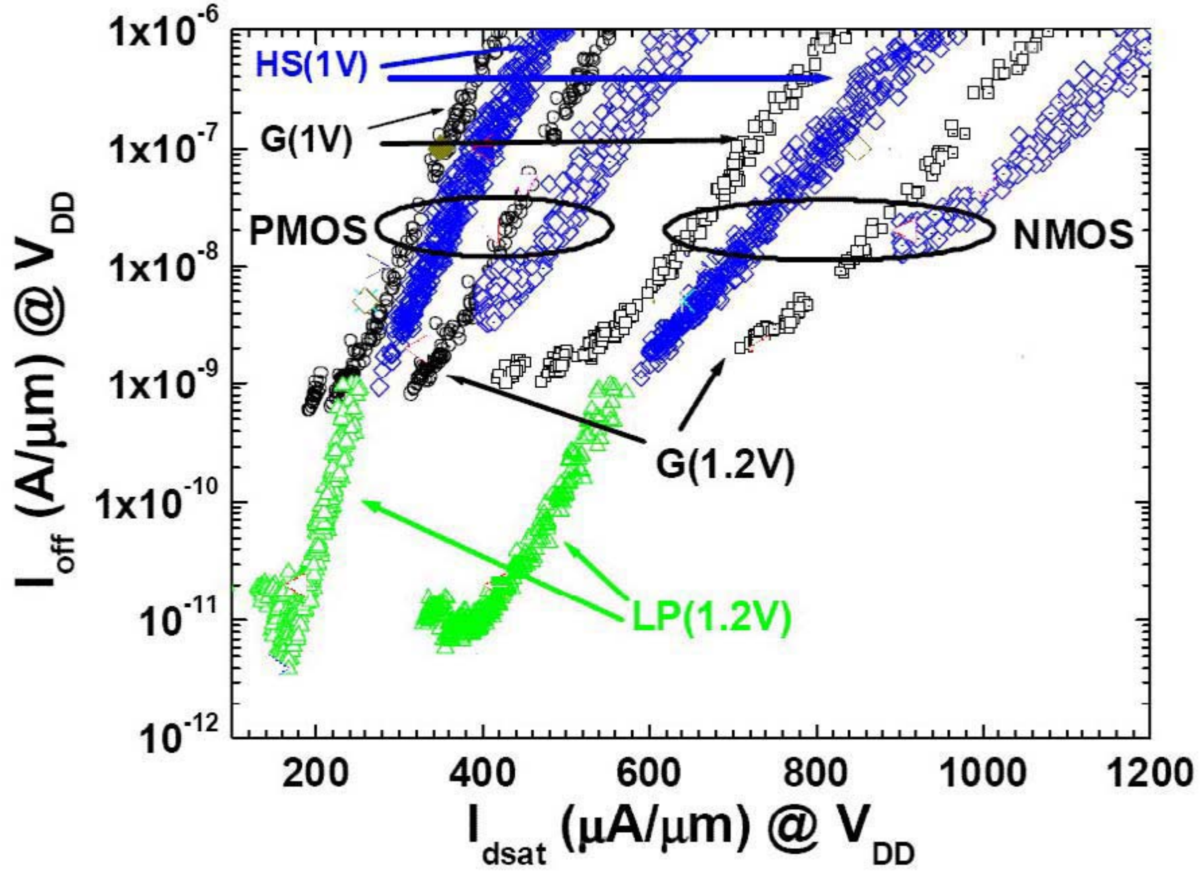
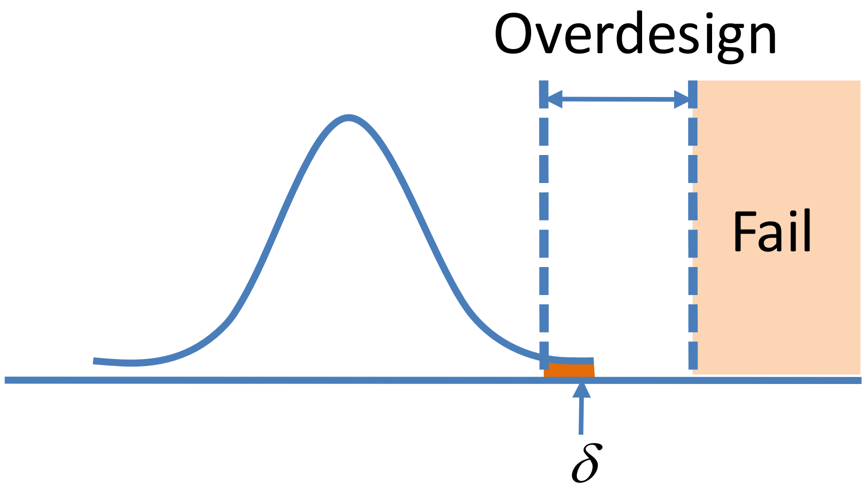
Off-power issues



Leakage Current Variability in Nanometer Technologies, Mohab Anis and Mohamed H. Aburahma
Proceedings of the 9th International Database Engineering & Application Symposium (IDEAS'05)

Why does it hurt

- If we cannot correctly assess the impact of variability, then we must resort to a conservative design approach



- Overdesign causes penalty in area, power, etc.

Why is it such a hard problem?

- Dual Nature: Random vs. Systematic
- Various levels of *Hierarchy*
  - die, field, wafer, lot
- Various *consumers* of variability information
  - device, process, circuit engineers
- A large portion of variability is <u>*not stationary*</u>

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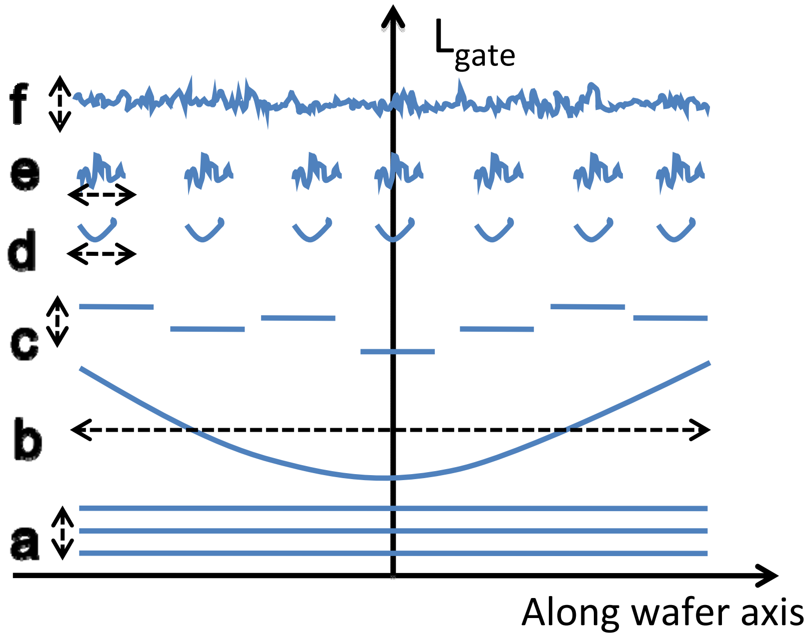
Hierarchical Spatial Variability Model

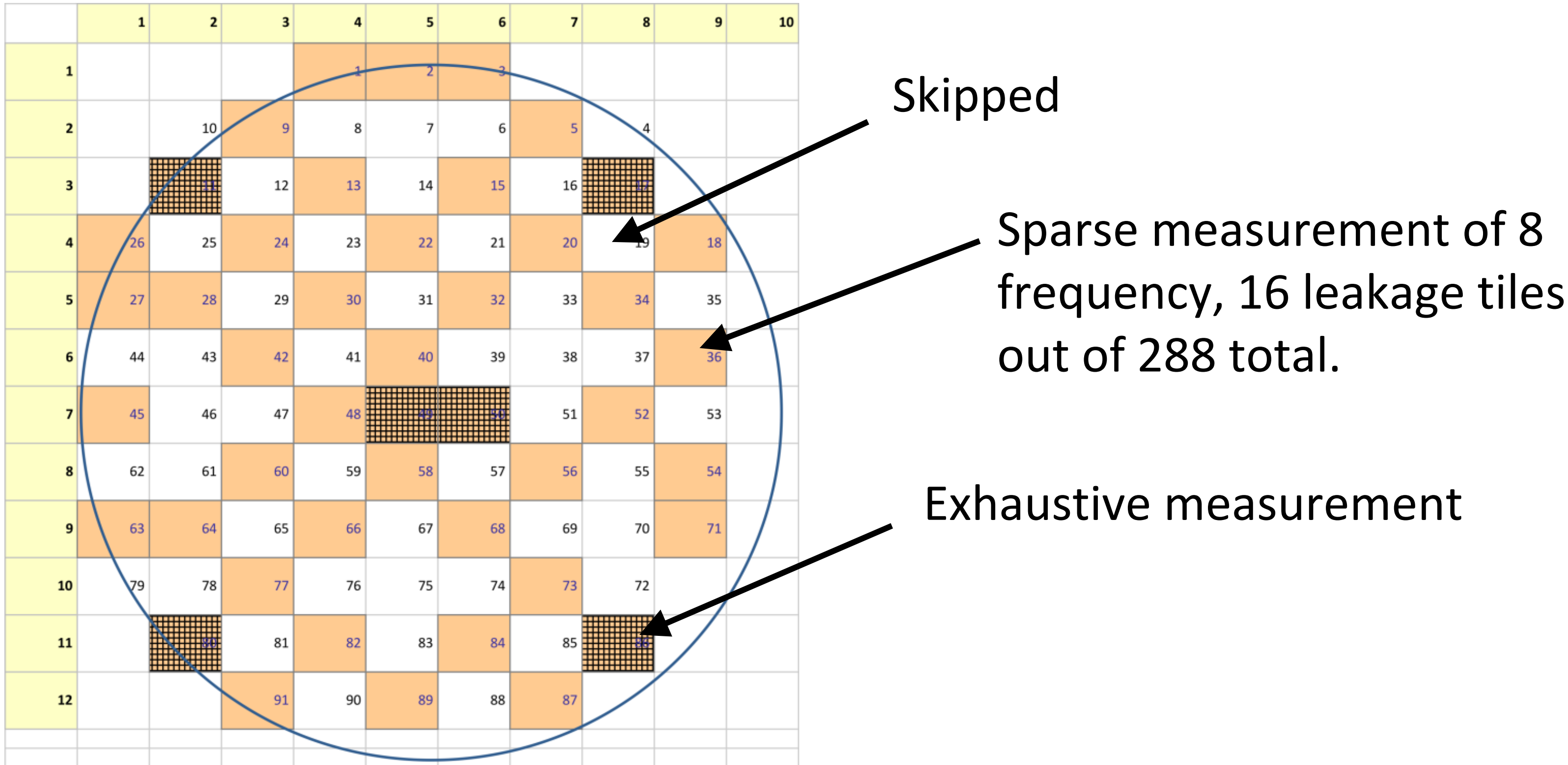


Variability components[1]

a) Wafer-to-wafer: random
b) Across-wafer: parabola
c) Die-to-die: random
d) Across-die: parabola
e) Layout dependent
f) Within-die: random

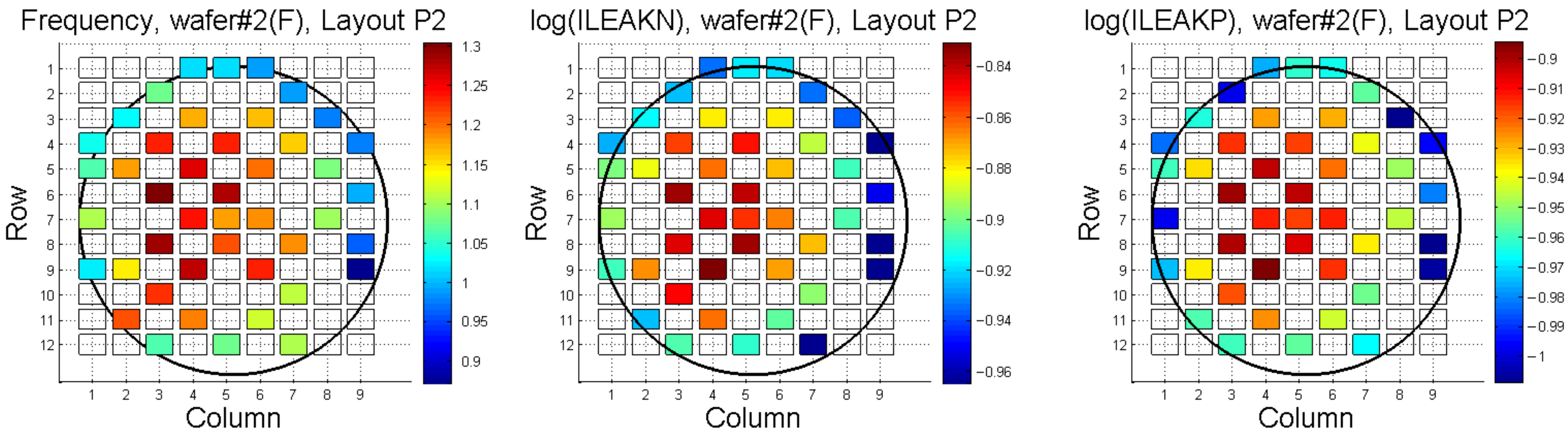
[1] Kun Qian, Costas J. Spanos, SPIE 2008

45nm Chip Sampling Scheme



- Sparsely measured chips provide good coverage of the wafer
- Small number of chips measured exhaustively
- Spatial emphasis near wafer edge where the variability is evident

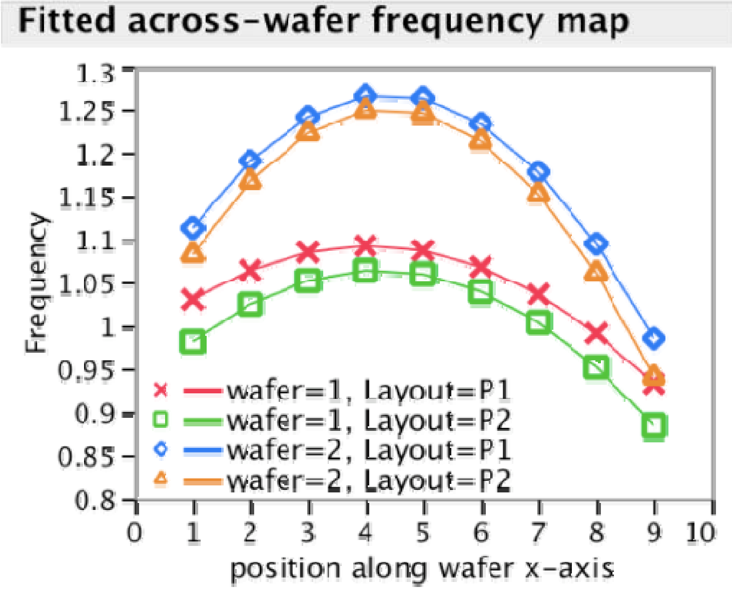
Wafer level Measurement
(& a variability "language")

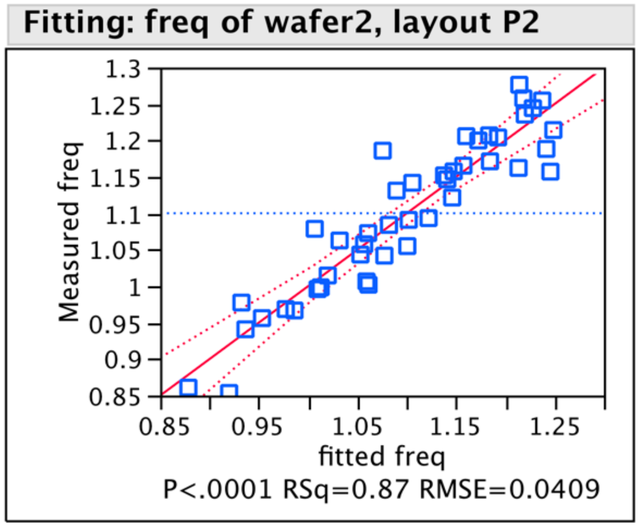


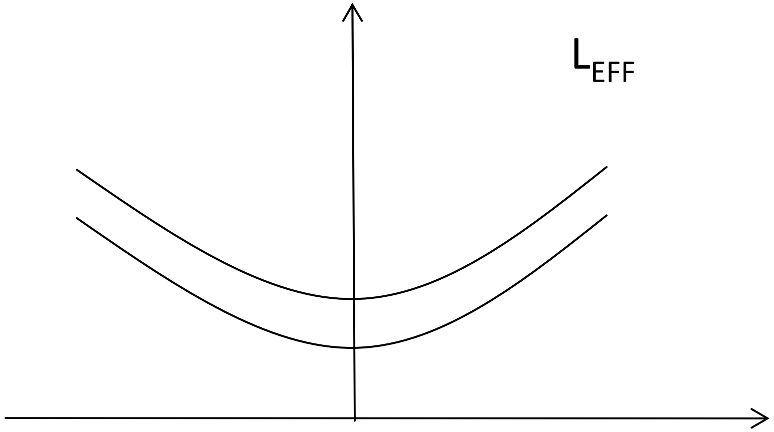
(a) $\overline{f}\left\langle \bullet, D, W2, P2 \right\rangle$ (b) $\overline{\log\left(I_{LEAKN}\right)}\left\langle \bullet, D, W2, P2 \right\rangle$ (c) $\overline{\log\left(I_{LEAKP}\right)}\left\langle \bullet, D, W2, P2 \right\rangle$

- Four indices: *copy*, *die*, *wafer*, *pattern*.
- A dot implies averaging over the respective index.
- Chip average of the measured RO frequency, log(I_{LEAKN}) and log(I_{LEAKP})
- Dome shape across wafer is evident (and rather common)

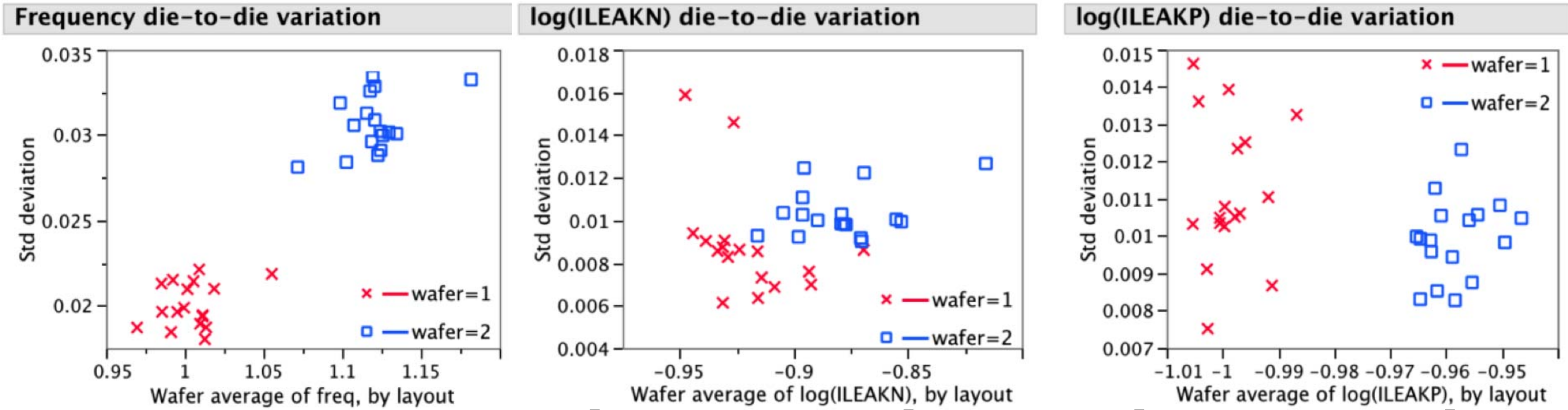
Across-wafer: Parabolic Fitting







- Bowl shape across-wafer gate CD variation (PEB, Etching)
- RO frequency has non-linear sensitivity to the L_{EFF} variation.
- Similar parabolic functions fitted to $\log(I_{LEAKN})$ and $\log(I_{LEAKP})$.



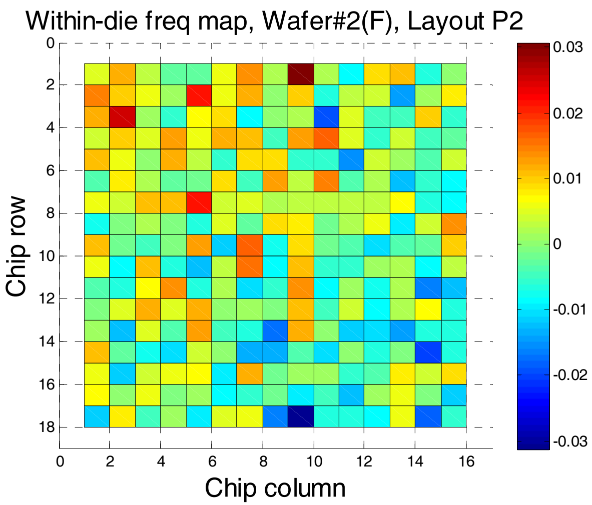
(a) $\sigma_D\left(f-\bar{f}\big|_{AW}\right)\langle\bullet,D,W,P\rangle$ vs. $\bar{f}\langle\bullet,\bullet,W,P\rangle$

(b) $\sigma_D\left[\overline{\log(I_{LEAKN})}-\overline{\log(I_{LEAKN})}\Big|_{AW}\right]\langle\bullet,D,W,P\rangle$ vs. $\overline{\log(I_{LEAKN})}\langle\bullet,\bullet,W,P\rangle$

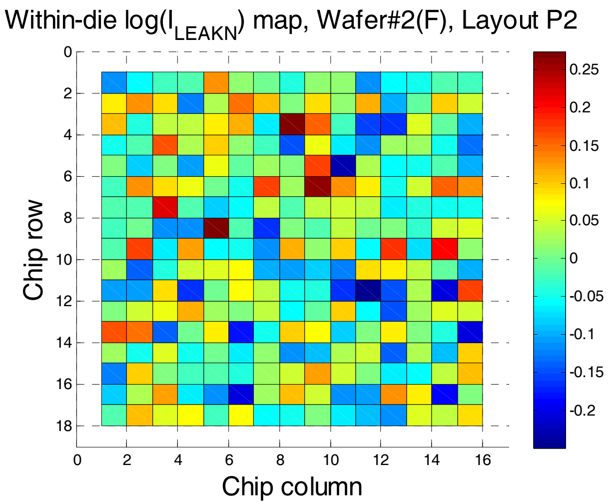
(c) $\sigma_D\left[\overline{\log(I_{LEAKP})}-\overline{\log(I_{LEAKP})}\Big|_{AW}\right]\langle\bullet,D,W,P\rangle$ vs. $\overline{\log(I_{LEAKP})}\langle\bullet,\bullet,W,P\rangle$

- Frequency is similar to systematic across-wafer variation
- $\log(I_{LEAKN})$ and $\log(I_{LEAKP})$ are comparable between two wafers

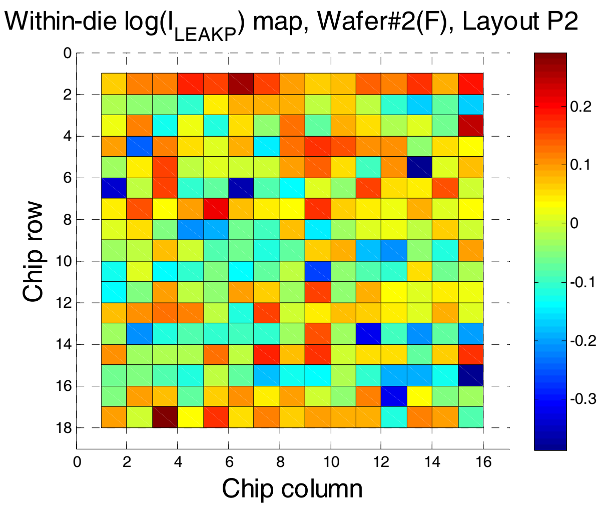
Within-die Variation: Random



(a) $\overline{f}\left\langle T,\bullet,W2,P2\right\rangle$



(b) $\overline{\log\left(I_{LEAKN}\right)}\left\langle T,\bullet,W2,P2\right\rangle$

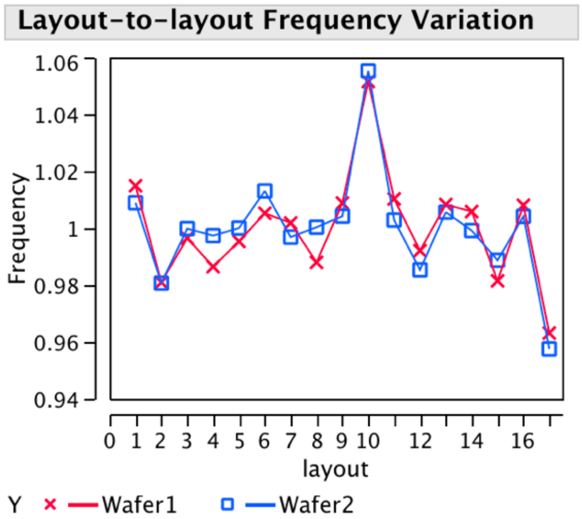


(c) $\overline{\log\left(I_{LEAKP}\right)}\left\langle T,\bullet,W2,P2\right\rangle$

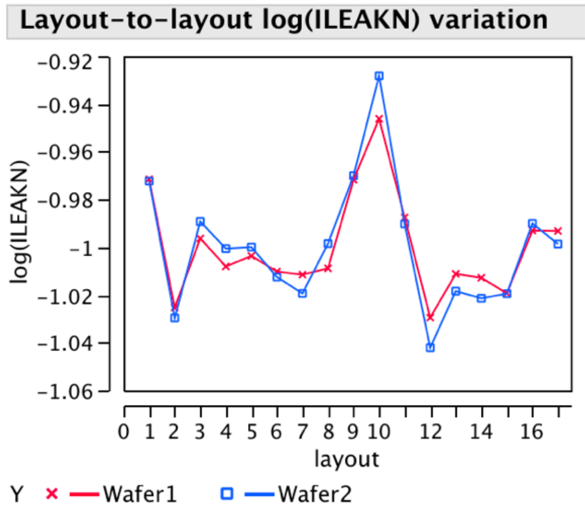
Systematic across-die variation is non-existent in our dataset:

- Die size is very small compared to the field size
- Purely random component, *NO* spatial correlation (more later…)

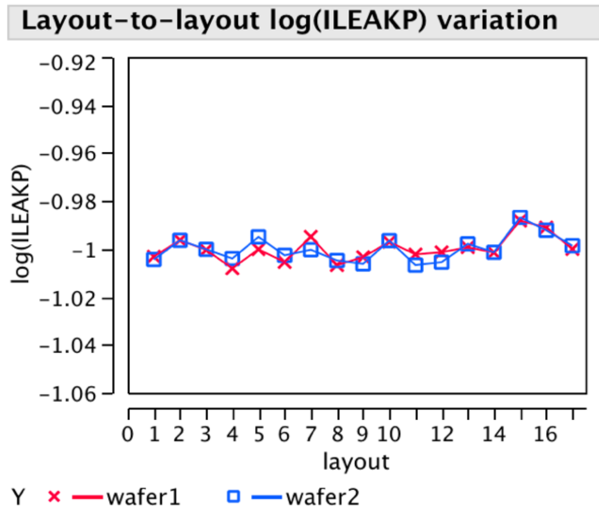
Pattern Effect Analysis



(a) $\overline{fL}\left\langle \bullet, W, P \right\rangle$



(b) $\overline{INL}\left\langle \bullet, W, P \right\rangle$



(c) $\overline{IPL}\left\langle \bullet, W, P \right\rangle$

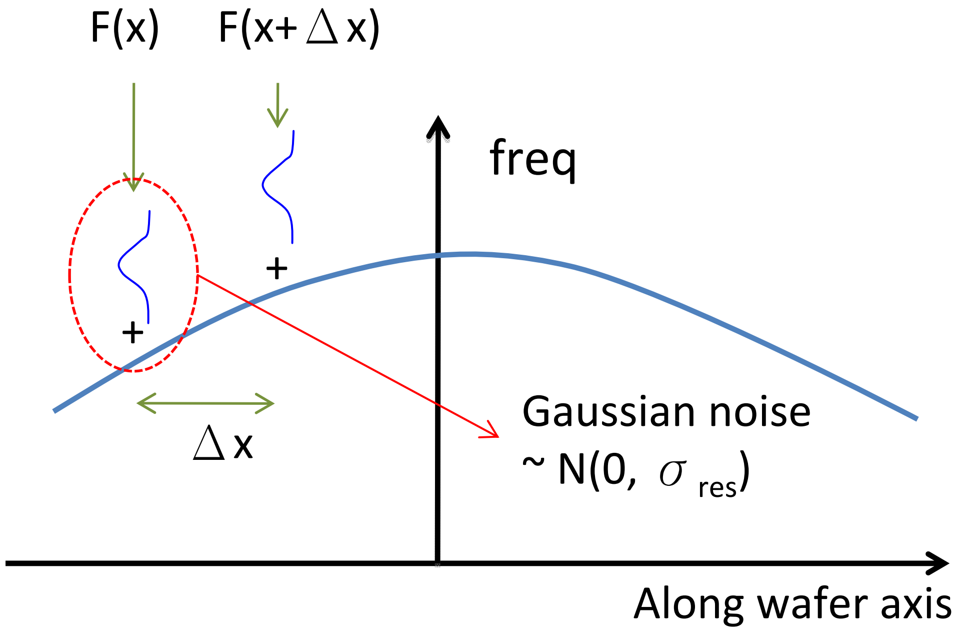
$$fL\left\langle D, W, P \right\rangle \equiv \frac{\overline{f}\left\langle \bullet, D, W, P \right\rangle}{\overline{f}\left\langle \bullet, D, W, \bullet \right\rangle}$$

$$INL\left\langle D, W, P \right\rangle \equiv \frac{\overline{\log\left(I_{LEAKN}\right)}\left\langle \bullet, D, W, P \right\rangle}{\overline{\log\left(I_{LEAKN}\right)}\left\langle \bullet, D, W, \bullet \right\rangle}$$

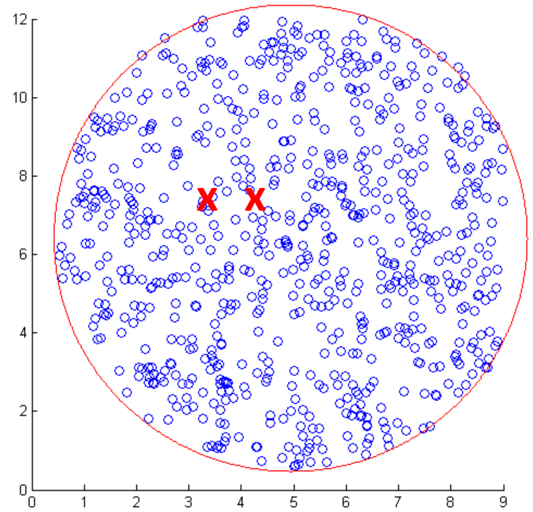
$$IPL\left\langle D, W, P \right\rangle \equiv \frac{\overline{\log\left(I_{LEAKP}\right)}\left\langle \bullet, D, W, P \right\rangle}{\overline{\log\left(I_{LEAKP}\right)}\left\langle \bullet, D, W, \bullet \right\rangle}$$

- Systematic pattern dependent effect
- Log(I_{LEAKP}) layout-to-layout variation is relatively small
- Freq and log(I_{LEAKN}) trend is highly correlated, but not log(I_{LEAKP})
- Freq & NMOS: Strain induced V_{TH} variation; PMOS: OPC residual in L_{EFF}

*Apparent** Spatial correlation



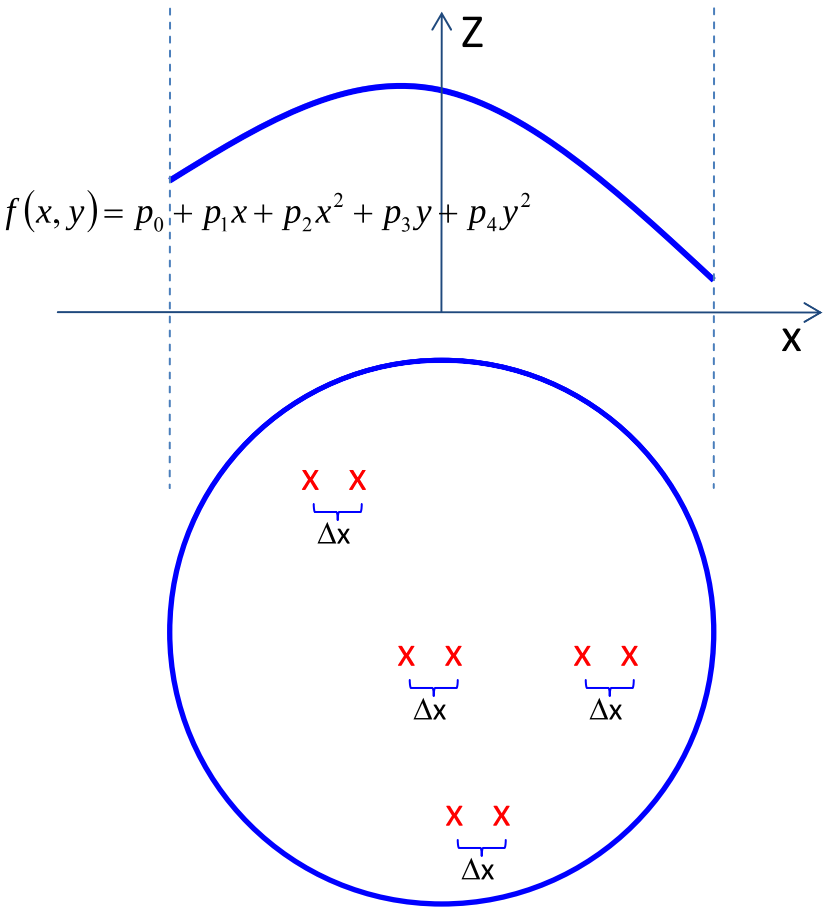
Device/chip position on wafer is **random**



- Frequency of a pair of device are random
  - their position on wafer and chip is random
  - There is local white noise
- Spatial correlation is the result of underlying systematic across-wafer & across-chip function (non-existent for the 45nm test-chip)

* Warning - "controversial"

Apparent Correlation Formulation



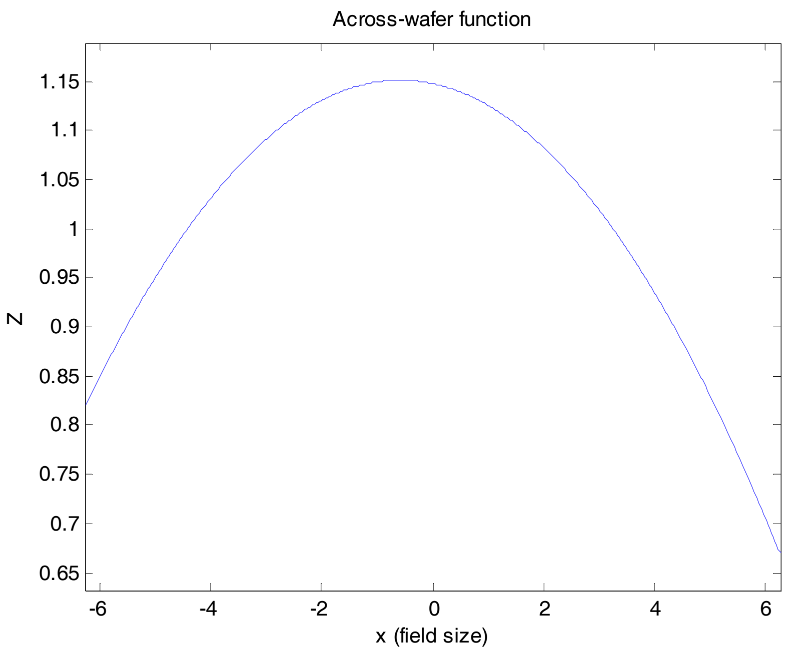
$$Z_1 = f(x,y) + e_1$$

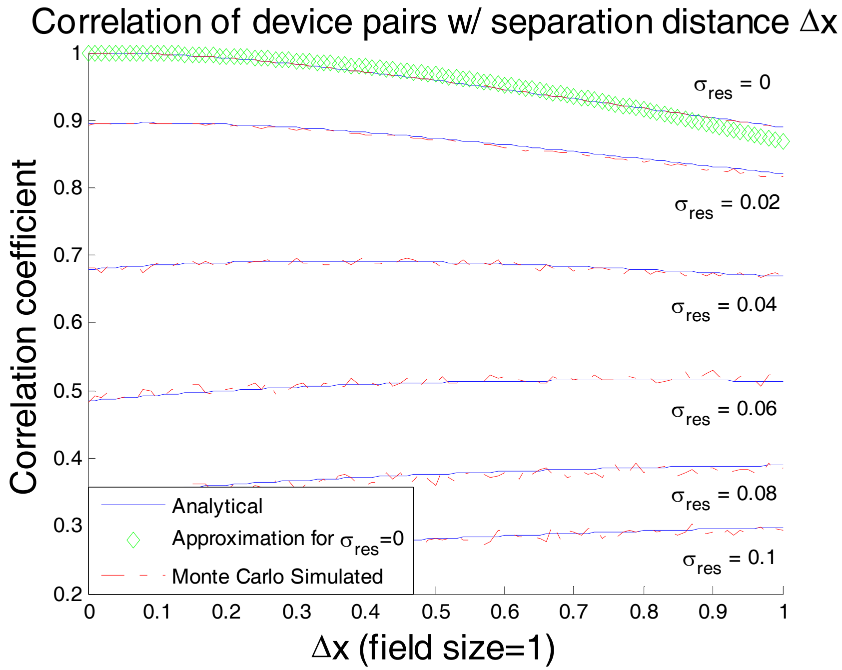
$$Z_2 = f(x+\Delta x, y) + e_2$$

$$\approx f(x,y) + \frac{\partial f(x,y)}{\partial x}\Delta x + e_2$$

- Z can be device or circuit parameter, e.g. L_{GATE}, RO freq
- Sources of randomness
  - Unknown position on wafer
  - Local random component

Apparent Spatial Correlation





- Analytical formula is verified by MC simulation
- Approximation formula is good for small Δx

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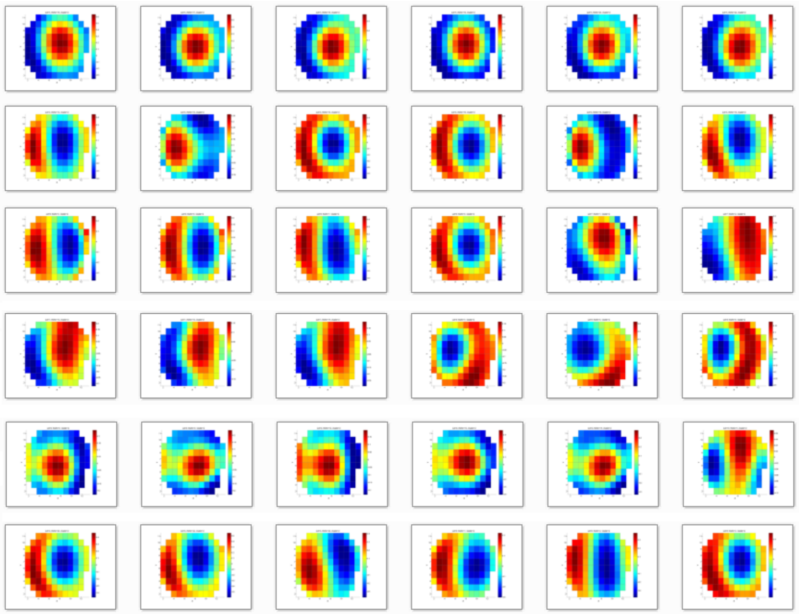
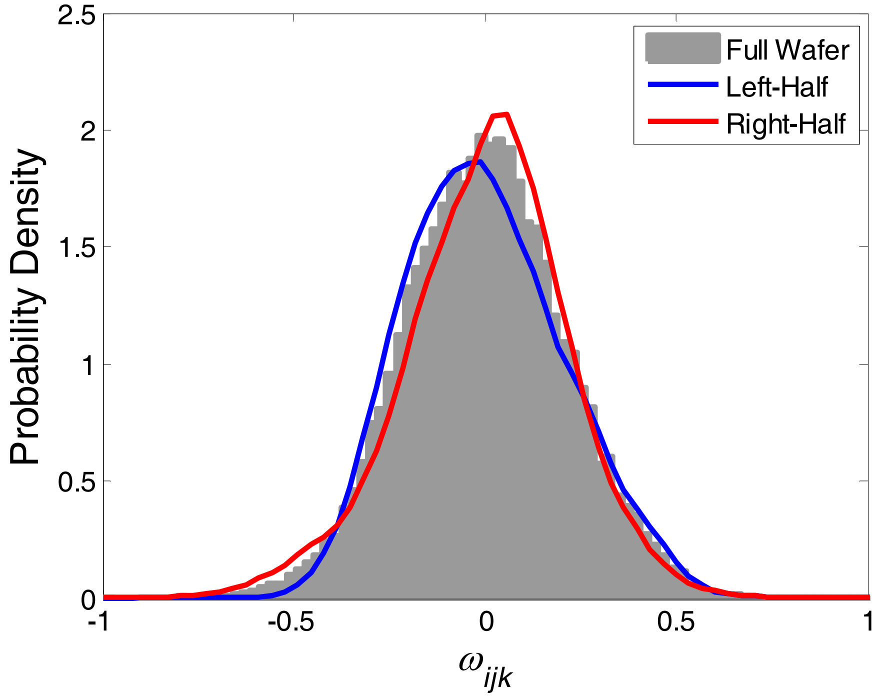
Model Hierarchy (lot, wafer, within wafer, within die)

$$p_{ijkl} = \eta + \lambda_i + \sigma_j + \rho_{ij} + \boxed{\beta_k + \omega_{ijk}} + \boxed{\gamma_l + \tau_{kl}} + \epsilon_{ijkl}$$

Model Estimator	Meaning
$\hat{\eta} = \bar{p}_{....}$	Global Mean
$\hat{\lambda}_i = \bar{p}_{i...} - \bar{p}_{....}$	Lot Factor
$\hat{\sigma}_j = \bar{p}_{.j..} - \bar{p}_{....}$	Wafer or Slot Factor
$\hat{\rho}_{ij} = \bar{p}_{ij..} - \bar{p}_{i...} - \bar{p}_{.j..} + \bar{p}_{....}$	Lot-Wafer Interaction Factor
$\hat{\beta}_k = \bar{p}_{..k.} - \bar{p}_{....}$	Average Wafer
$\hat{\omega}_{ijk} = \bar{p}_{ijk.} - \bar{p}_{ij..} - \bar{p}_{..k.} + \bar{p}_{....}$	Deviation from Average Wafer
$\hat{\gamma}_l = \bar{p}_{...l} - \bar{p}_{....}$	Average Die
$\hat{\tau}_{kl} = \bar{p}_{..kl} - \bar{p}_{..k.} - \bar{p}_{...l} + \bar{p}_{....}$	Die-Site Interaction Factor
$\hat{\epsilon}_{ijkl} = p_{ijkl} - \bar{p}_{ijk.} + \bar{p}_{..k.} - \bar{p}_{..kl}$	Residual

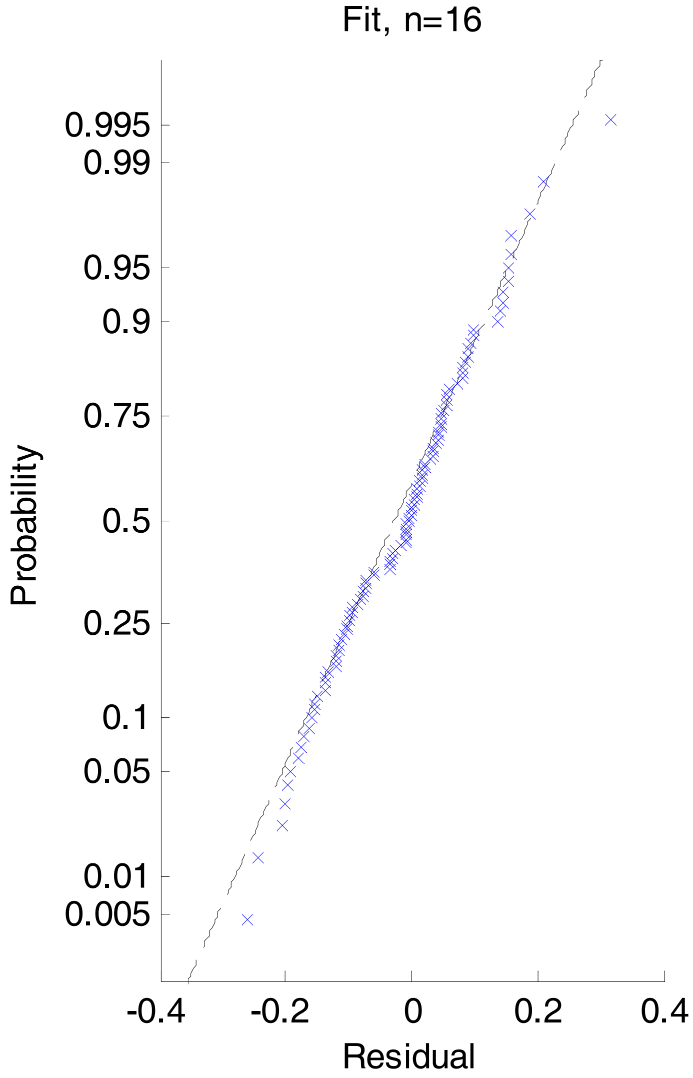
The Statistics of Systematic Variability

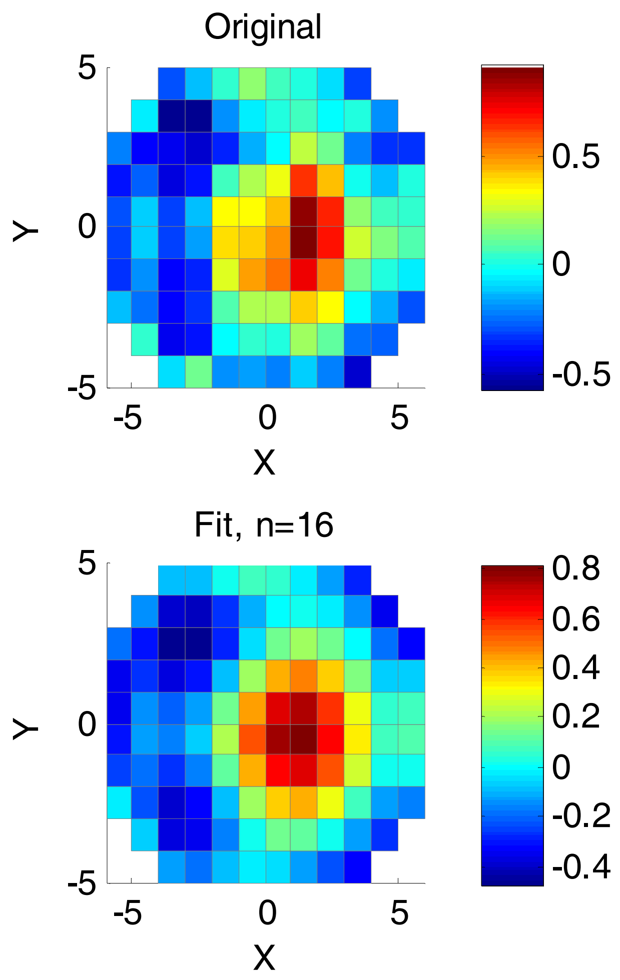




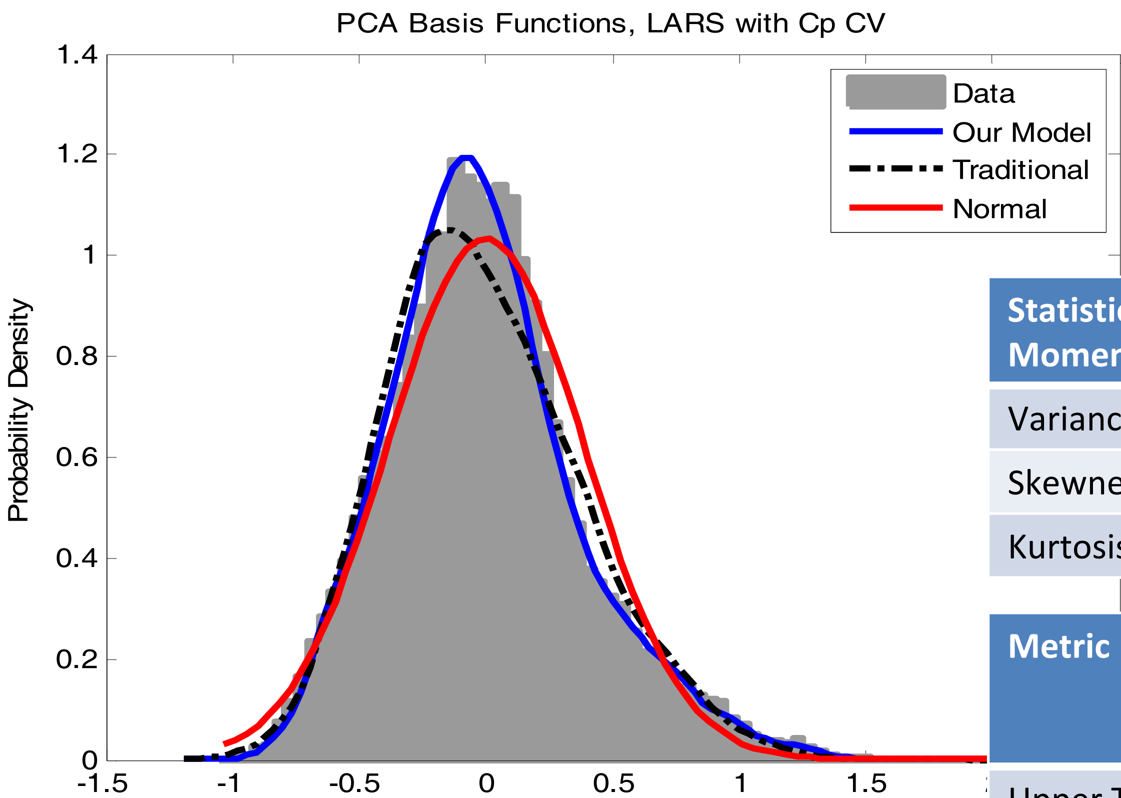
- Propose a model to capture statistics of systematic variability
- Propose and demonstrate a solution at inter-die level
- Extend it to intra-die level

Average Wafer





Results using PCA Basis Functions



Statistical Moment	Data	Traditional Model	Our Model
Variance	0.149	0.147	0.142
Skewness	0.545	0.401	0.563
Kurtosis	3.555	3.002	3.544

Metric	% Actual Data [95% CI]	% Traditional Model	% Our Model
Upper Tail	1.47 [1.34, 1.61]	1.00	1.45
Lower Tail	0.02 [0.00, 0.03]	0.09	0.02
Out of Spec [-1, 1]	1.49 [1.35, 1.62]	1.00	1.45

Traditional Method:

$$\hat{\beta} + \varepsilon_{\hat{\omega}}$$

$$\varepsilon_{\hat{\omega}} \sim \mathcal{N}\left(0, \mathrm{var}(\hat{\omega}_{ijk})\right)$$

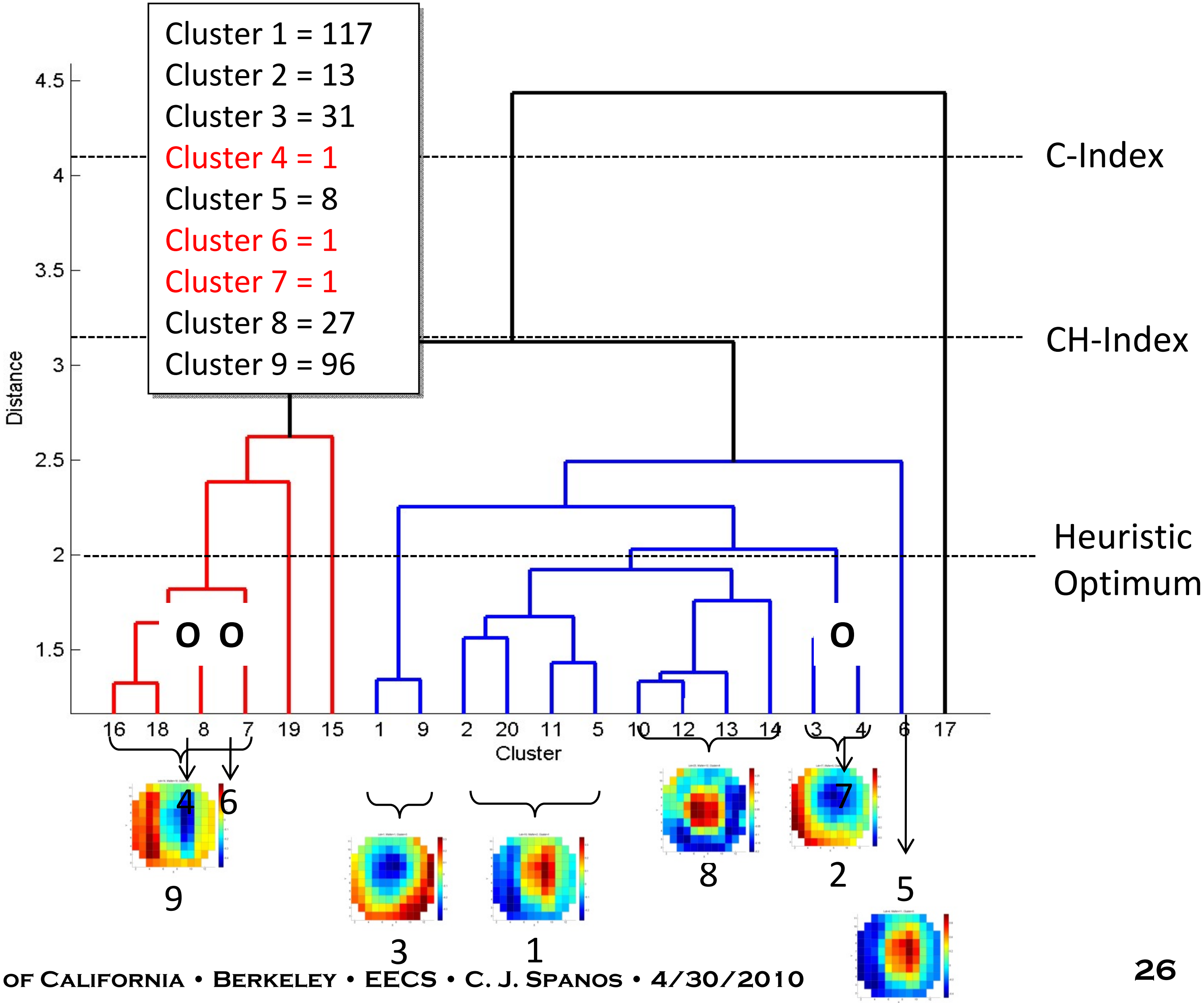
Proposed Method:

$$\hat{\beta} + \tilde{\omega} + \varepsilon_R$$

$$\varepsilon_R \sim \mathcal{N}\left(0, \sigma_R^2\right)$$

$$R = \hat{\omega}_{ijk} - \tilde{\omega}$$

A Bonus Application: Cluster Analysis



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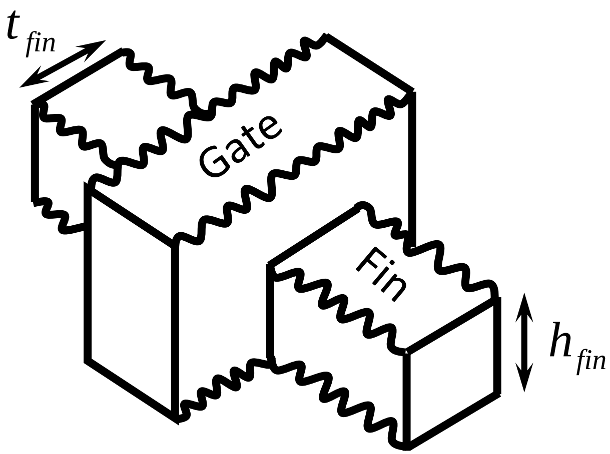
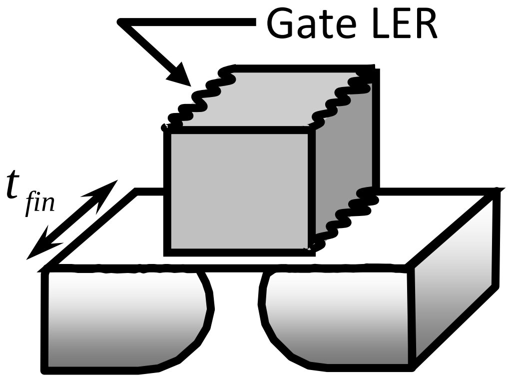
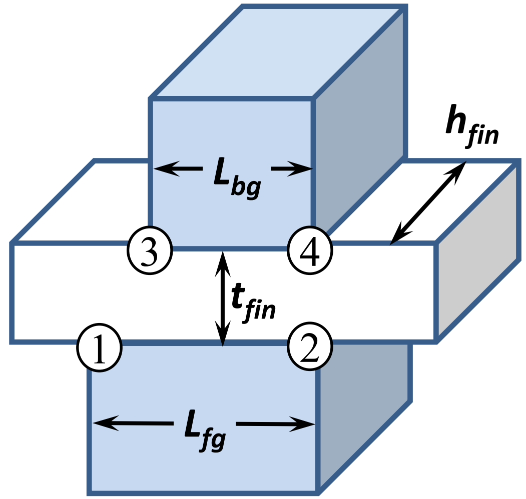
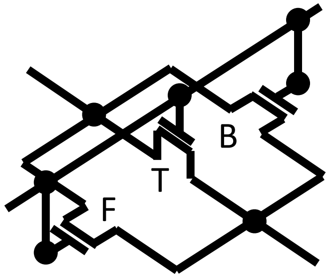
LER in FinFET

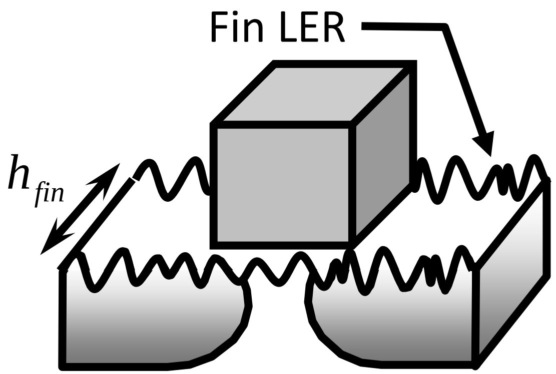




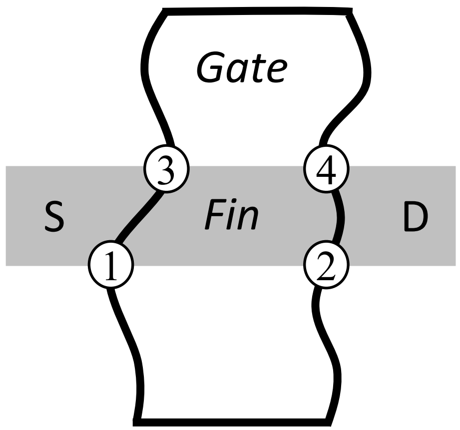
Top Gate







Front and Back Gates



LER Simulation Details

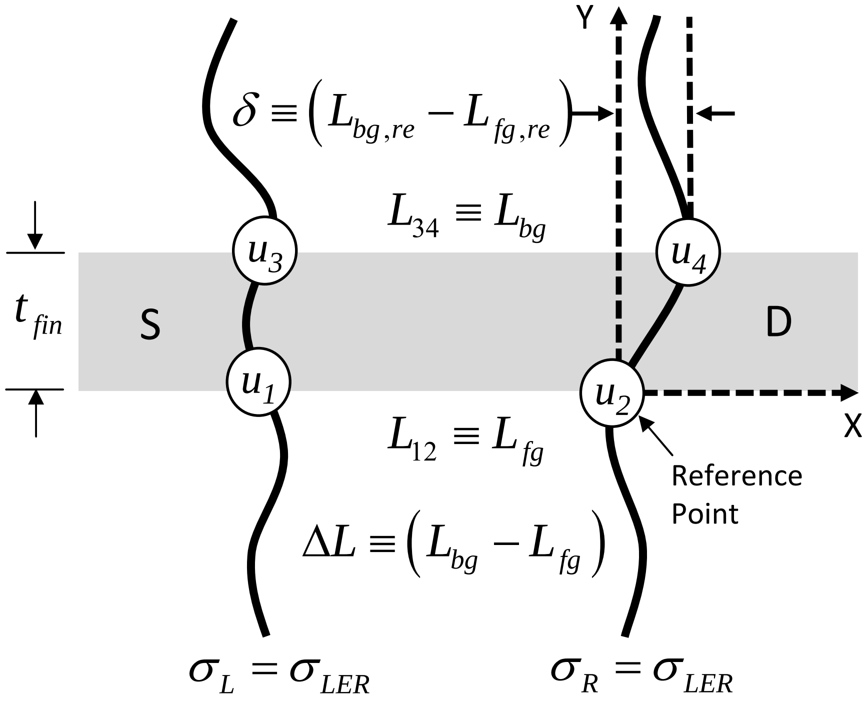
TABLE 1: 2-D DEVICE SIMULATION PARAMETERS

Electrical/Doping	Structural
V_{dd}=0.9V	L_g=13nm
ϕ_m=4.62eV	t_{ox}=6A
N_B=1e15 cm^{-3}	L_{sp}=7.2nm
$N_{s/d}$=1e20 cm^{-3}	t_{fin}=7.5nm
$\sigma_{s/d}$=4nm/dec	t_{poly}=13nm

TABLE 2: 2-D NOMINAL DEVICE PERFORMANCE PARAMETERS.

Parameter	Units	Value
$V_{t,sat}$	mV	210
SS	mV/dec	69
DIBL	mV/V	30
$g_{m,sat}$	mA/V	6.75
$I_{d,sat}$	mA/µm	2.48
I_{off}	pA/µm	94.4

LER Model Description



$$\sigma_{\delta}^{2} = 2\sigma_{LER}^{2}\left(1 - \rho_A(t_{fin})\right)$$

$$\rho(y) = e^{-\left(\frac{|y|}{\xi}\right)^{2\alpha}}$$

Auto-correlation function

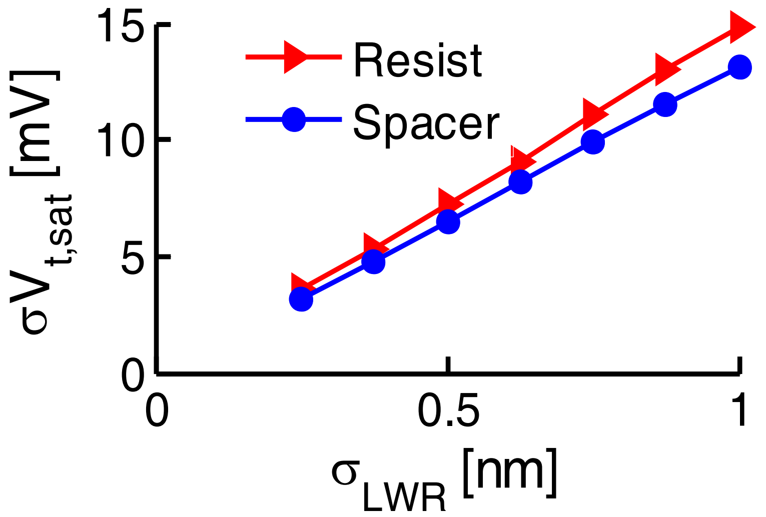
For a resist-defined gate electrode,

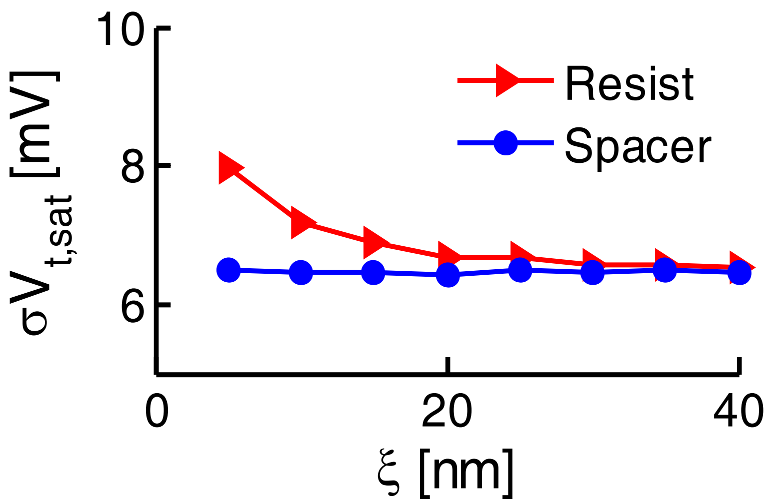
$$\sigma_{\Delta L}^{2} = 4\sigma_{LER}^{2}\left[1 - \rho_A(t_{fin})\right].$$

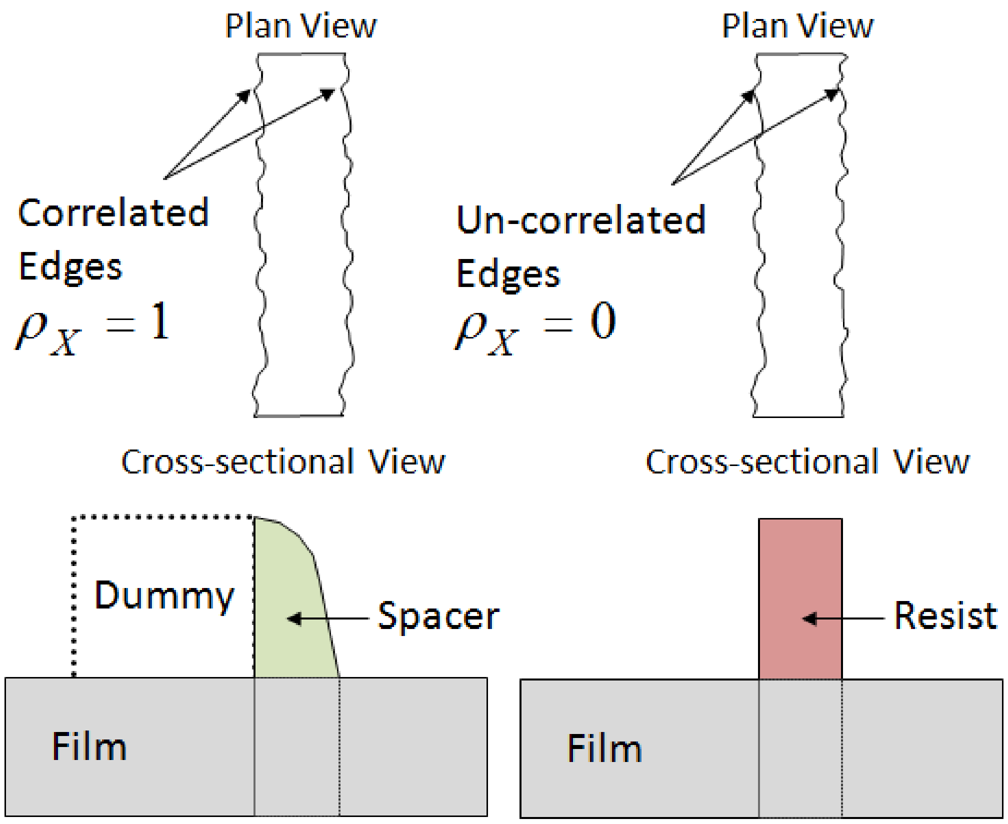
For a spacer-defined gate electrode ,

$$\sigma_{\Delta L}^{2} = 0$$

Spacer v. Resist







(a) Spacer Defined

(b) Resist Defined

$$\sigma_{LWR}^2 = 2\sigma_{LER}^2 \left(1-\rho_X\right)$$

$$\sigma_L = \sigma_R \equiv \sigma_{LER}$$

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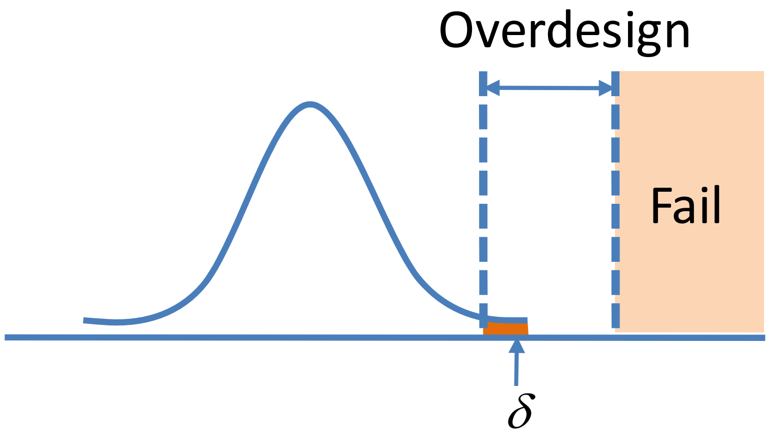
Reclaiming the Overdesign Margin

To design a circuit with yield 1-δ (failure probability δ)

Conservative design

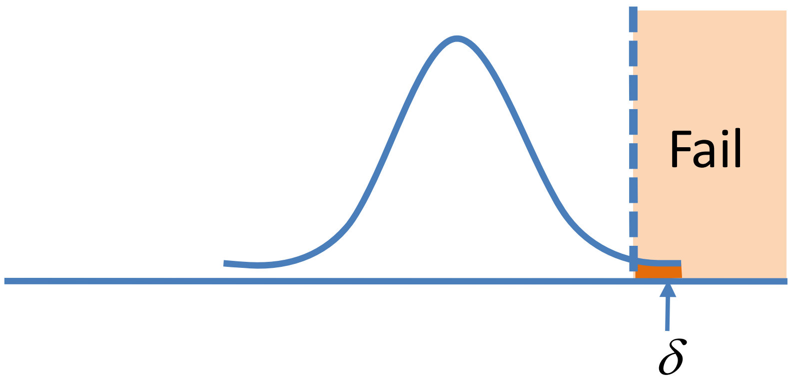
- Cannot correctly assess the impact of variability
- Resort to conservative approach



- Overdesign causes penalty in area, power etc.

Yield-constrained design

- Incorporate the yield in the design loop
- Resulting circuit has the desired yield



- Can achieve smaller area, power…

General Problem

Process parameter $y \in \Omega$ is random

$$\begin{array}{ll} \text{minimize} & A(x) \\ \text{subject to} & f(x) \leq 0 \end{array}$$

$$\begin{array}{ll} \text{minimize} & A(x) \\ \text{subject to} & P_f = P(y\colon f(x,y) > 0) < \delta \end{array}$$

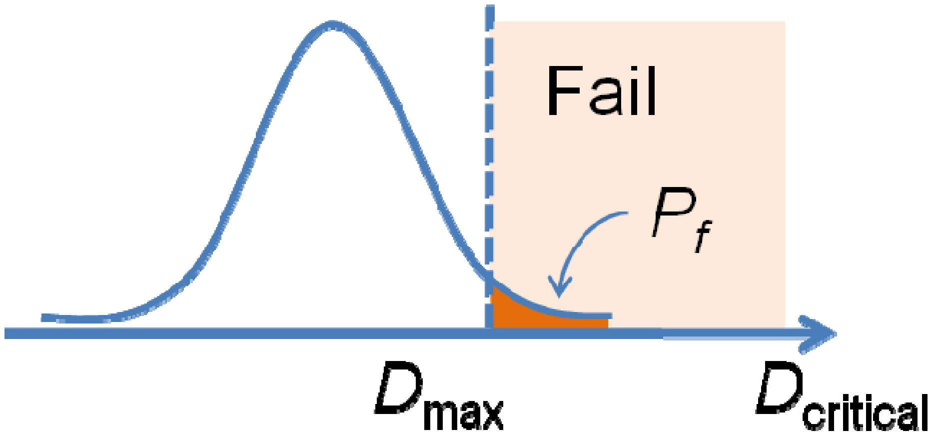
$$\begin{array}{ll} \text{minimize} & A(x) \\ \text{subject to} & \max_{y \in \Omega}(f(x,y)) \leq 0 \end{array}$$

Approximate $f(x,y)$ with $\hat{f}(x,y)$ such that the distribution of $\hat{f}(x,y)$ can be easily found

Problem:
- Usually gives pessimistic result
- Sometimes the worst-case cannot be well defined

Problem:
- Accuracy of the approximation
- Only limited types of distribution can be used
- Fidelity very bad at tail

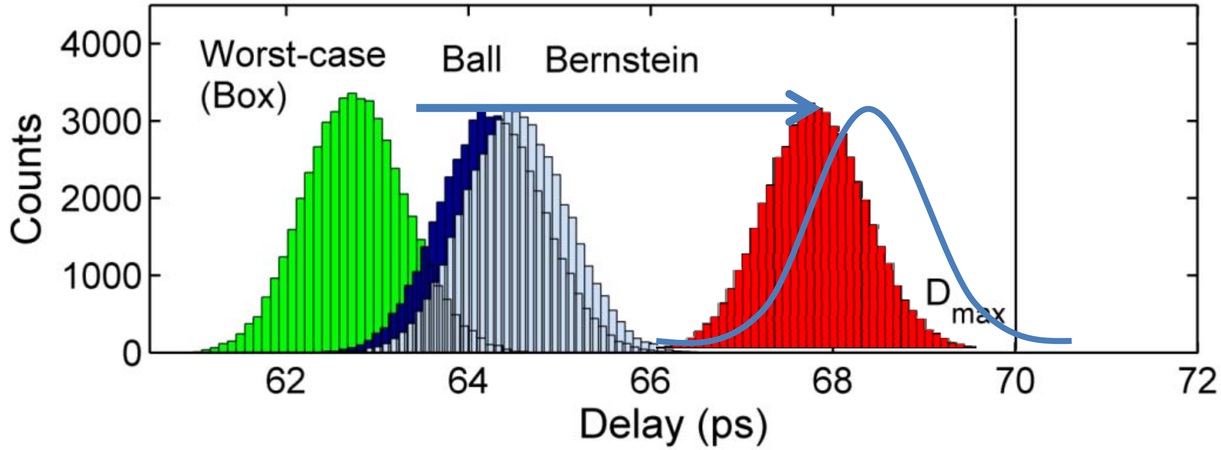
Yield-constrained Circuit Sizing



$$\begin{aligned} &\text{minimize} \quad && A(x) = a^T x \\ &\text{subject to} \quad && P_f = \text{Prob}\left(D_{\text{critical}} > D_{\max}\right) \le \delta \\ & && x \ge 1 \end{aligned}$$

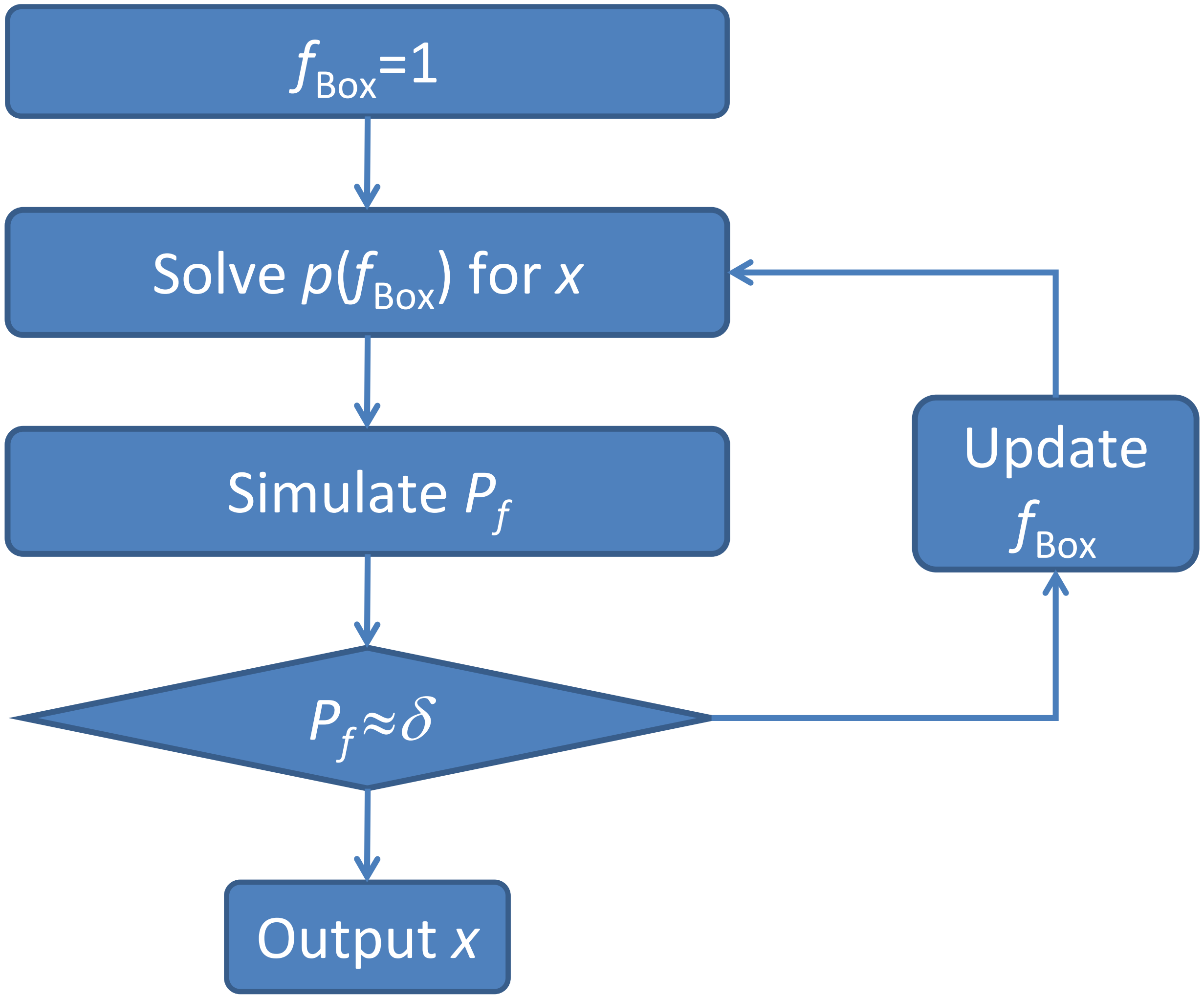
$$D_{\text{critical}} = \max_p \left(\sum_{i \in \text{path}(p)} (R_i^0 + R_g \zeta_g + R_i^r \zeta_i) \widetilde{C}_i(x) \right)$$

How to Remove Pessimism



- Observations
  - The design is pessimistically constrained
  - GP can be solved efficiently
  - Failure probability can be effectively obtained through simulation (next section)
- Sequential Geometric Programming

Sequential Geometric Programming

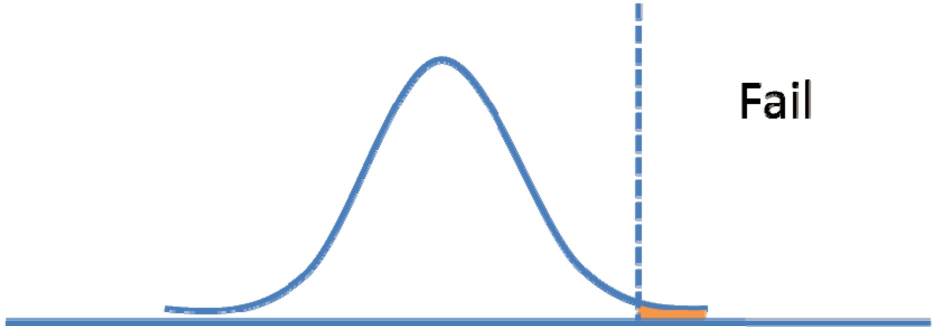


Monte Carlo

$$y = (y_g, y_1 \ldots y_m)^T \in \mathbf{R}^{m+1}$$

$$\{y_r\}_{r=1}^{R} \sim g(y)$$

$$\hat{P}_f = \frac{1}{R} \sum_{r=1}^{R} \mathbf{1}\left(D_{\text{critical}}(y_r) > D_{\max}\right)$$

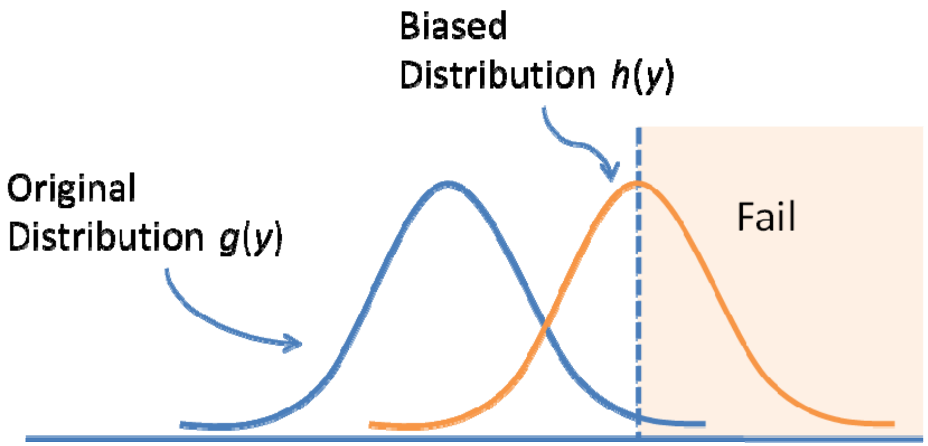


- Variance of the estimate $\mathrm{Var}(\hat{P}_f) = \frac{1}{R}(P_f - P_f^2).$

- In order for $\sqrt{\mathrm{Var}(\hat{P}_f)} \Big/ P_f \leq k$

$$R = \frac{1}{k^2} \cdot \frac{1 - P_f}{P_f}$$

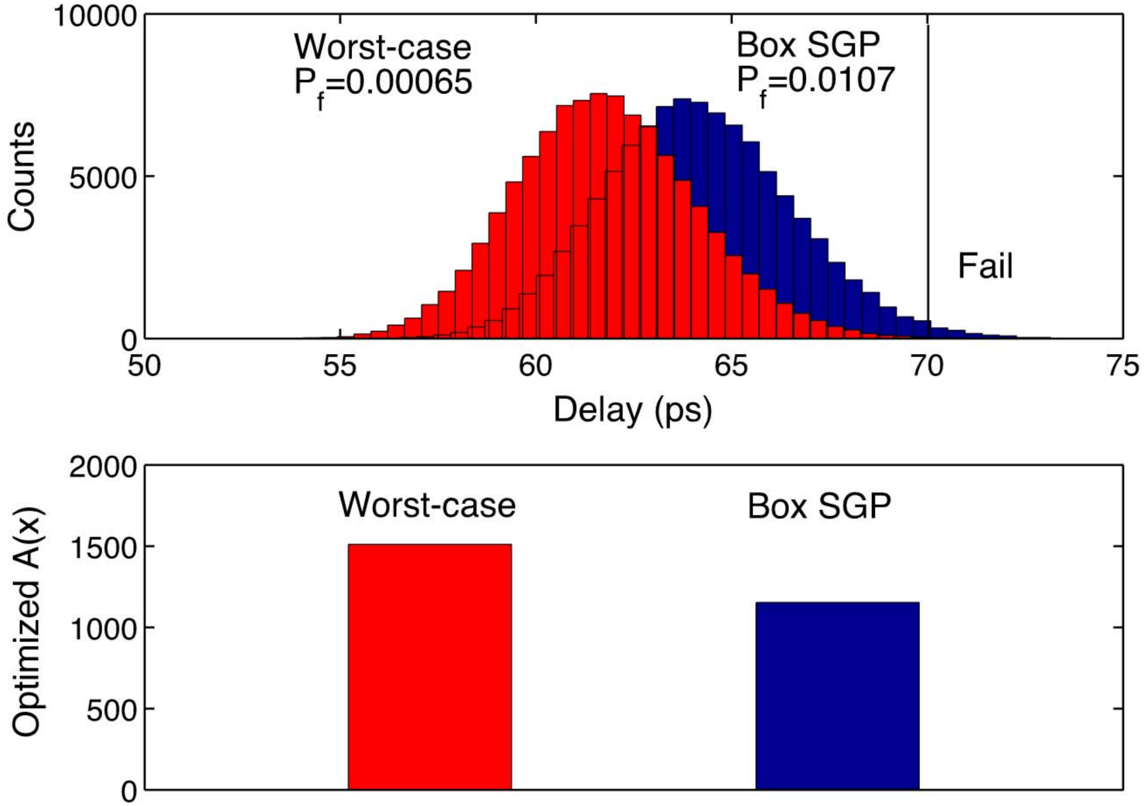
Importance Sampling



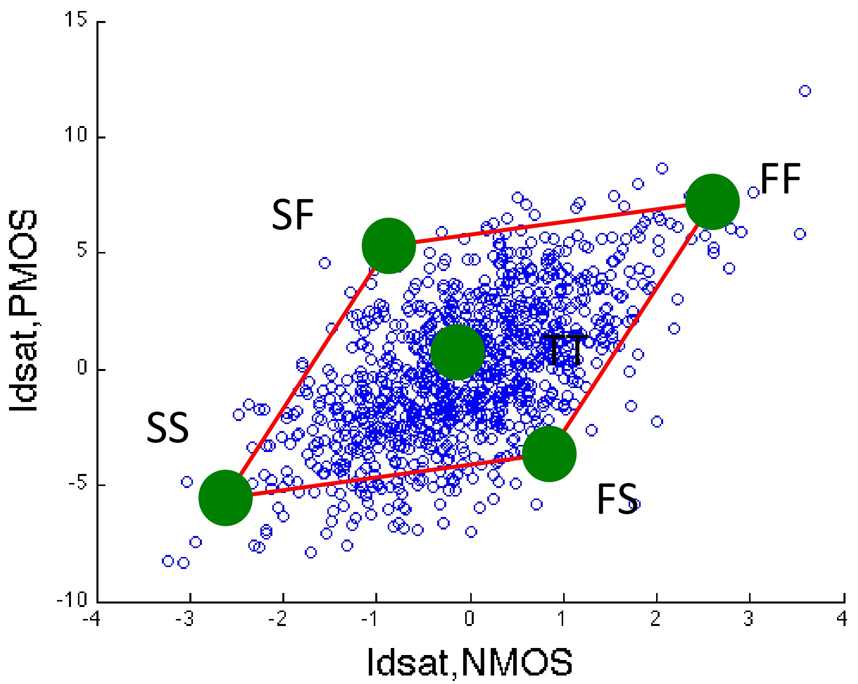
$$P_f = \int \mathbf{1}\left(D_{\text{critical}}(y) > D_{\max}\right) g(y)\,\mathrm{d}y$$

$$= \int \left(\mathbf{1}\left(D_{\text{critical}}(y) > D_{\max}\right) \frac{g(y)}{h(y)} \right) h(y)\,\mathrm{d}y$$

SGP Example: 8-bit Adder



Conventional Model Extraction



- Corner models deals with worst cases, is often too pessimistic.
- Strictly models only a couple transistors in extreme conditions

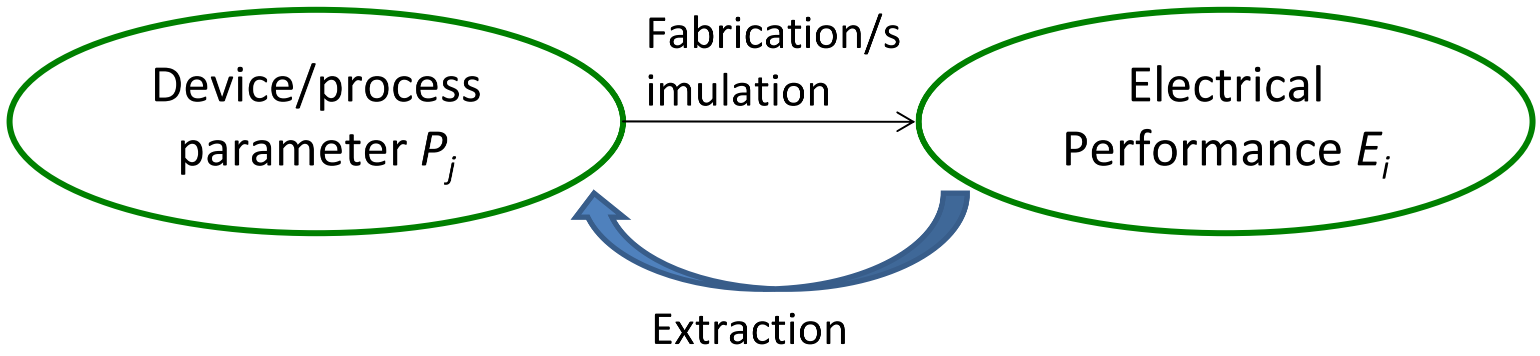
For each process split (extreme condition)
Pick a nominal die in terms of speed/power

For each nominal die
Pick a set of transistors of different drawn size
Which is close to the "median"

Extraction a
Parameter set for each performance corner
$\{Pi\}_{Fast}$, $\{Pi\}_{Slow}$, $\{Pi\}_{Typical}$

Generic Compact Model Extraction

- Electrical test data E_i: Id-Vg, Cg-Vg, etc.
  Device parameter P_j: vfbo, uo, toxo, nsubo, etc.
  Model equations: $\{E_i\} = f_k(\{P_j\})$
- Goal: optimize parameter set $\{P_j\}$ to fit the electrical measurements $\{E_i\}$ while <u>keeping the spatial variation information</u>



Statistical Model Extraction

$$\begin{bmatrix} \sigma^2_{\delta V_{tr}} \\ \sigma^2_{\frac{\delta\beta_r}{\beta_r}} \\ \sigma^2_{\delta V_{ts}} \\ \sigma^2_{\frac{\delta I_{ss}}{I_{ss}}} \end{bmatrix} = \begin{bmatrix} \left(T_{ox}\frac{\partial V_{tr}}{\partial T_{ox}}\right)^2 & \left(\frac{\partial V_{tr}}{\partial V_{fb}}\right)^2 & \left(\mu_0\frac{\partial V_{tr}}{\partial \mu_0}\right)^2 & \left(\frac{\partial V_{tr}}{\partial \Delta_L}\right)^2 & \left(\frac{\partial V_{tr}}{\partial V_{tl}}\right)^2 \\ \left(\frac{T_{ox}}{\beta_r}\frac{\partial \beta_r}{\partial T_{ox}}\right)^2 & \left(\frac{1}{\beta_r}\frac{\partial \beta_r}{\partial V_{fb}}\right)^2 & \left(\frac{\mu_0}{\beta_r}\frac{\partial \beta_r}{\partial \mu_0}\right)^2 & \left(\frac{1}{\beta_r}\frac{\partial \beta_r}{\partial \Delta_L}\right)^2 & \left(\frac{1}{\beta_r}\frac{\partial \beta_r}{\partial V_{tl}}\right)^2 \\ \left(T_{ox}\frac{\partial V_{ts}}{\partial T_{ox}}\right)^2 & \left(\frac{\partial V_{ts}}{\partial V_{fb}}\right)^2 & \left(\mu_0\frac{\partial V_{ts}}{\partial \mu_0}\right)^2 & \left(\frac{\partial V_{ts}}{\partial \Delta_L}\right)^2 & \left(\frac{\partial V_{ts}}{\partial V_{tl}}\right)^2 \\ \left(\frac{T_{ox}}{I_{ss}}\frac{\partial I_{ss}}{\partial T_{ox}}\right)^2 & \left(\frac{1}{I_{ss}}\frac{\partial I_{ss}}{\partial V_{fb}}\right)^2 & \left(\frac{\mu_0}{I_{ss}}\frac{\partial I_{ss}}{\partial \mu_0}\right)^2 & \left(\frac{1}{I_{ss}}\frac{\partial I_{ss}}{\partial \Delta_L}\right)^2 & \left(\frac{1}{I_{ss}}\frac{\partial I_{ss}}{\partial V_{tl}}\right)^2 \end{bmatrix} \begin{bmatrix} \sigma^2_{\frac{\delta T_{ox}}{T_{ox}}} \\ \sigma^2_{\delta V_{fb}} \\ \sigma^2_{\frac{\delta\mu_0}{\mu_0}} \\ \sigma^2_{\delta\Delta_L} \\ \sigma^2_{\delta V_{tl}} \end{bmatrix}$$

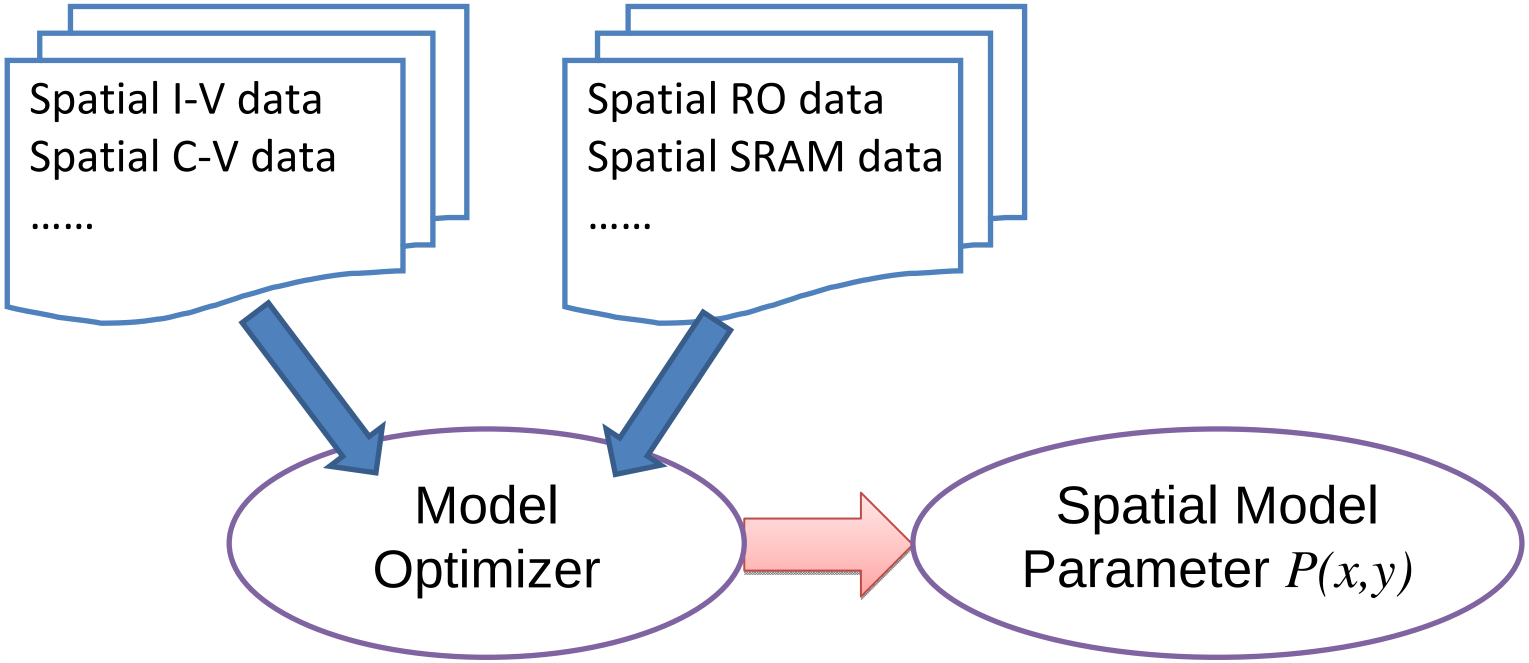
$$\sigma^2_{E_i} = \sum_j \left(\frac{\partial E_i}{\partial P_j}\right)^2 \sigma^2_{P_j}$$

*McAndrew, 2008

- Backward Variance Propagation method
- Solve for variance of physical parameters (unlike PCA method)
- Assumes Gaussian distribution of P_j and E_i

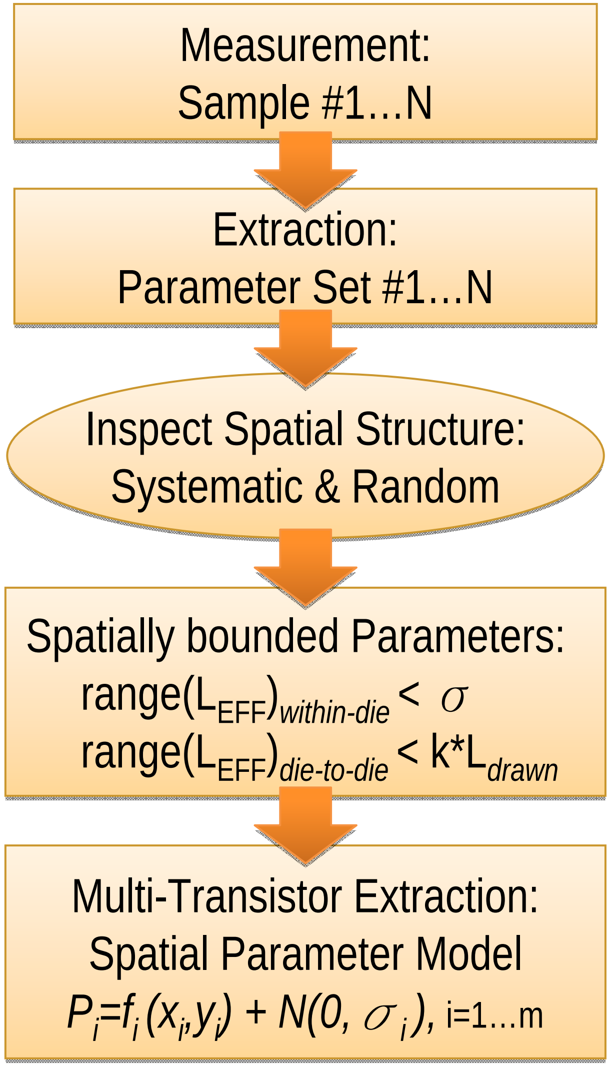
Towards a "variation-aware" compact model

- In the presence of spatial variability data, compact models should capture characteristics of transistors over large space, instead of just the worst case conditions.
- Model parameters should contain spatial component.

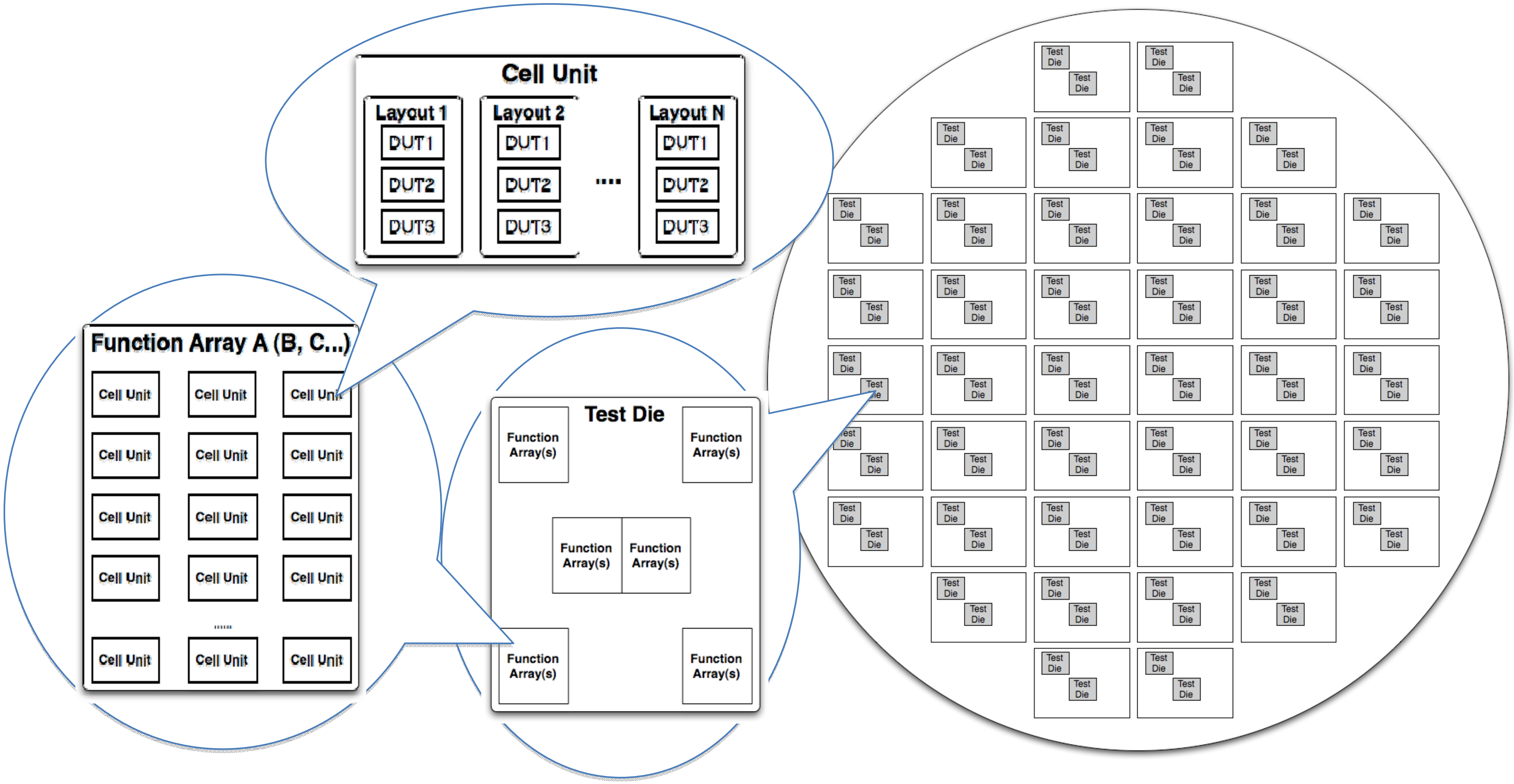


Variation-Aware Model Extraction

- Extracted parameters will have both deterministic and random components, as well as spatial hierarchy
  - Eliminate assumption of Normal dist.
- Extraction of statistical moments and spatial characteristics done *simultaneously* over a number of sample within the chip and across the wafer
  - Captures the real variation at all levels
- Model accuracy is being verified on 45nm and 32nm test chips (transistors, logic and memory devices)



Optimal Sampling for Spatial & Layout Variability



Outline

- Background
- Approaches
  - Global Empirical Model (Hierarchical / Spatial)
    - Some interesting artifacts – "spatial correlation"
  - Wafer-to-wafer systematic variability
  - LER modeling and impact assessment
  - Entering the design flow
- Future

On-demand custom variability "views"

Data (metology and simulation) → Complete & parsimonious Hierarchical / Hybrid Model

Model Estimator	Meaning
$\hat{\eta} = \bar{p}_{....}$	Global Mean
$\hat{\lambda}_i = \bar{p}_{i...} - \bar{p}_{....}$	Lot Factor
$\hat{\sigma}_j = \bar{p}_{.j..} - \bar{p}_{....}$	Wafer or Slot Factor
$\hat{\rho}_{ij} = \bar{p}_{ij..} - \bar{p}_{i...} - \bar{p}_{.j..} + \bar{p}_{....}$	Lot-Wafer Interaction Factor
$\hat{\beta}_k = \bar{p}_{..k.} - \bar{p}_{....}$	Average Wafer
$\hat{\omega}_{ijk} = \bar{p}_{ijk.} - \bar{p}_{ij..} - \bar{p}_{..k.} + \bar{p}_{....}$	Deviation from Average Wafer
$\hat{\gamma}_l = \bar{p}_{...l} - \bar{p}_{....}$	Average Die
$\hat{\tau}_{kl} = \bar{p}_{..kl} - \bar{p}_{..k.} - \bar{p}_{...l} + \bar{p}_{....}$	Die-Site Interaction Factor
$\hat{\epsilon}_{ijkl} = p_{ijkl} - \bar{p}_{ijk.} + \bar{p}_{..k.} - \bar{p}_{..kl}$	Residual

→ Circuit Simulation (physical process corners)

→ Statistical Timing Analysis (die-level, apparent "spatial" correlation)

→ Parametric Yield Targeting ("total" variability)

→ Process Fingerprinting (Fault diagnosis through clustering)

...

Of Further Interest

- What about Statistical Circuit Simulation?
  - Propagating Gaussian and Mixture of Gaussian (MOG) distributions through interval representation
- What about temporal non-stationarity?
  - Can be modeled or "collapsed" depending on the needed "view"
- What about SRAM variability?
  - Nothing special other than we really must capture extreme tails of distribution extremely well (see above)
- What about novel devices (CNTs, etc)?
  - Blending a Hybrid/Hierarchical model of CMOS "backbone" with *ab initio* statistical simulation of novel devices

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