Variability and Design of SRAM in Scaled and Emerging Technologies

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Outline

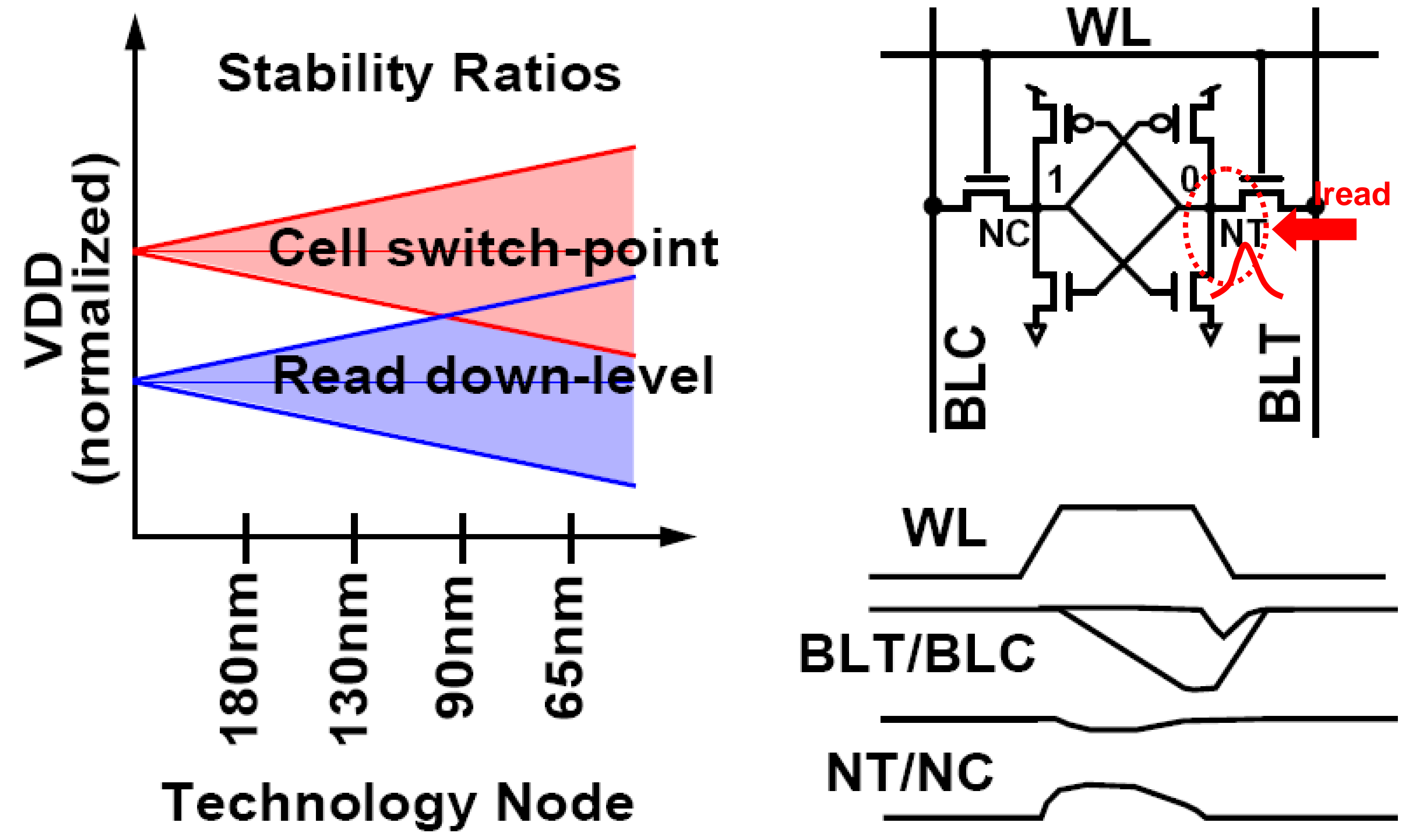
Part-1: Prof. Ching-Te Chuang

- SRAM Design Challenges
- 6T SRAM Cell and Circuit Techniques
- Alternative SRAM Cells & Low-Voltage Operation

Part-2: Prof. Pin Su

- FinFET vs. Bulk SRAM
- Analytical FinFET/UTBSOI Subthreshold SRAM Framework
- SNM of FinFET 6T SRAM Cells
- Impact of Surface Orientation

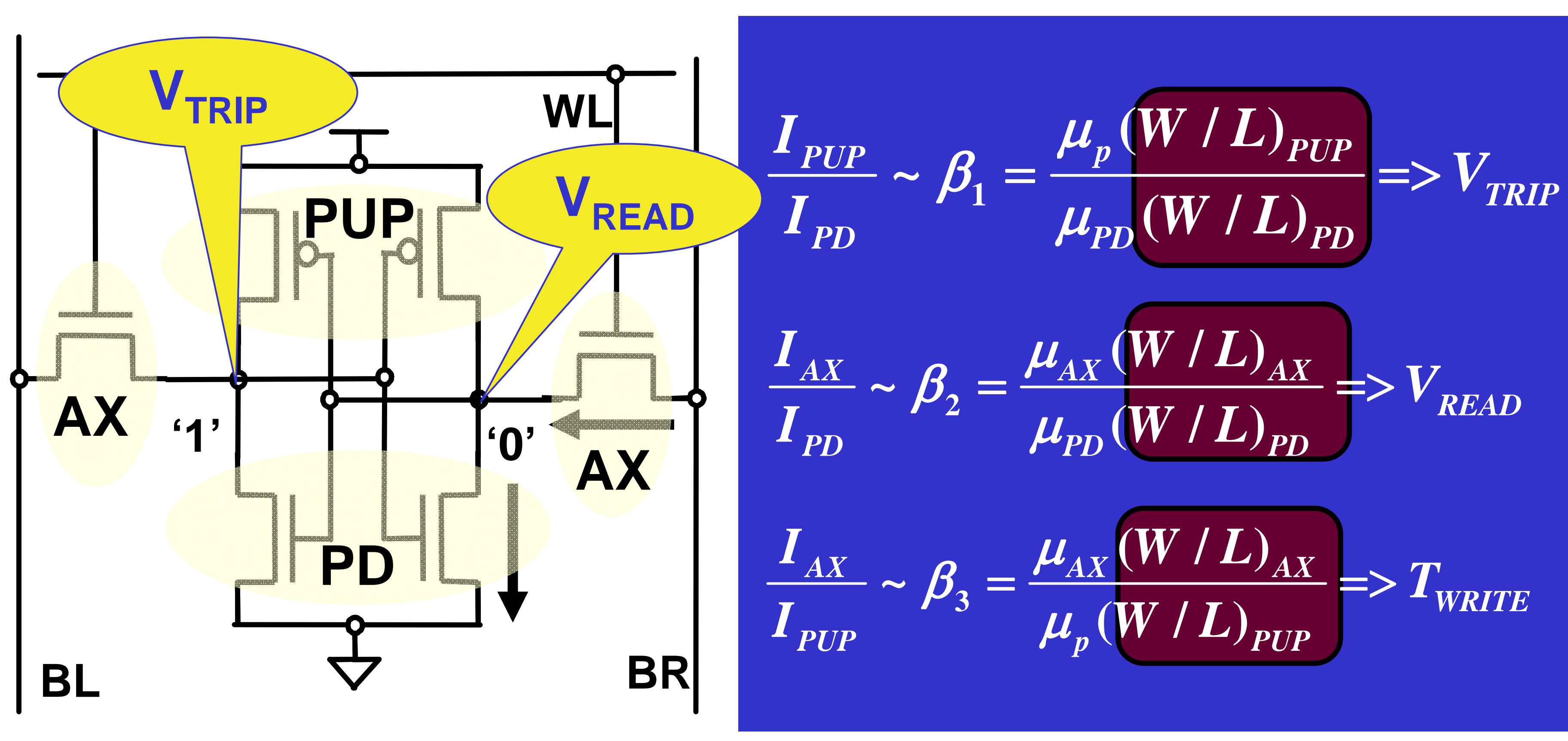
Scaling, Read Disturb & Cell Stability Margin



(H. Pilo, ISSCC, 2005)

Conflicting Read/Write Requirements

- To facilitate Read and minimize Read-disturb (V_{READ})
  - ➔ Strong PD NMOS and weak AX NMOS (small β_2)
- To improve Writability (Write margin)
  - ➔ Strong AX NMOS and weak PUP PMOS (large β_3)



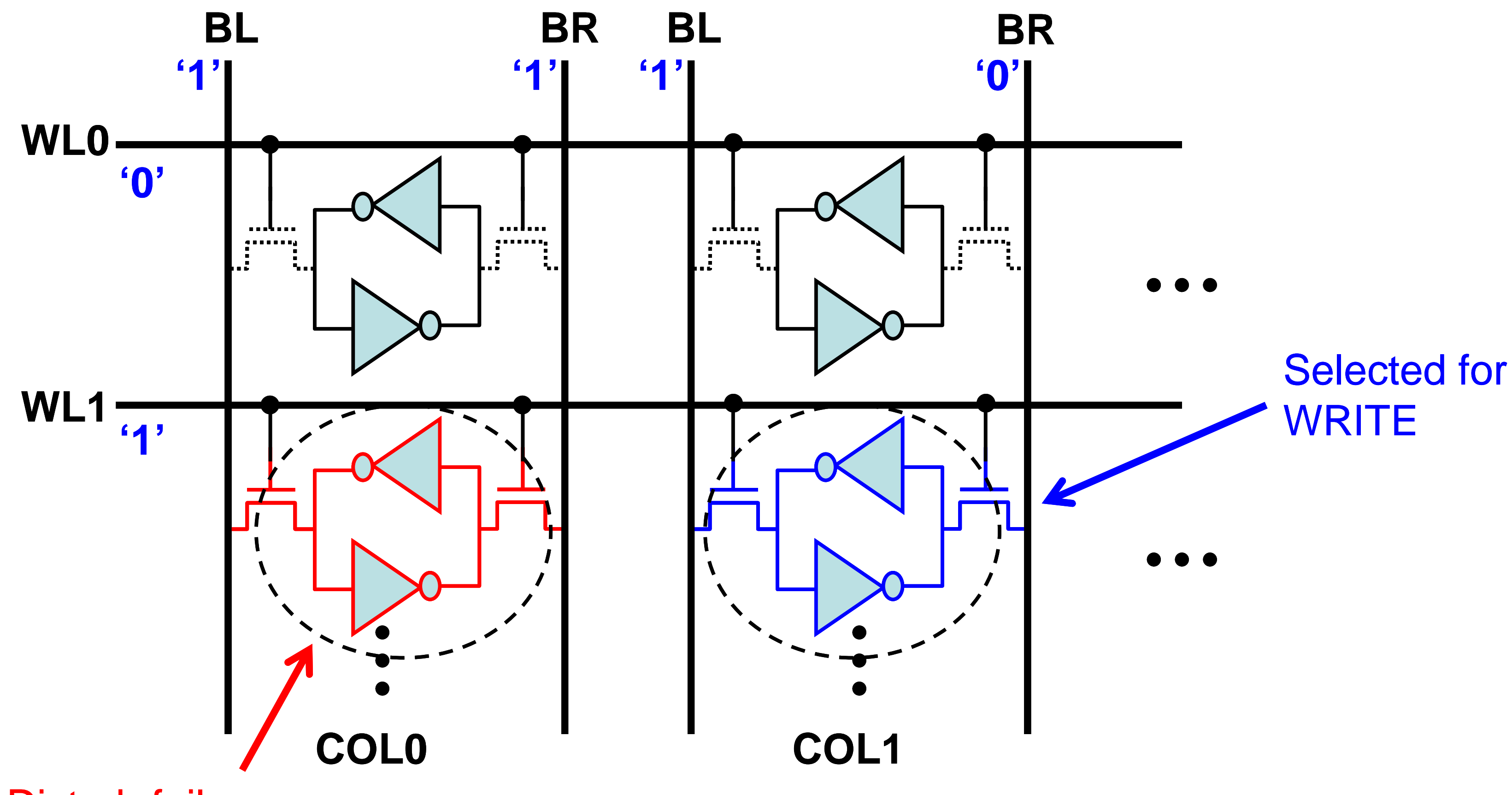
$$\frac{I_{PUP}}{I_{PD}} \sim \beta_1 = \frac{\mu_p (W/L)_{PUP}}{\mu_{PD} (W/L)_{PD}} \Rightarrow V_{TRIP}$$

$$\frac{I_{AX}}{I_{PD}} \sim \beta_2 = \frac{\mu_{AX} (W/L)_{AX}}{\mu_{PD} (W/L)_{PD}} \Rightarrow V_{READ}$$

$$\frac{I_{AX}}{I_{PUP}} \sim \beta_3 = \frac{\mu_{AX} (W/L)_{AX}}{\mu_p (W/L)_{PUP}} \Rightarrow T_{WRITE}$$

Half-Select Disturb

- During a Read or Write operation, half-selected cells on the selected word-line are actually experiencing “Read” operation
  - ➔ Disturb similar to Read-disturb

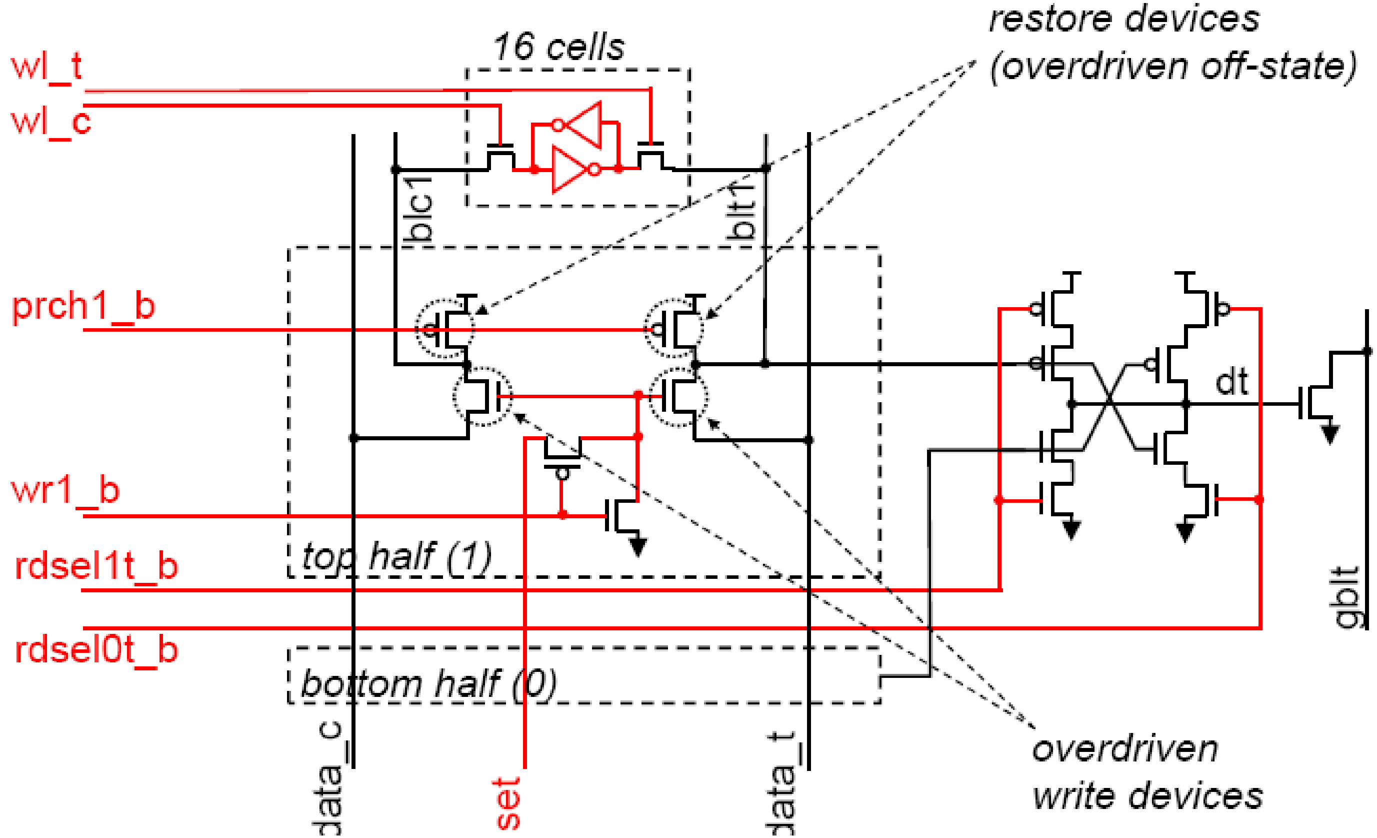


6T SRAM Cell and Circuit Techniques

- Thin cell layout
- Hierarchical bit-lines with short local bit-lines
- Dual supply
- Large signal domino-like sensing
- Unclamped or weakly-clamped local bit-lines
- Power-gating with header/footer
- Adaptive Read/Write supply
  - ➔ Dynamic Read/Write supply
  - ➔ Floating power-line Write
  - ➔ Capacitive coupling
- Read-assist and Write-assist circuits
  - ➔ Suppressed Wordl-Line
  - ➔ Negative Bit-Line
  - ➔ Self-Adjust/Repair
- Exploit device structure (e.g. Asymmetrical Transistor)

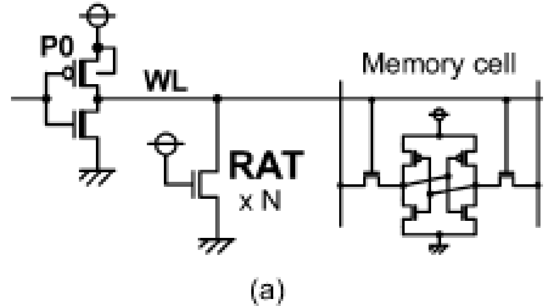
Example: IBM Power7^{TM} Dcache

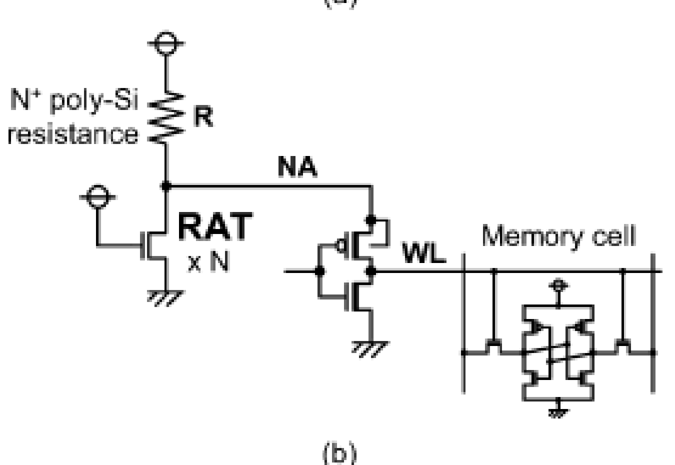
- Dual supply
- Hierarchical bit-lines with short local bit-lines
- Unclamped local bit-lines
- Large signal domino-like sensing

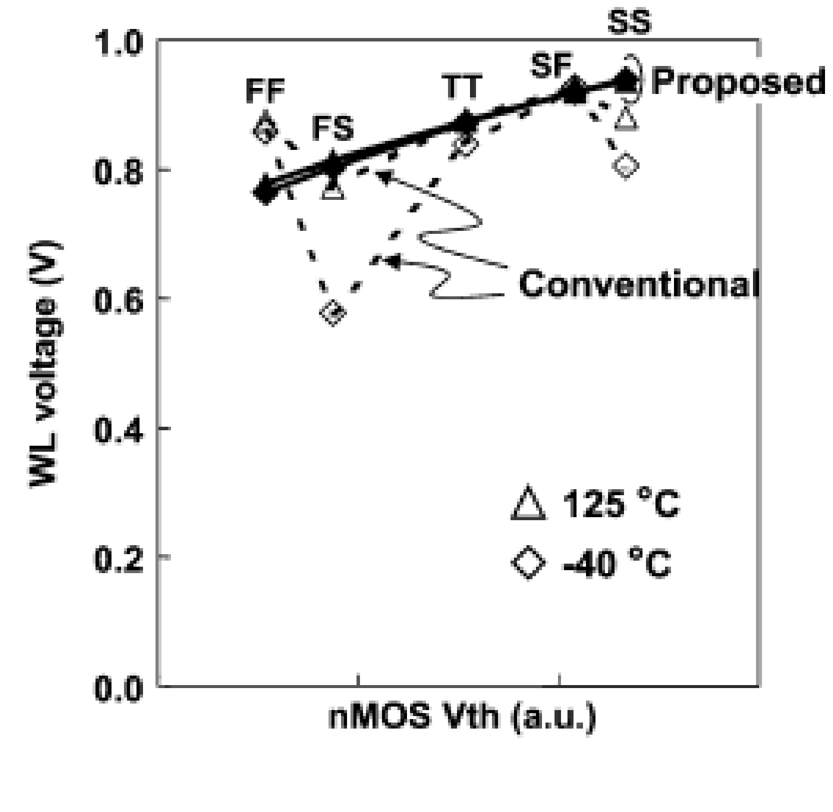


(J. Pille et al., ISSCC, 2010)

Suppressed Word-Line: 1



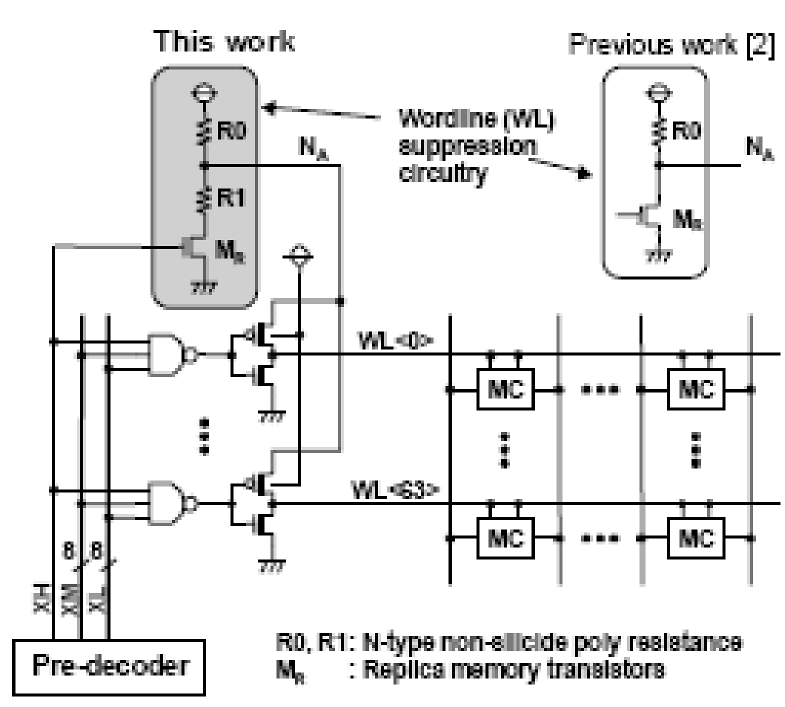


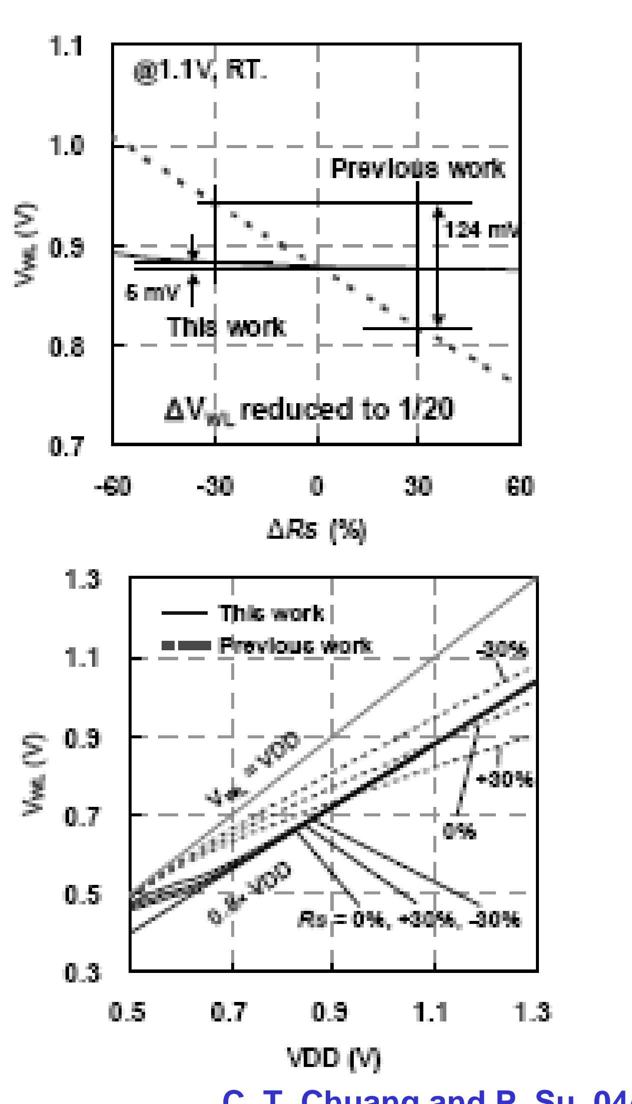


(K. Nii et al., ISSC, 01/2008)

Suppressed Word-Line: 2

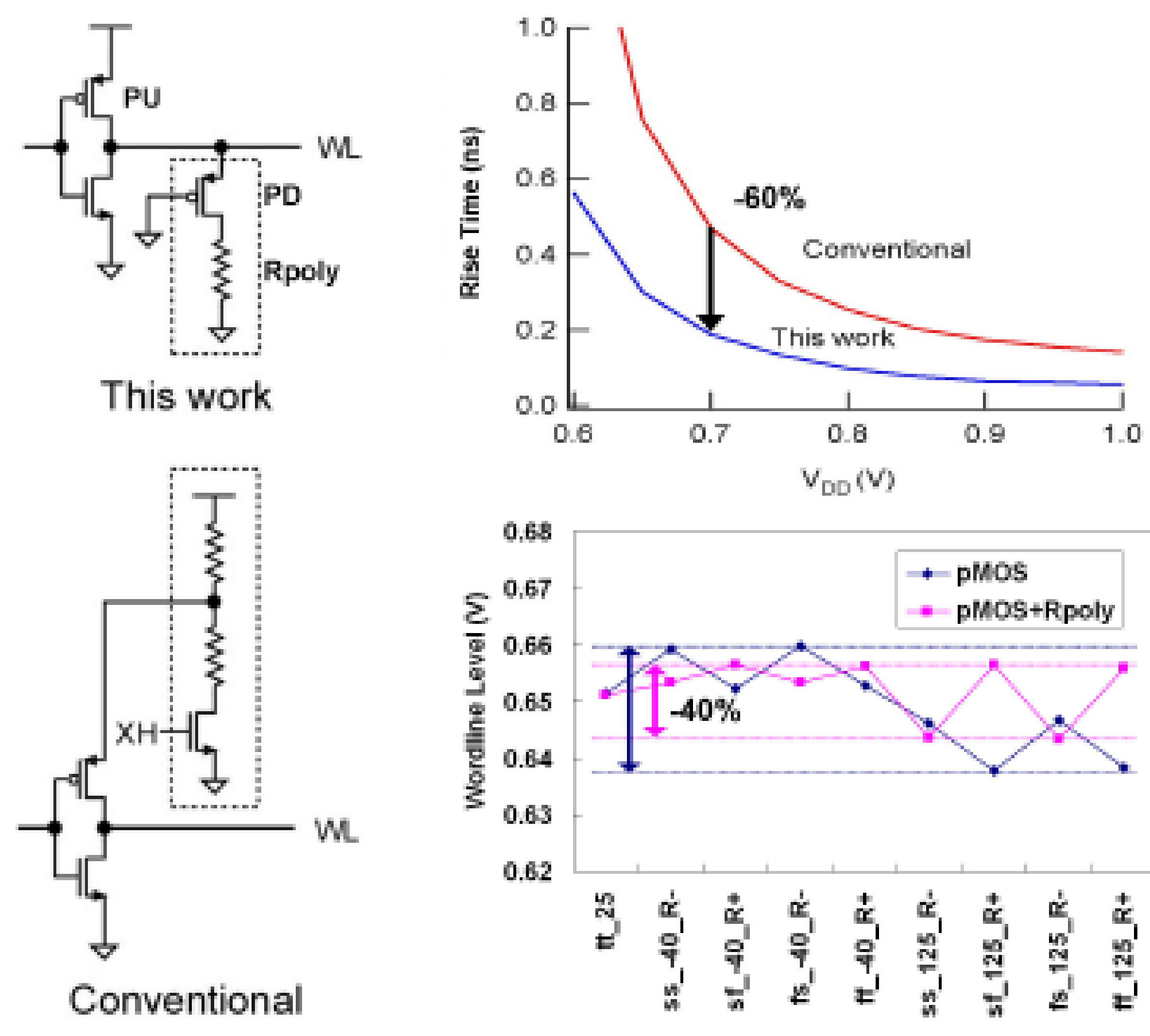
- Split-R to mitigate sheet resistance variation





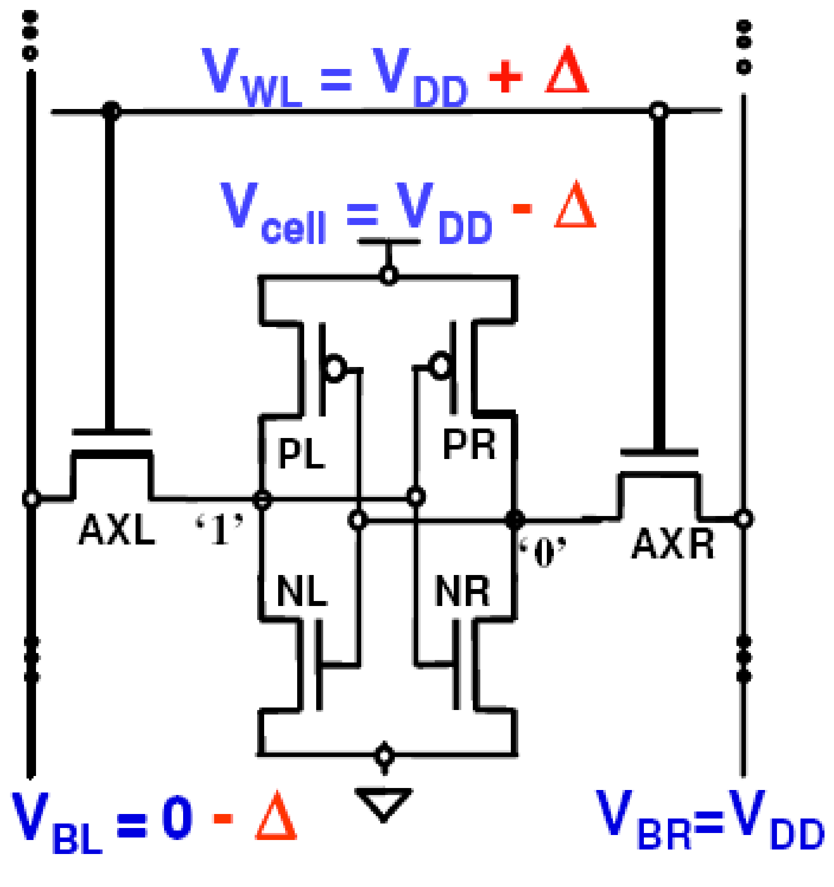
(K. Nii et al., Symp. VLSI Circuits., 2008)

Suppressed Word-Line: 3



(Y.Fujimura et al.,ISSCC, 2010)

Methods for Reducing Write Failure

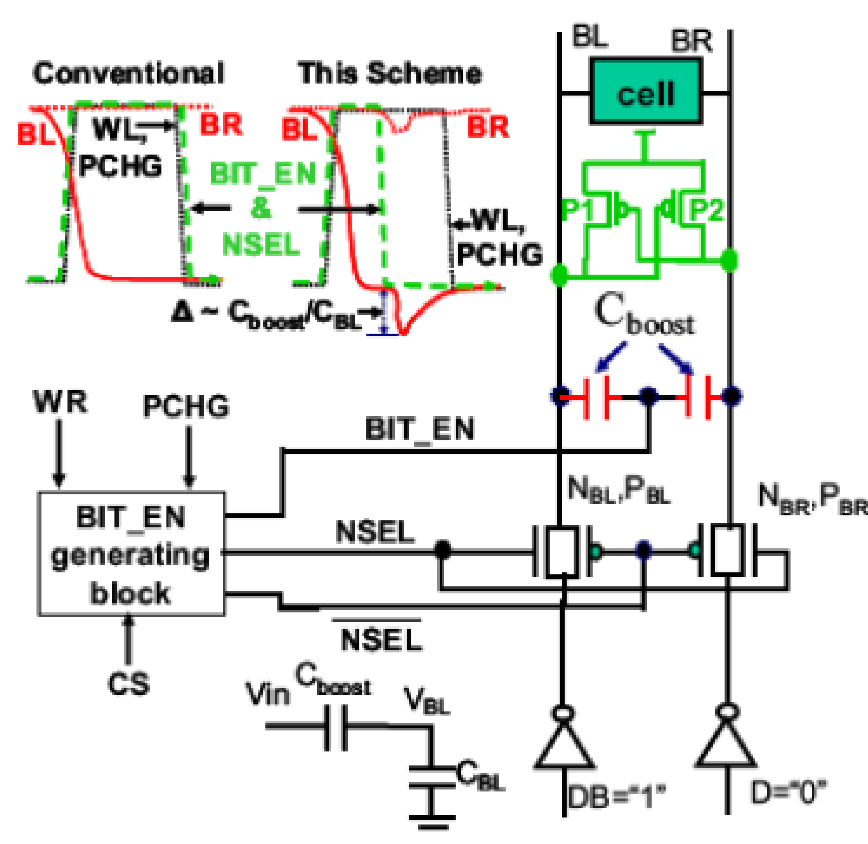


- Higher WL voltage
  - + Stronger access (AXL & AXR)
  - – Half-select disturb
- Lower cell supply (V_{cell})
  - + Weaker pull-up (PL)
  - – Weaker latch effect (weaker PR)
- Negative bit-line voltage
  - + Stronger access (AXL)
  - + Latch strength is same

(S. Mukhopadhyay et al., ISCAS, 2008)

Transient Negative Bit-Line: 1

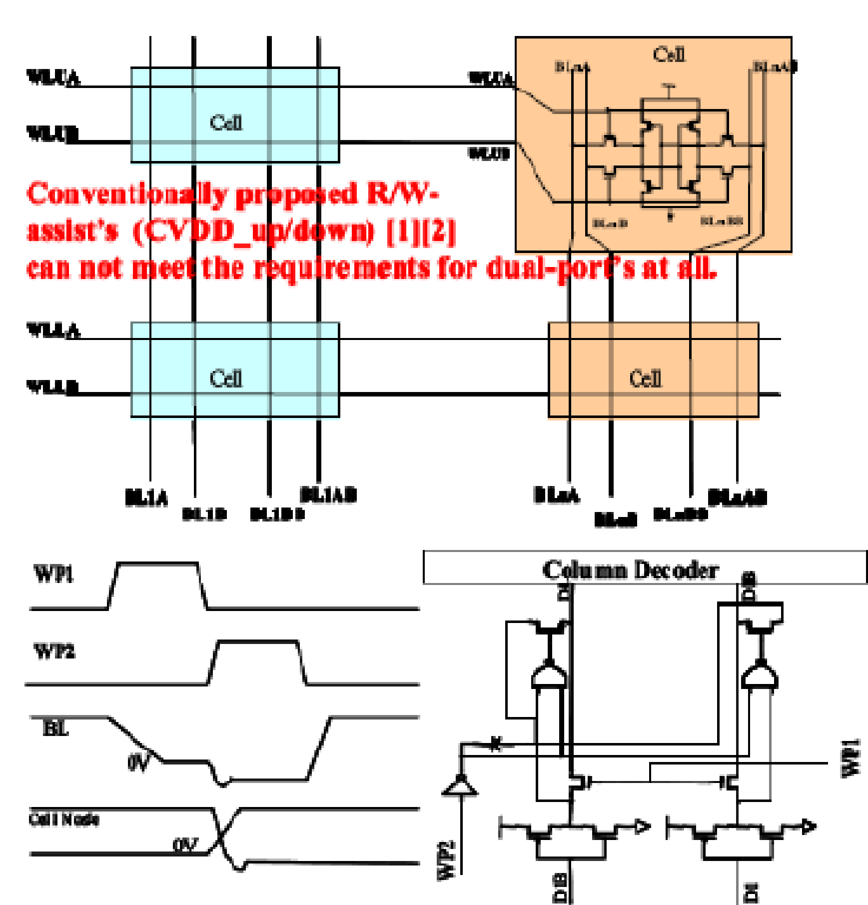
- Two boosting capacitors connected directly to each and every BL pair
- Negative pulse also coupled into the BL that held at "High"
- Cross-coupled P1 & P2 provide a push-pull to reduce the disturbance
- NBL timing subject to PVT variation and V_T scatter



[1] S. Mukhopadhyay, R. Rao, J. J. Kim, and C. T. Chuang, "Capacitive Coupling Based Transient Negative Bit-line Voltage (Tran-NBL) Scheme for Improving Write-ability of SRAM Design in Nanoscale Technologies," Proc. IEEE International Symposium on Circuits and Systems (ISCAS), Seattle, Washington, May 18-21, 2008, pp. 384-387.

Transient Negative Bit-Line: 2

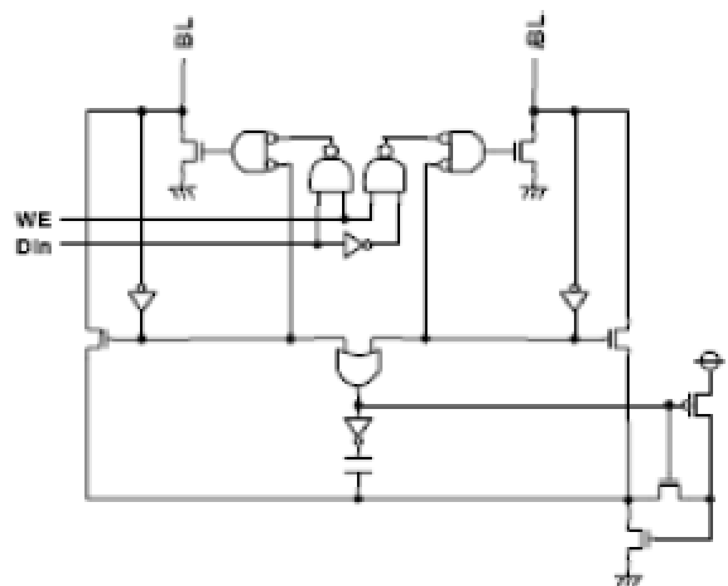
- Single boosting capacitor shared by BL pair
- DI determines the transient negative pulse passed to BL or BLB
- Timing of the negative pulse is derived with delay chains and several control signals
- NBL timing subject to PVT variation and V_T scatter



(D. P. Wang et al., Int'l SOC Conf., 2007)

Transient Negative Bit-Line: 3

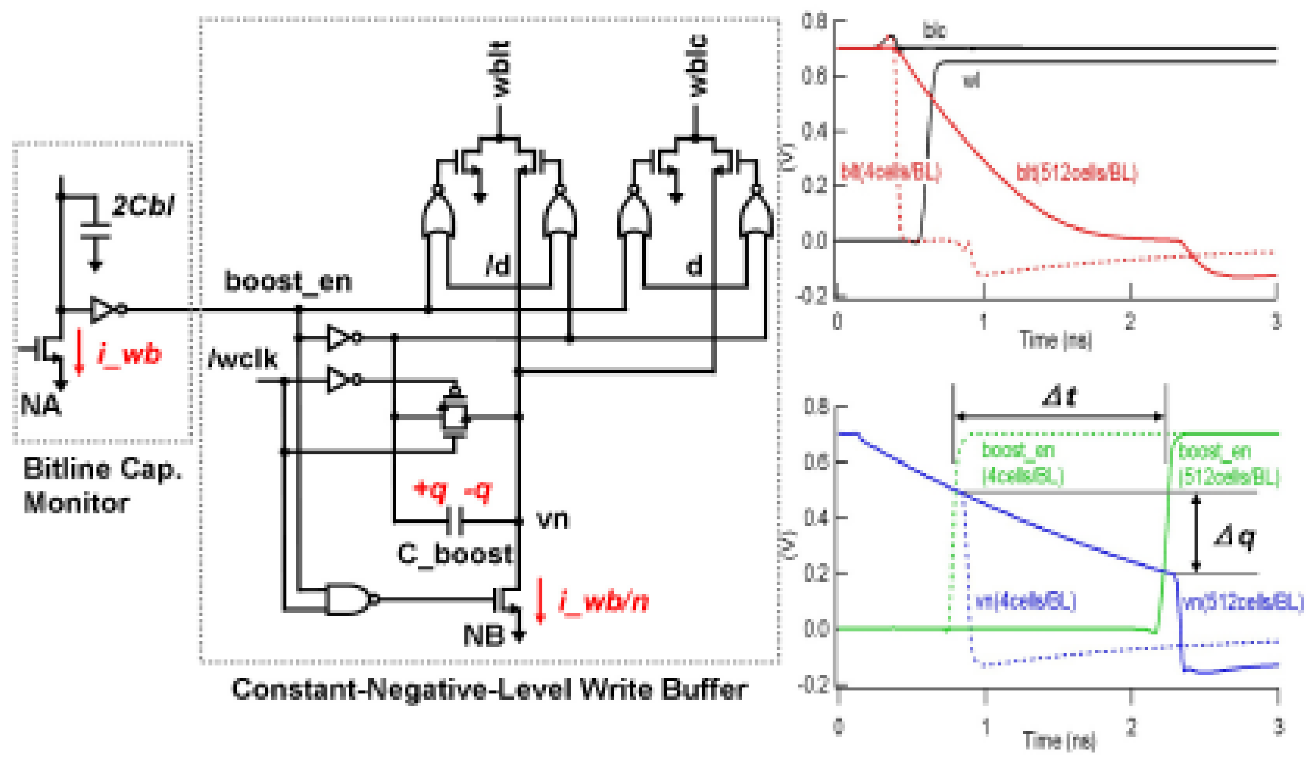
- Transient NBL action initiated by low-going BL
- Timing of NBL pulse much more tolerant to variation
- Extra inverter needed for each and every BL
- Device count and area overhead



(K. Nii et al., Symp. VLSI Circuits., 2008)

Transient Negative Bit-Line: 4

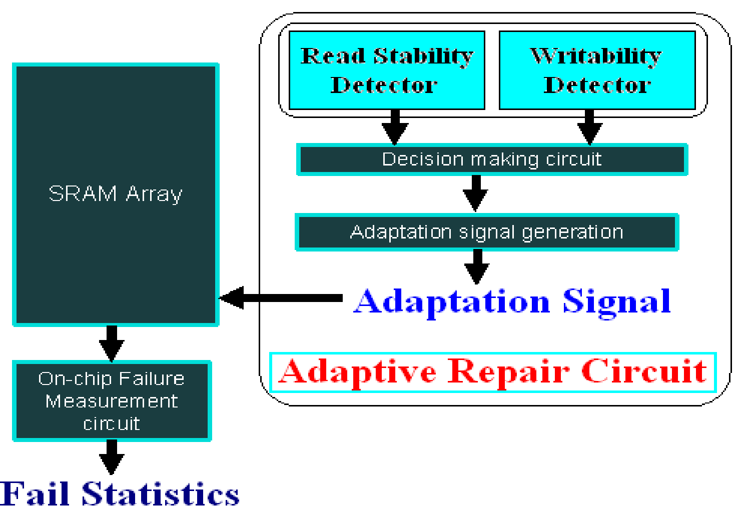
- **Bit-line capacitance monitor tracks BL discharging time and controls the amount of charges stored in boosting capacitor**
- **Constant NBL level for SRAM compiler applications**

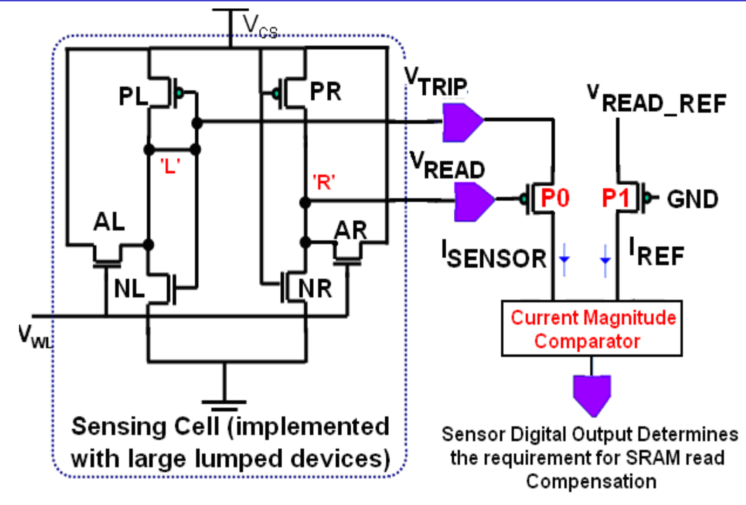


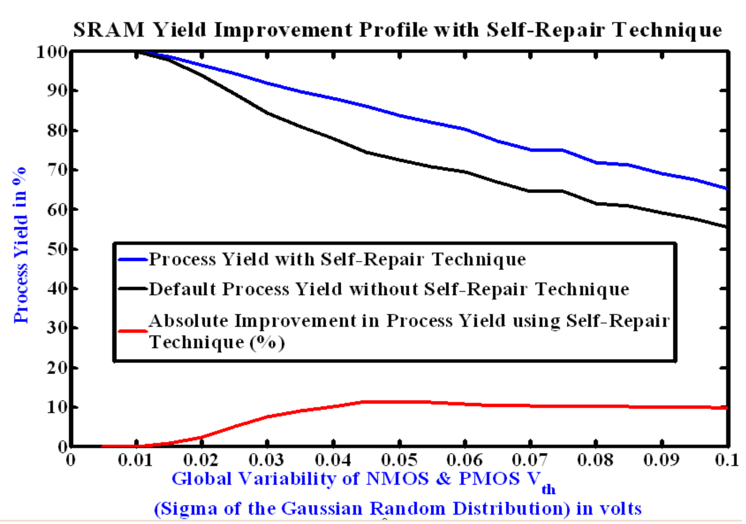
$\Delta q = \Delta t * i_wb/n = (\Delta Cbl * Vdd / i_wb) * (i_wb/n) \propto \Delta Cbl$

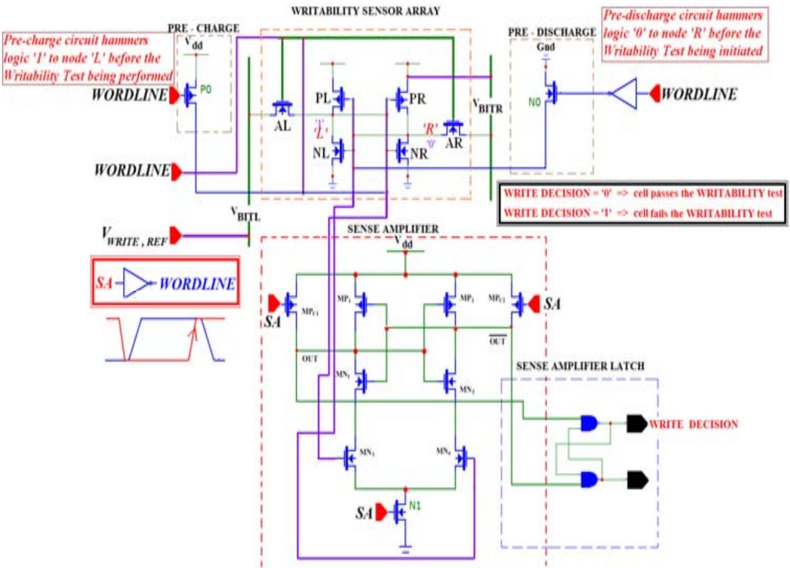
(Y.Fujimura et al.,ISSCC, 2010)

Self-Adjust/Repair SRAM



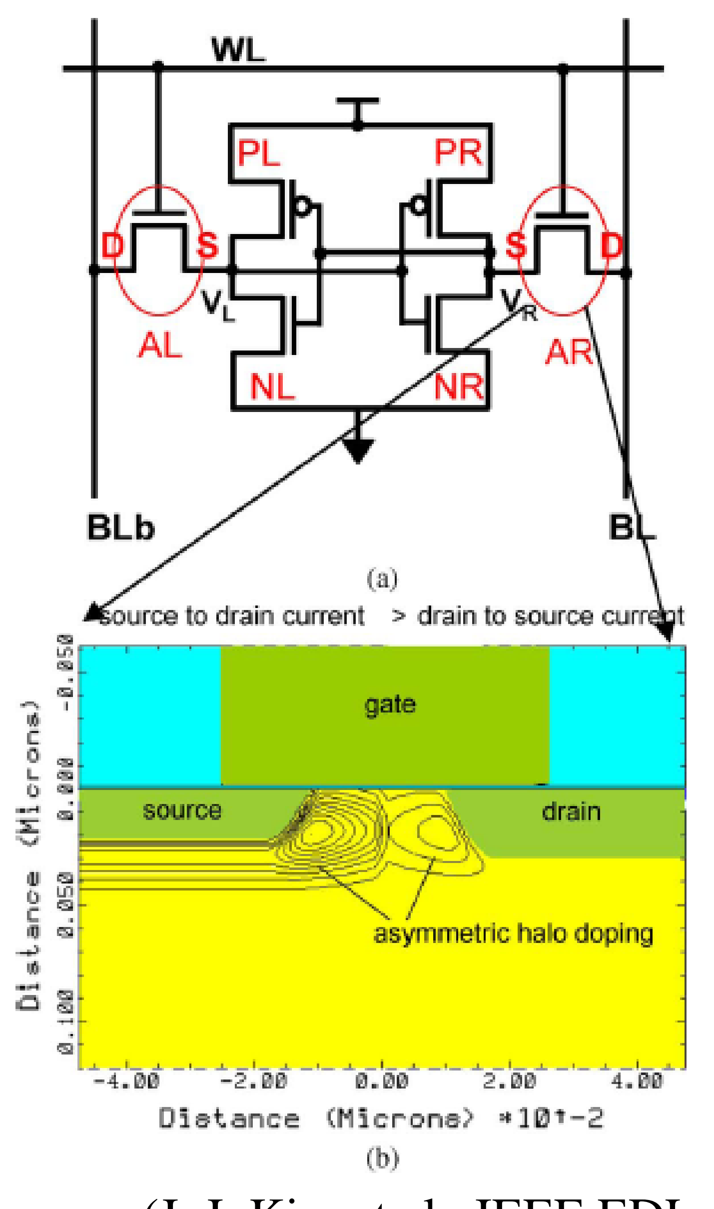






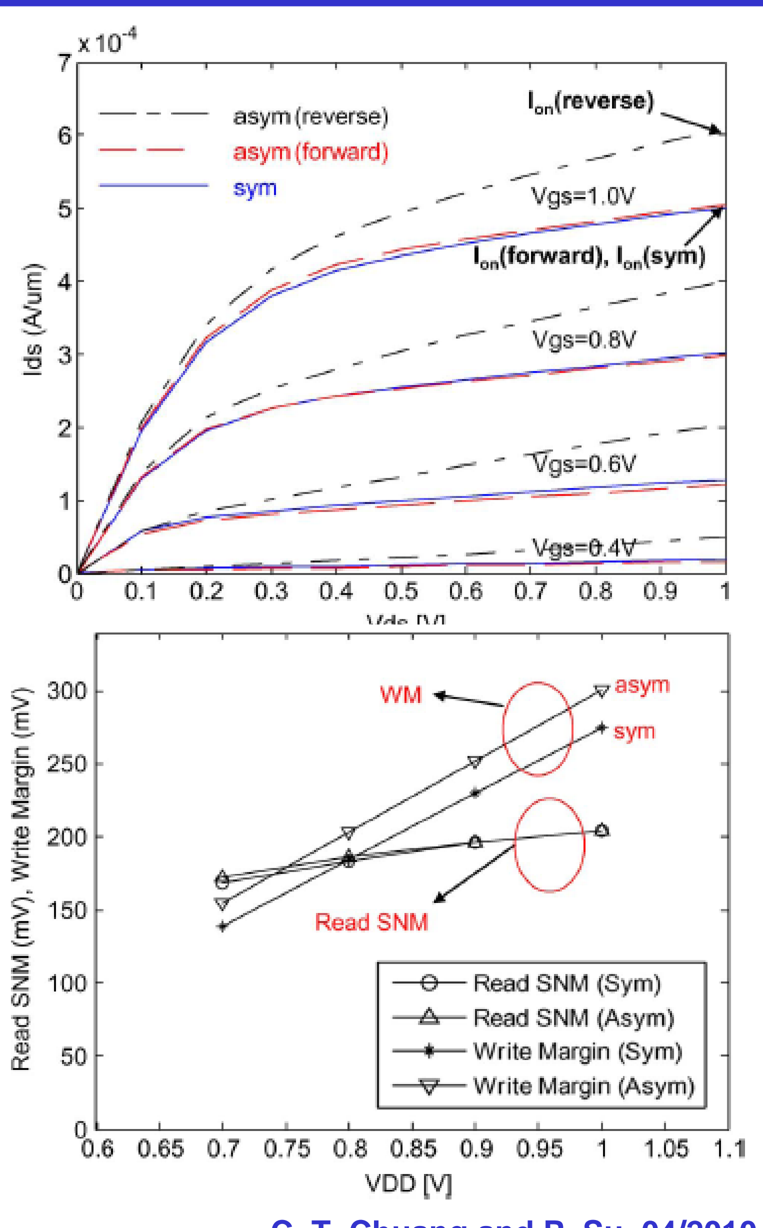
(N. Mojumder et al., VLSI Test Symp., 04/2008 & IEEE T-VLSI, 01/2010)

Asymmetrical Transistor in 6T SRAM: 1



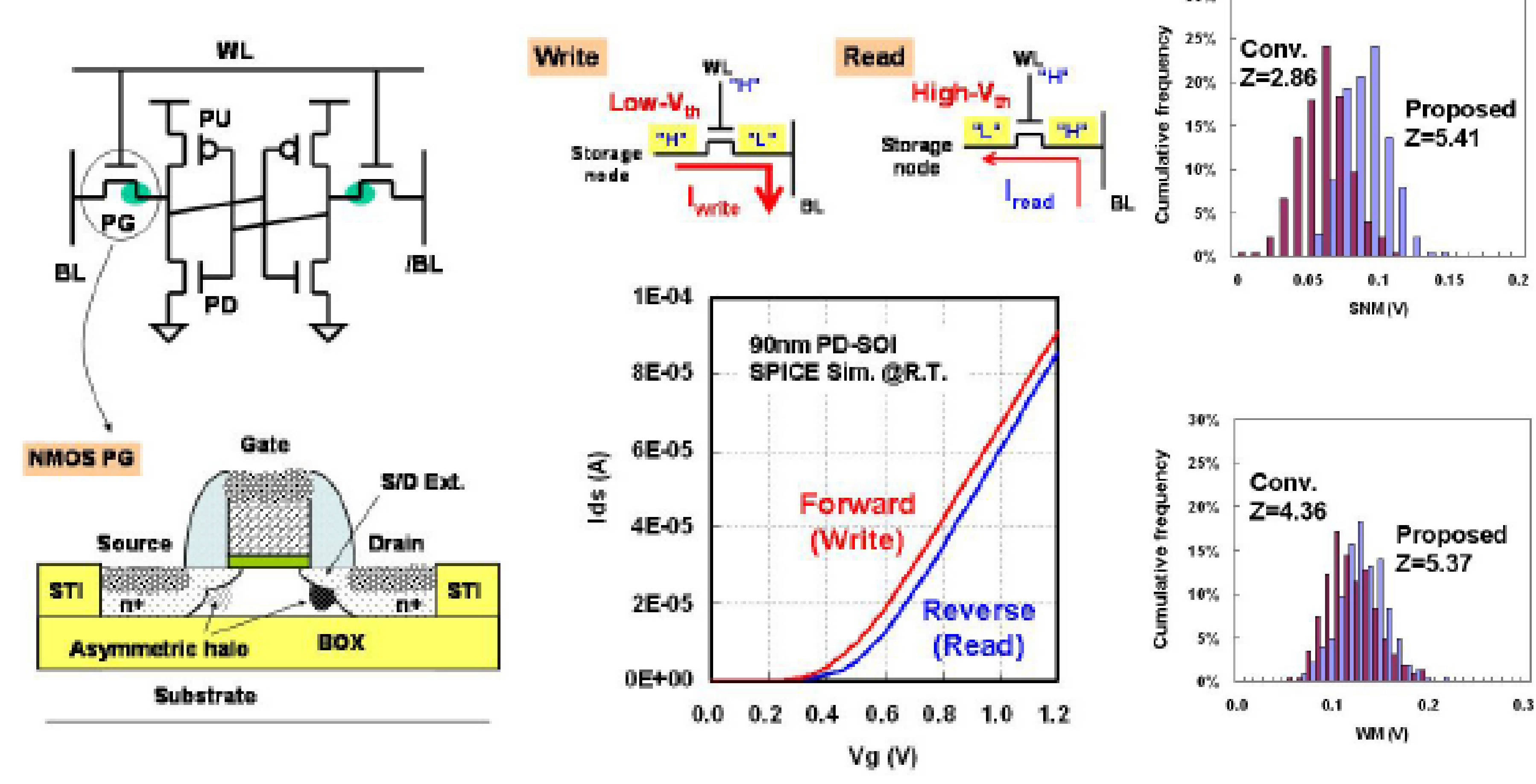
(a)

(b)



(J. J. Kim et al., IEEE EDL, 08/2009)

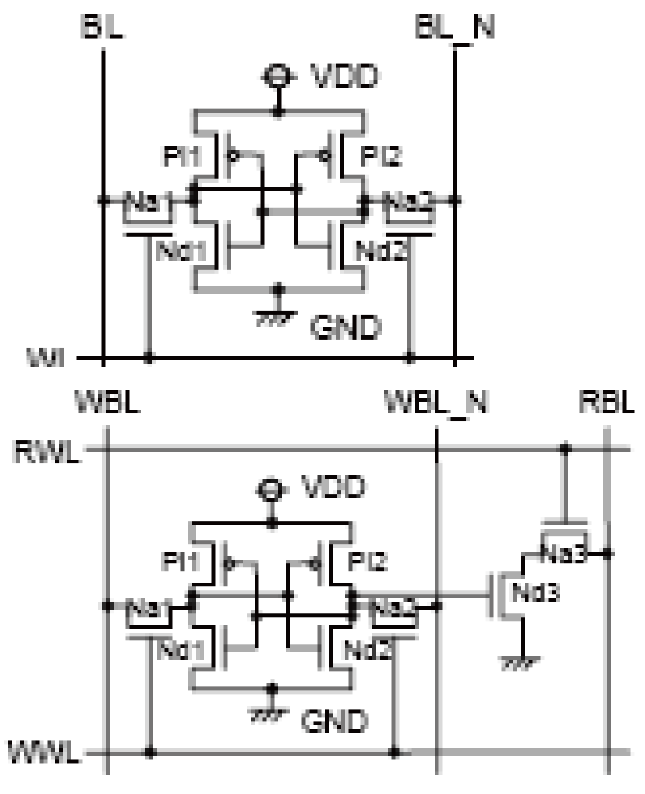
Asymmetrical Transistor in 6T SRAM: 2

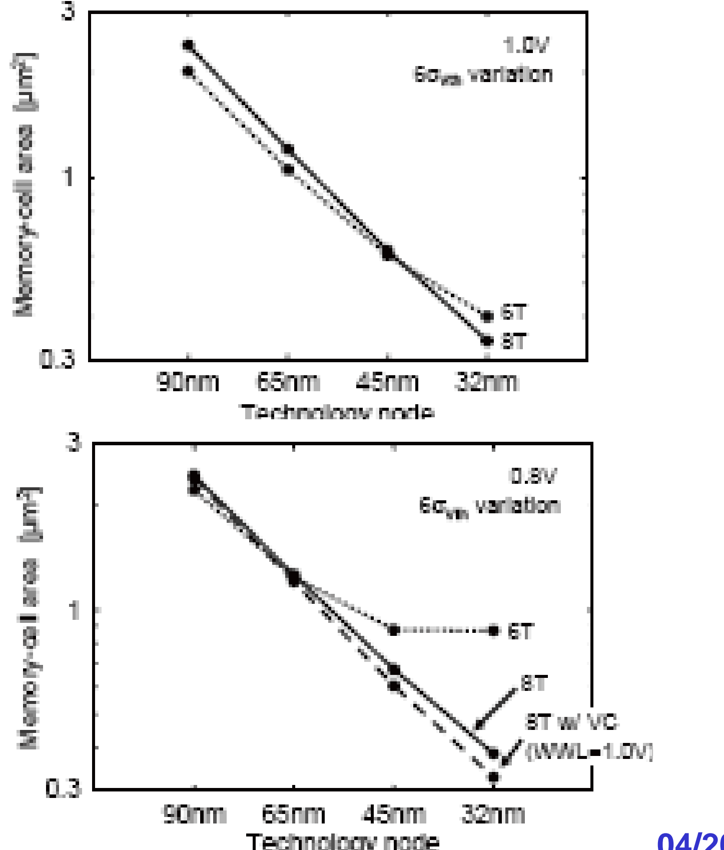


(K. Nii et al et al., ISSCC, 2010)

6T vs 8T SRAM: Cell Size Scaling

- 6T cell: Conflicting Read/Write margin requirements
  - ➔ Read: Large pull-down NMOS cell Tx & large β ratio (pull-down/access width ratio)
  - ➔ Write: large access pass-Tx
- 8T cell: Pull-down NMOS cell Tx can be reduced w/o degrading Read margin
  - ➔ Dynamic voltage control enables further scaling
    - ◆ V_a for memory cell, V_{max} for WWL and RWL
    - ◆ 64 Mb 8T SRAM with V_{min} = 0.42 V in 90 nm CMOS

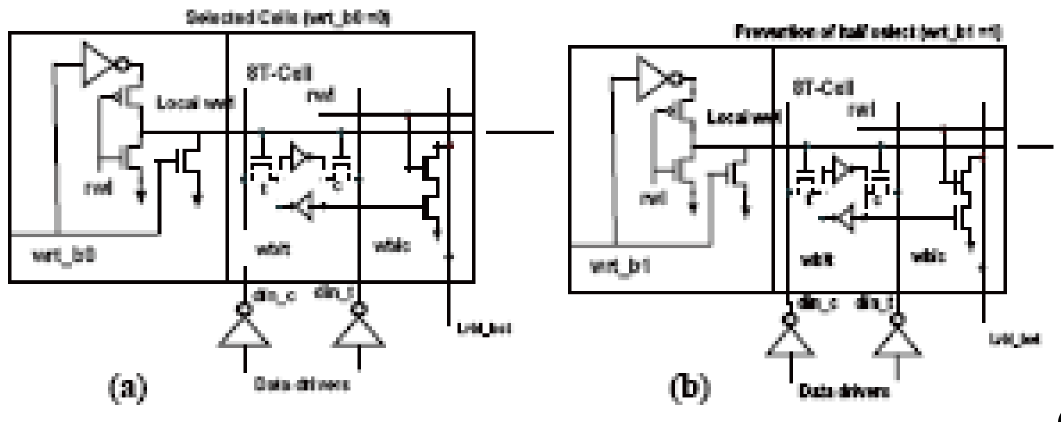




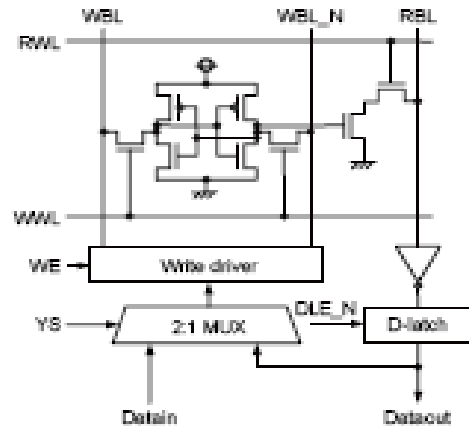
(Y. Morita et al., Symp VLSI Circuits, 2007)

8T SRAM: Half-Select Disturb during Write

- During Write, half-selected cells on the same wordline still experience storage node disturb similar to "Read" disturb in 6T SRAM
  - ➔ Especially worse for dual supply SRAM with V_{MAX} applied to WWL
- Array architecture approach (L. Chang et al., Symp. VLSI Circuits, 2007)
  - ➔ No column select. Floorplan such that all bits in a word are spatial adjacent
  - ➔ Constraint: Bits from different words can not be physically interleaved
  - ➔ 5.3 GHz, 0.41 V V_{min}, 32Kb subarray in 65 nm PD/SOI
- Gated Write wordline signal (Byte Write)
  - ➔ Local Write wordline "on" only for the selected block
  - ➔ 6.6+ GHz, 0.4 V V_{min}, dual-supply, 1.2 Mb SRAM in 65 nm PD/SOI
- Write-back scheme
  - ➔ RWL activated even during Write, all cell data in selected WL read out to D-latches
  - ➔ Dataout is then written back to half-selected cells
  - ➔ 0.42 V V_{min}, 64 Mb SRAM in 90 nm CMOS



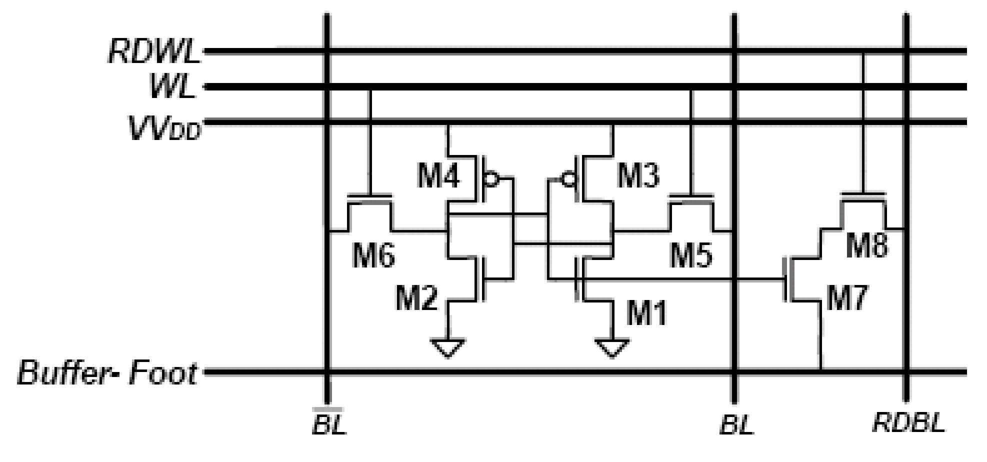
(R. Joshi et al., Symp VLSI Circuits, 2007)

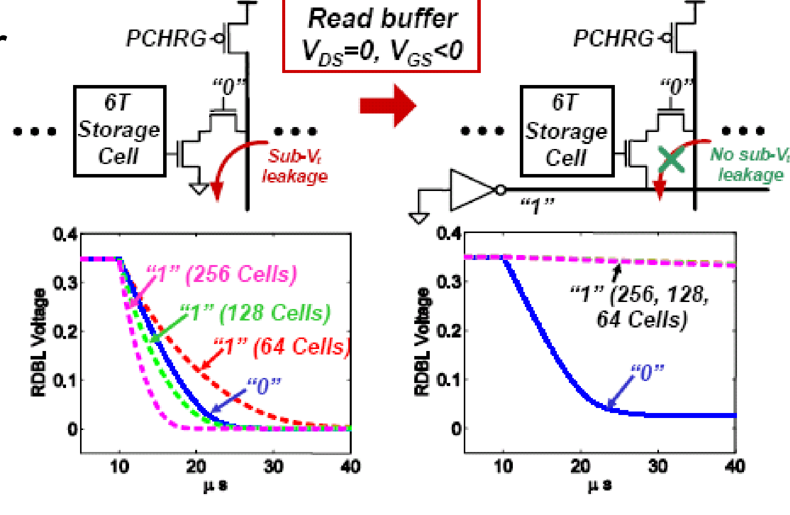


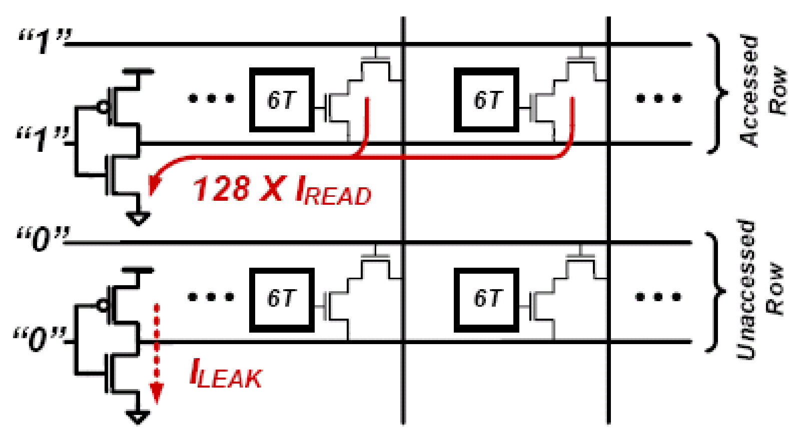
(Y. Morita et al., Symp VLSI Circuits, 2007)

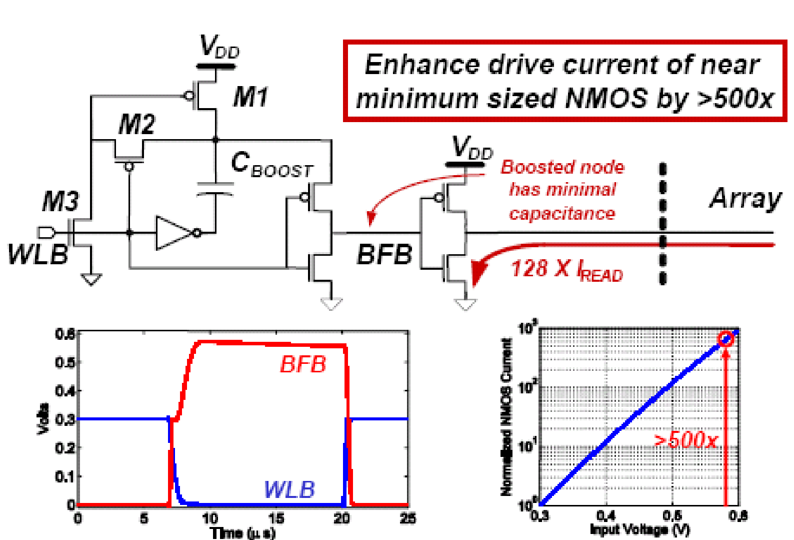
Sub-V_T 8T SRAM

- 256Kb, 65 nm CMOS, 25kHz, 2.83/3.96 μW (Read/Write)@ V_{min} = 0.35V
- Buffer-foot with gate-boosted foot driver





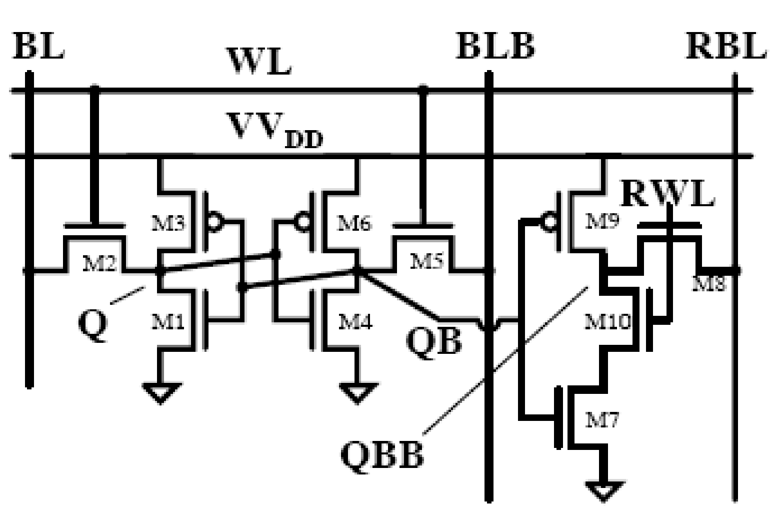


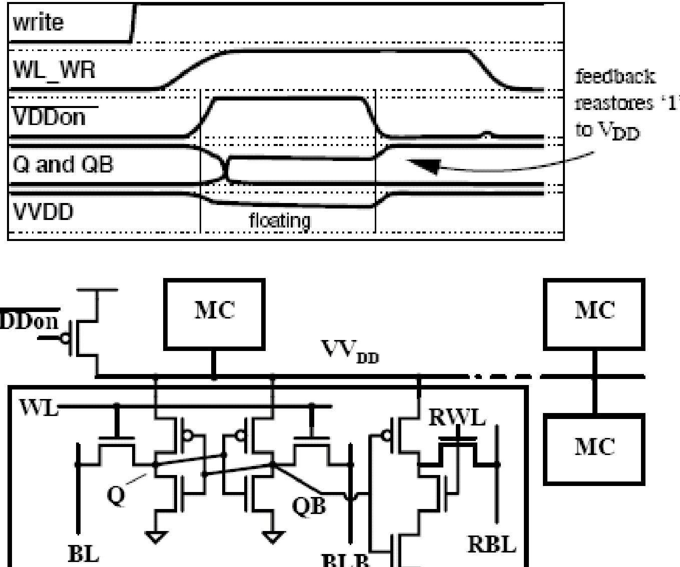


(N. Verma and A. P. Chandrakasan, ISSCC, 2007)

256Kb 10T Sub-V_T SRAM in 65nm CMOS

- Enable sub-V_T Read/Write by lowering leakage from unaccessed cells
  - ➔ For QB='0', Ileak across top RWL NFET ~ 0
  - ➔ For QB='1' Ileak across top RWL NFET ~ 0 with negative VGS
- Floating VV_{DD} while boosting WWL by ~ 50-80mV improves V divider 10X, making cell Writable at 0.3V (WL and Write driver operated at 100 mV above V_{DD}; Write is much easier in Sub-V_T with exponential dependency of V divider)
- 475 KHz, 3.28 μW @ V_{DD} = 0.4V
- Leakage reduction
  - ➔ 0.6V -> 0.4V: 2.5X ; 0.6V -> 0.3V: 3.8X ; 1.2V -> 0.3V: 60X

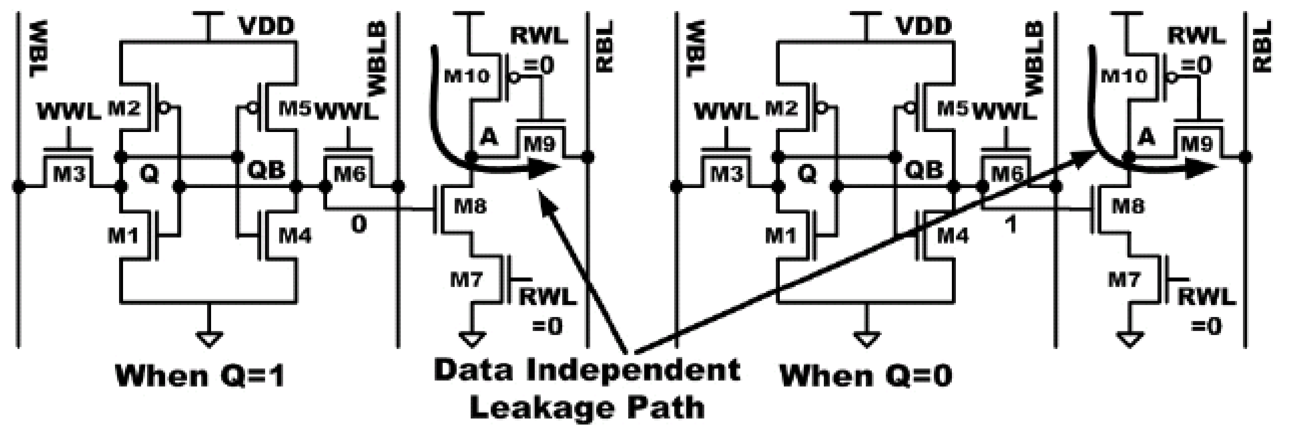




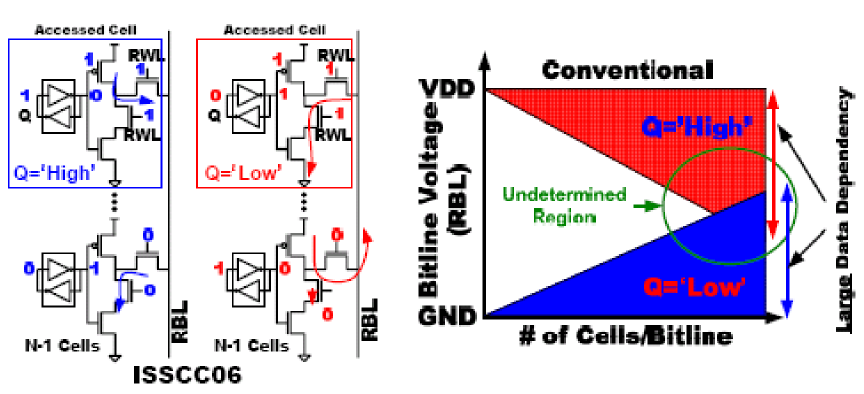
(B. H. Calhoun and A. Chandrakasan, ISSCC, 2006)

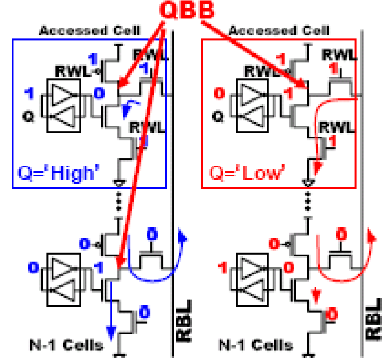
Sub-V_T SRAM w. Data-Independent BL Leakage

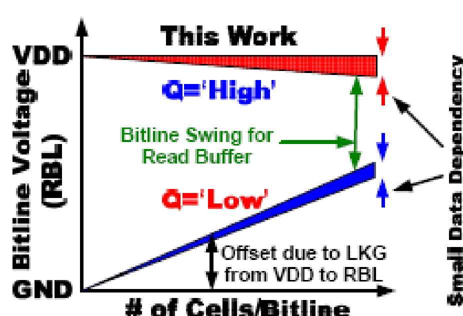
- 480 Kb: 120 KHz, 10.2 μA @ 0.2V in 130 nm CMOS
- Data-independent bit-line leakage



Proposed SRAM Cell & Bitline Leakage Path







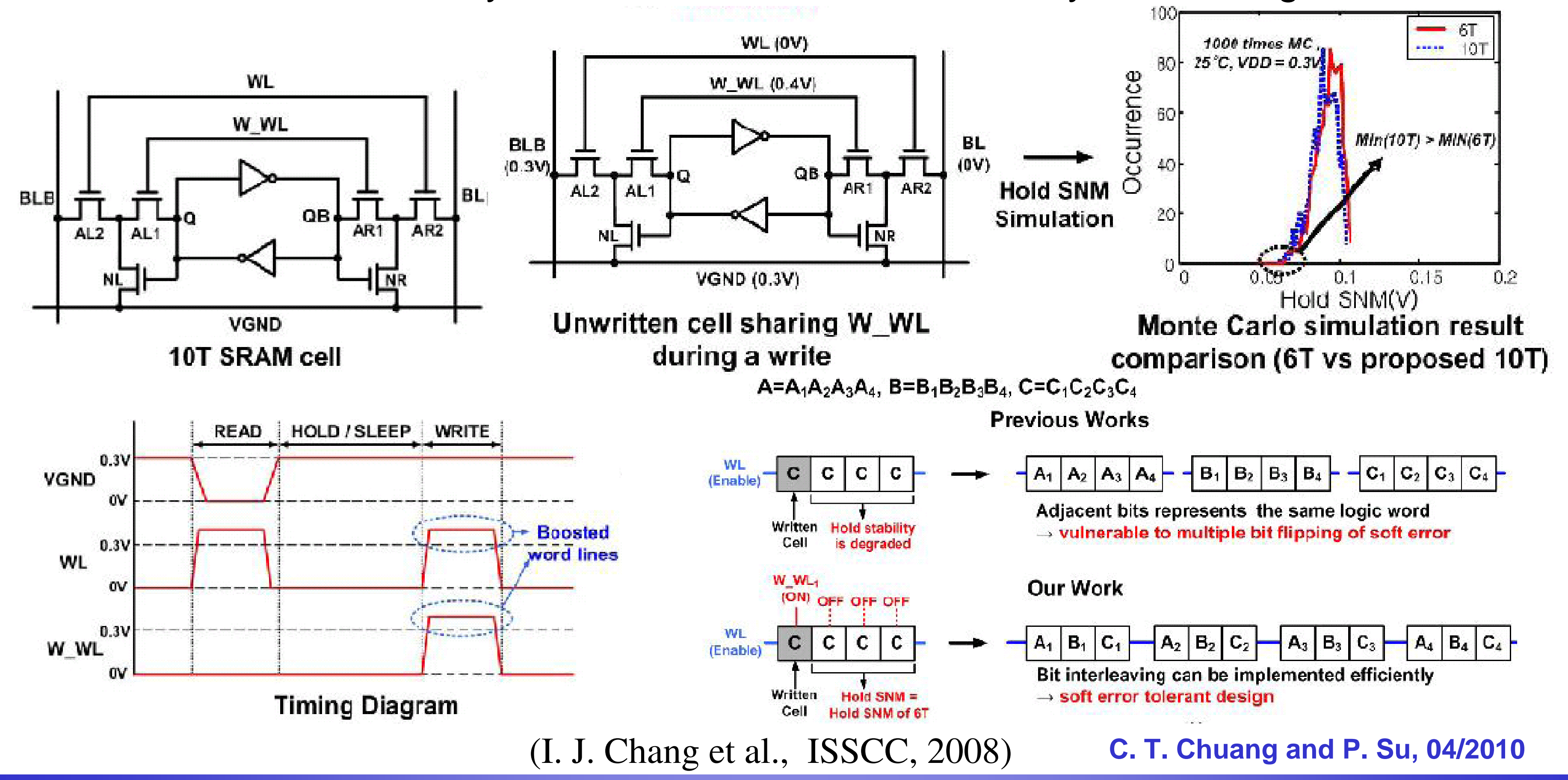
- Undetermined region due to data-dependency
- Possible read failure using single threshold read buffer

- Bitline logic high and low levels are fixed
- Logic level difference of 130mV at 0.2V with 1kcells/bitline

(T. H. Kim et al., ISSCC, 2007)

10T Sub-V_T SRAM w. Bit-Interleaving and Differential Read

- 32 Kb: 166 KHz@0.25V (Leakage: 1.4 uA for 49 Kb@0.25V) in 90 nm CMOS
- $V_{cc,min}$ = 0.16V: 500 Hz, 0.123 μW @ 0.16V
- W_WL shared by cells in a column
  - ➔ Writing a cell does not affect Hold stability of other cells along the same WL
  - ➔ Allows bit-interleaving for soft-error immunity
- Differential Read w. dynamic DCVSL for better stability and leakage tolerance



(I. J. Chang et al., ISSCC, 2008)

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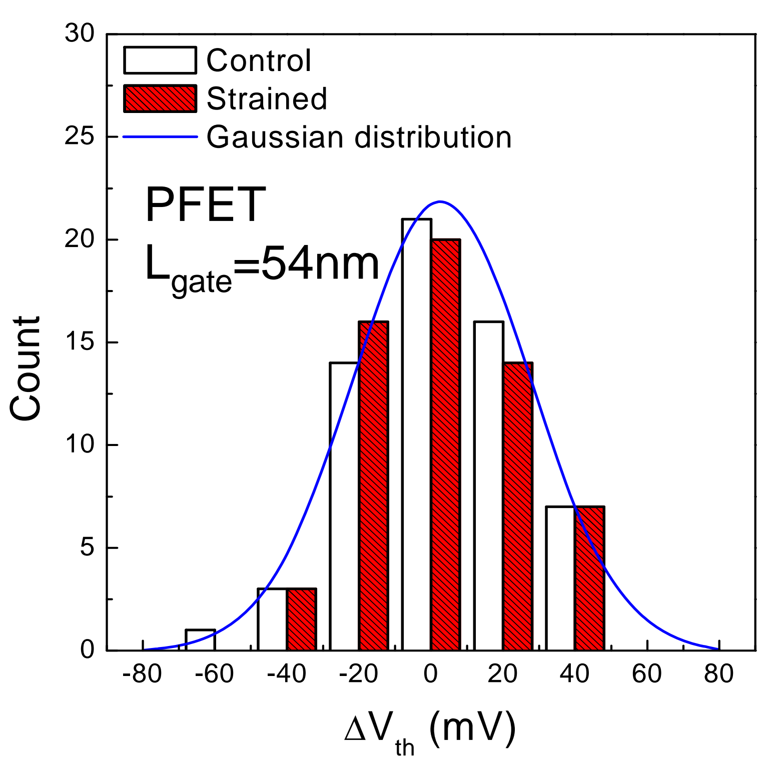
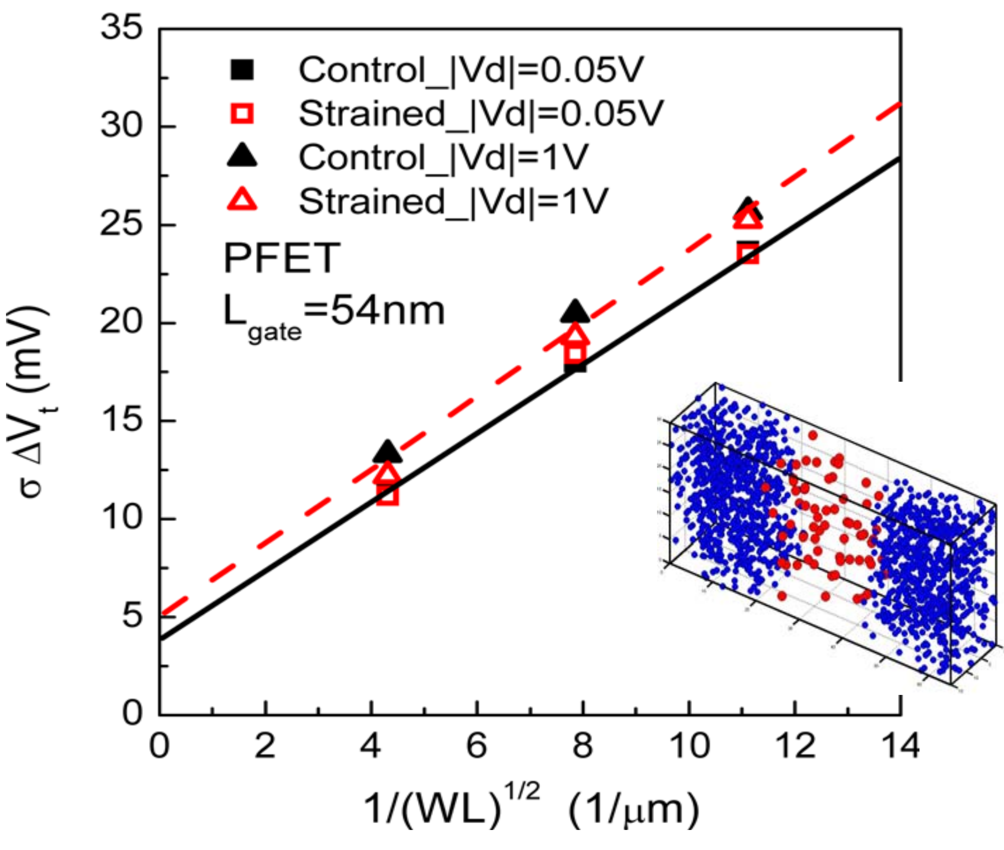
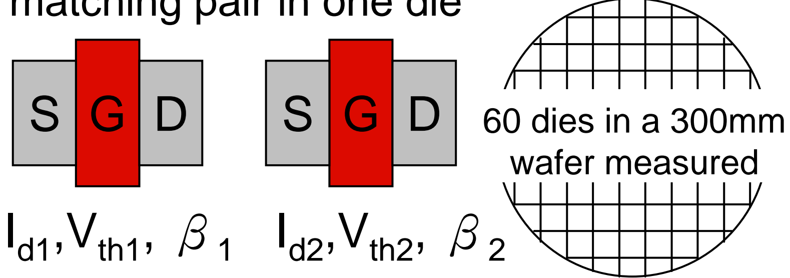
FinFET SRAM for Ultralow-Power Applications

- Ultralow-power applications such as portable devices, implanted medical instruments, and wireless body sensing networks require SRAM operating at low supply voltage below V_T.
- Degraded functional robustness is a serious concern for subthreshold SRAM.
- Conventional Bulk 6T SRAM cell has failed to offer adequate stability in the subthreshold region.

Random Mismatch in Bulk Transistors



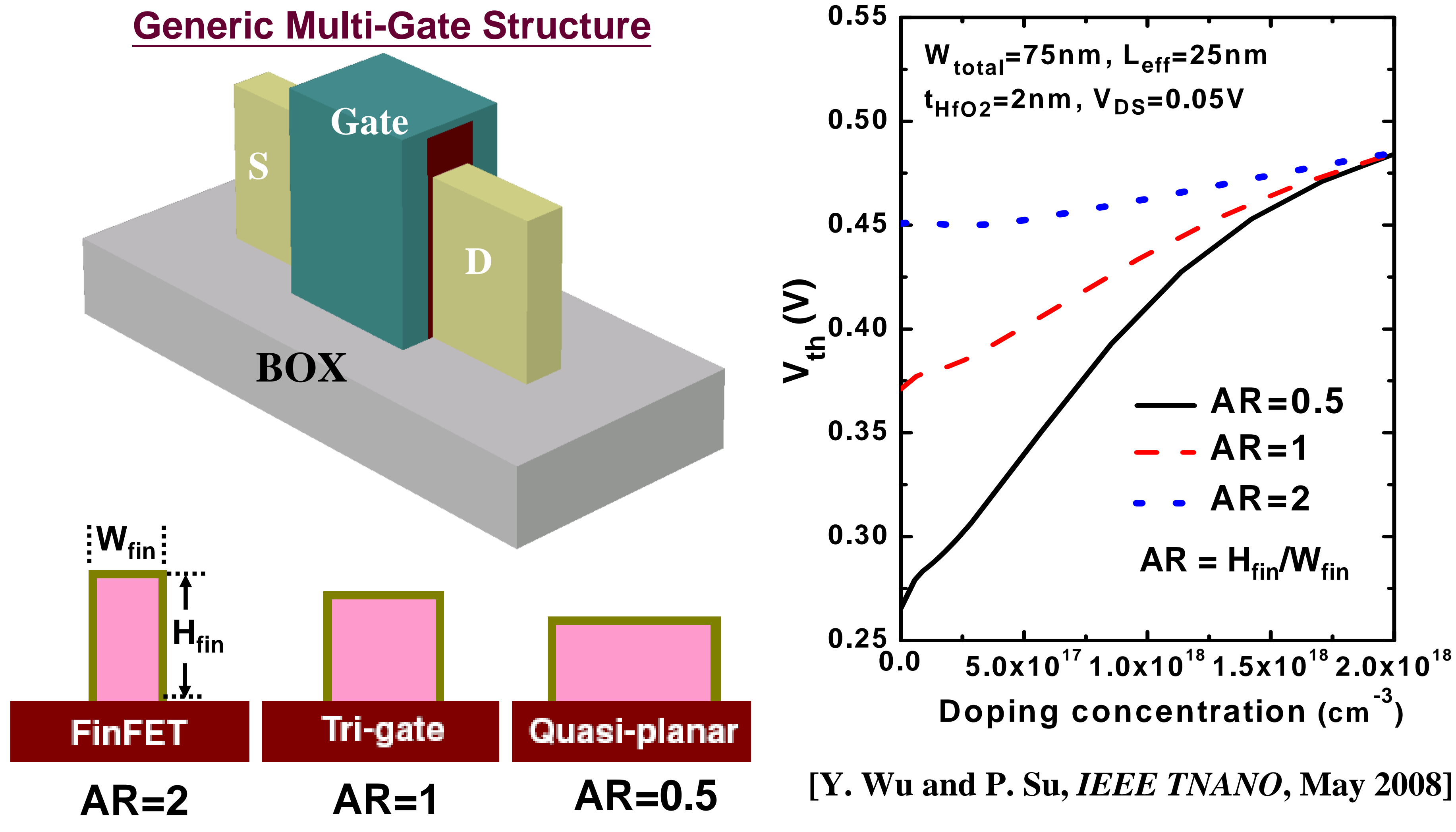




[J. Kuo *et al.*, *IEEE TNANO*, March 2010]

- **The impact of Random Dopant Fluctuation increases with device scaling because the sensitivity of a transistor increases with decreasing channel volume.**

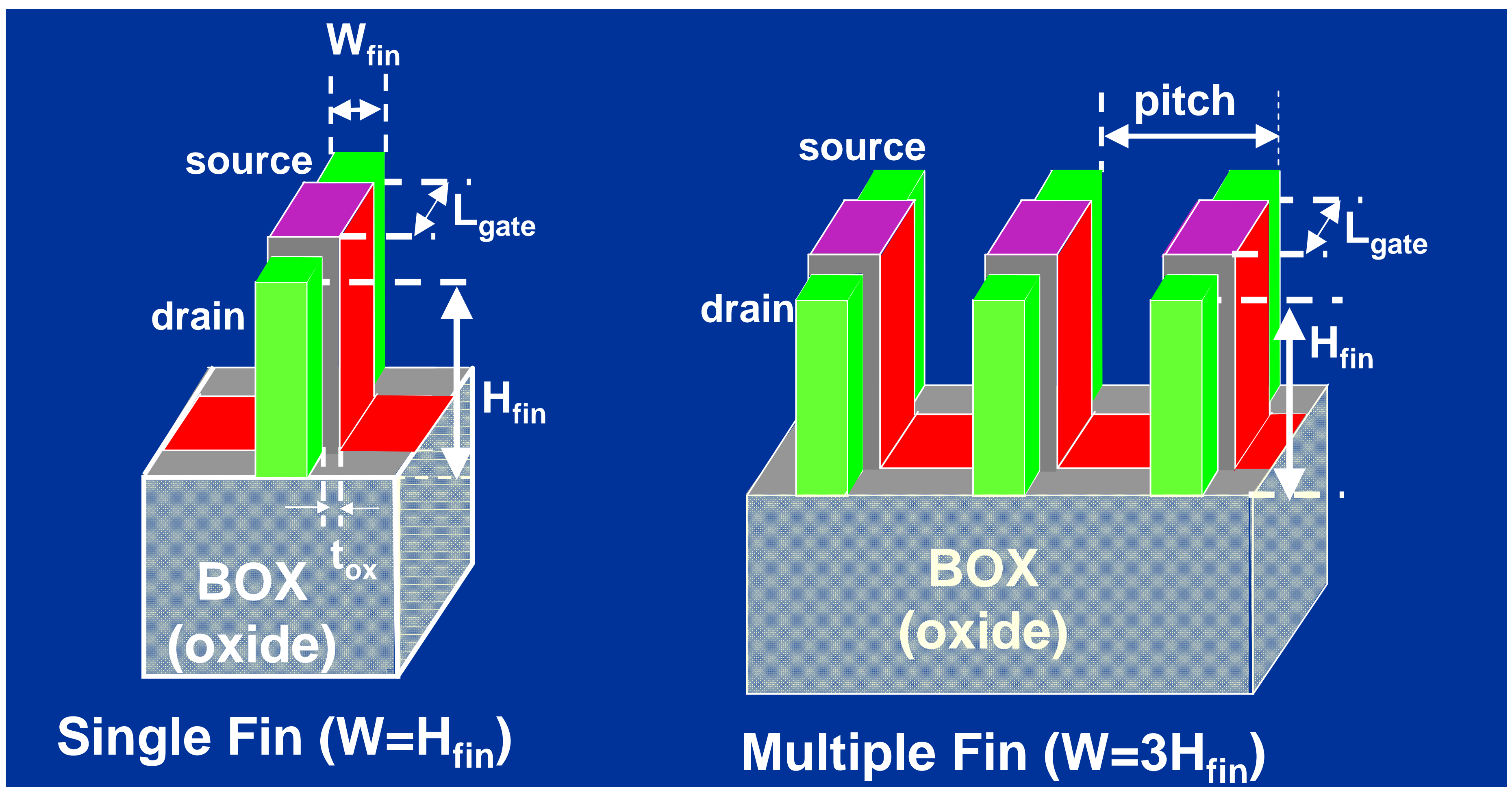
Threshold Voltage Sensitivity to Doping



[Y. Wu and P. Su, *IEEE TNANO*, May 2008]

- Small fin-width (W_{fin}) enhances the gate control and reduces the V_{th} dependence on channel doping.

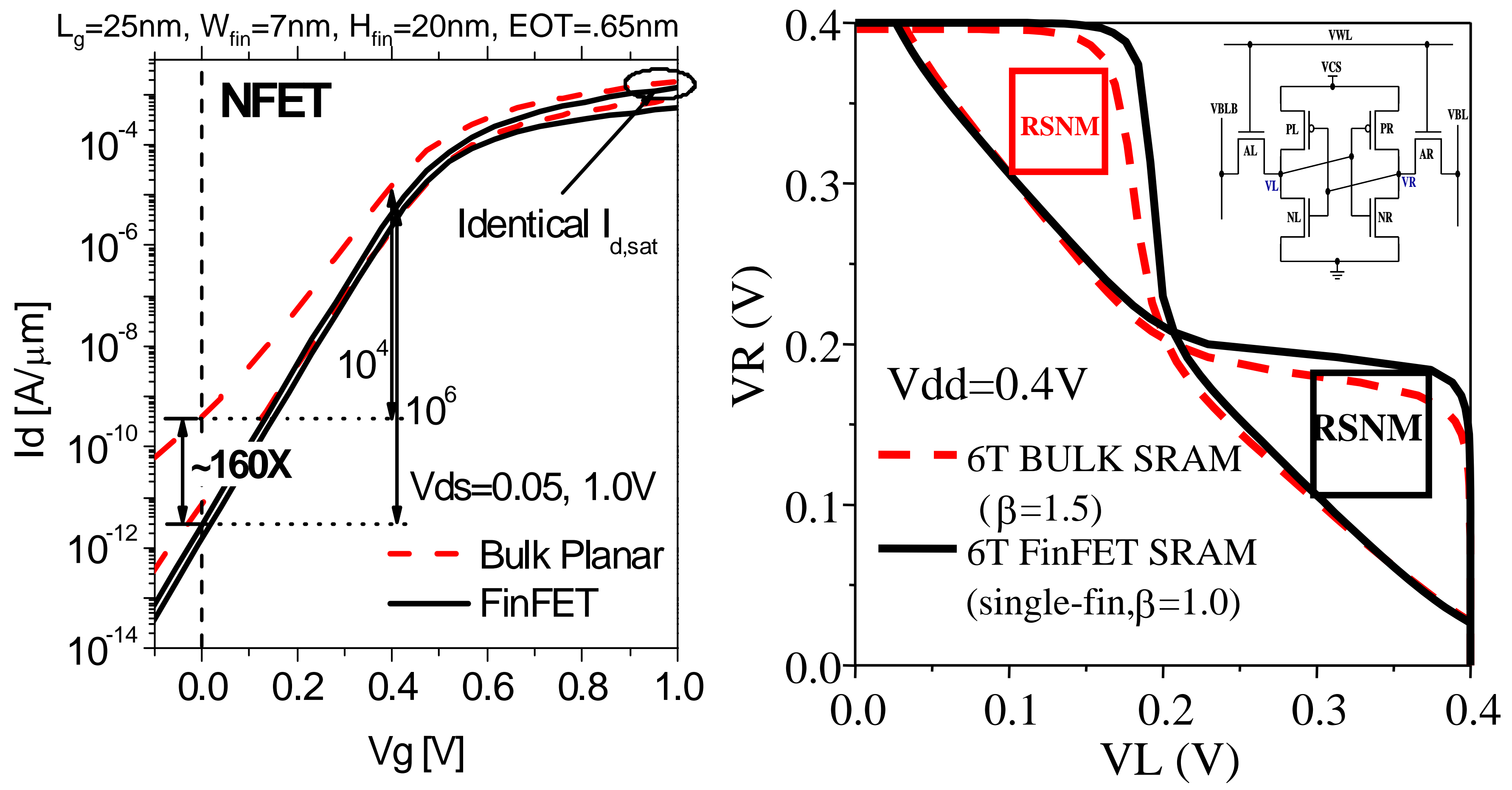
FinFET



- The device width for FinFET is quantized (integer multiple of H_{fin}).
- In a minimum-sized FinFET SRAM cell, single-fin devices are used.

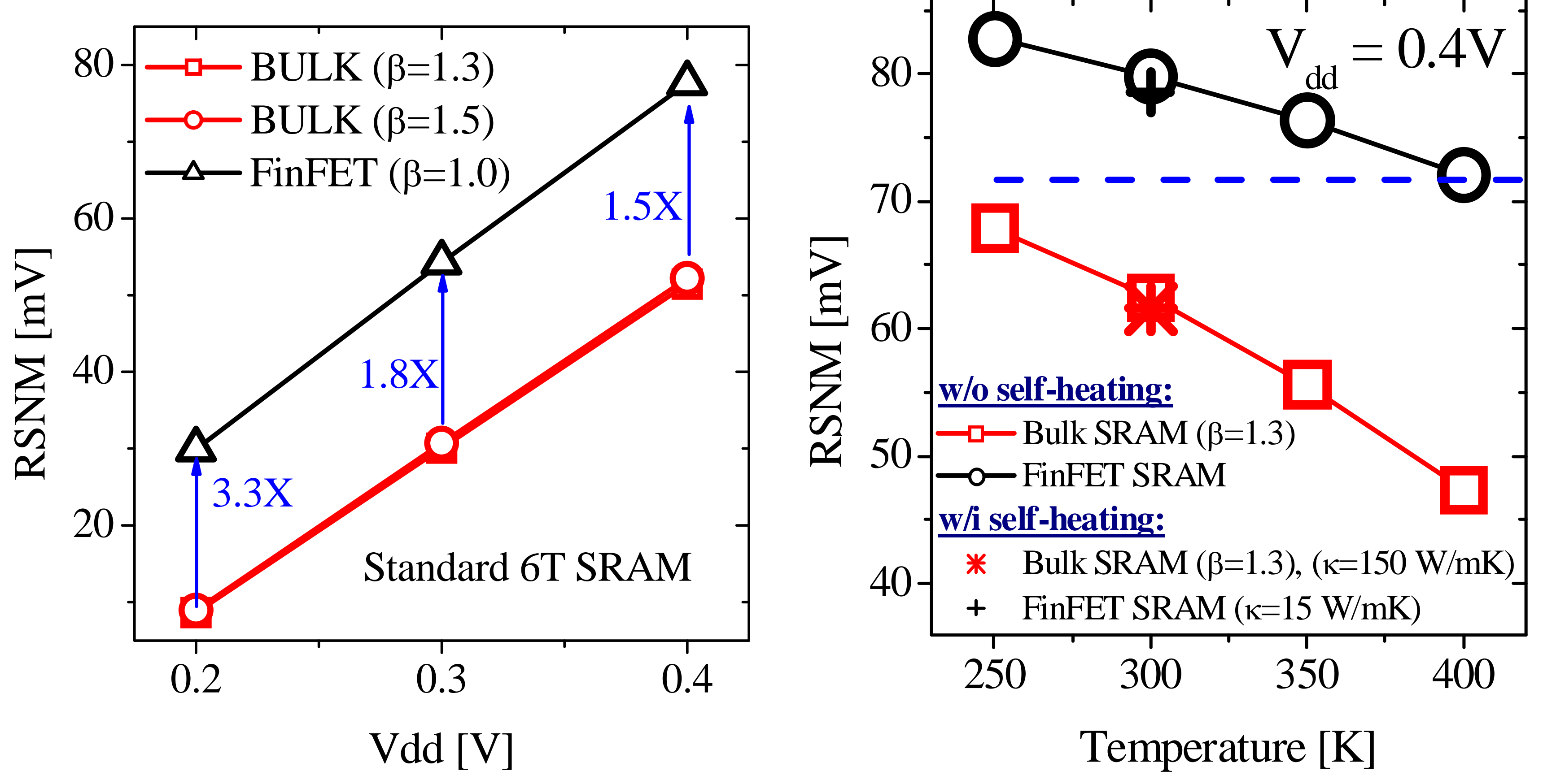
C. T. Chuang and P. Su, 04/2010

FinFET vs. Bulk



- **FinFET exhibits steeper subthreshold slope and larger I_{on}/I_{off} ratio than the Bulk counterpart.**

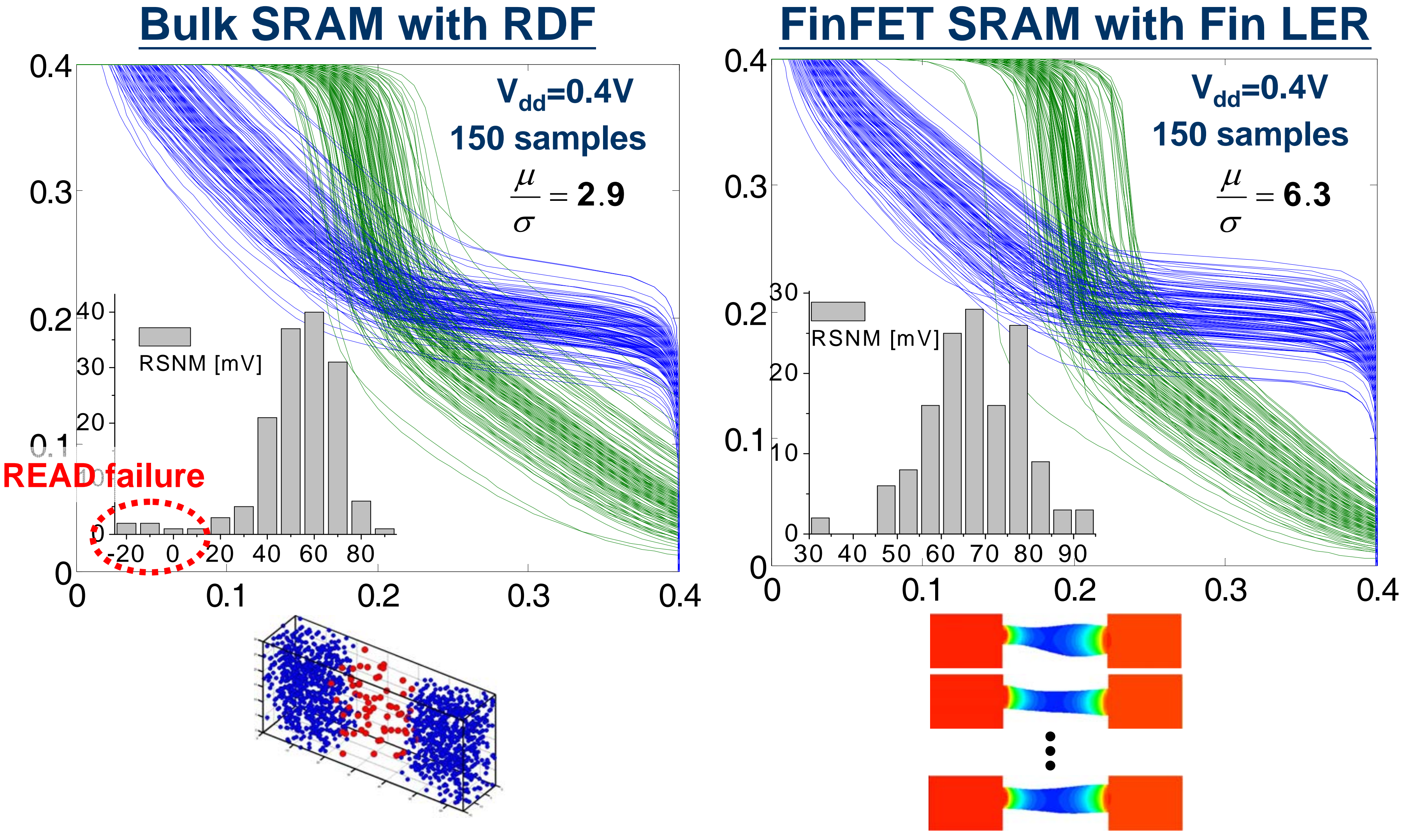
FinFET vs. Bulk



- **FinFET SRAM cell shows larger Read Static Noise Margin (RSNM) than the Bulk counterpart because of its superior electrostatic integrity.**

[M.-L. Fan *et al.*, *IEEE TED*, June 2010]

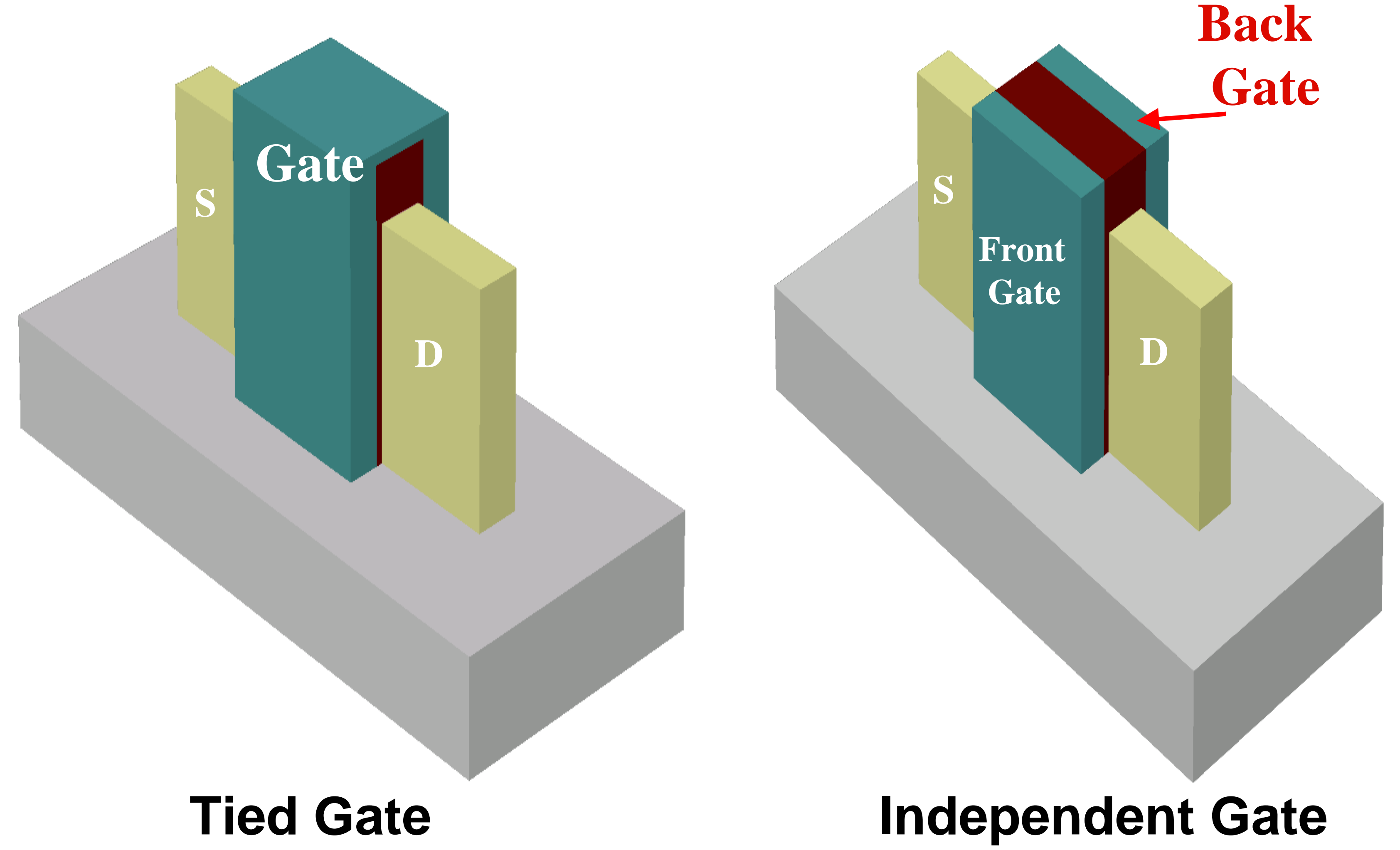
FinFET vs. Bulk



- FinFET SRAM cell can be more robust than the Bulk counterpart.

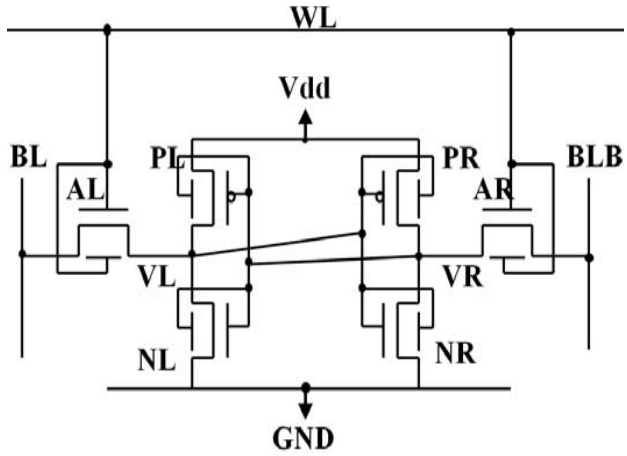
[M.-L. Fan *et al.*, *IEEE TED*, June 2010]

Independent-Gate Control Capability of FinFET

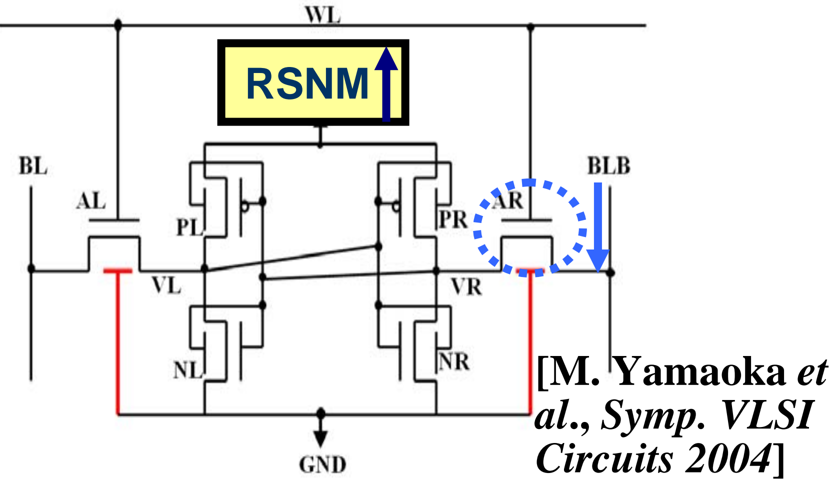


Several 6T FinFET SRAM Cells

Cell (I): standard tied-gate 6T

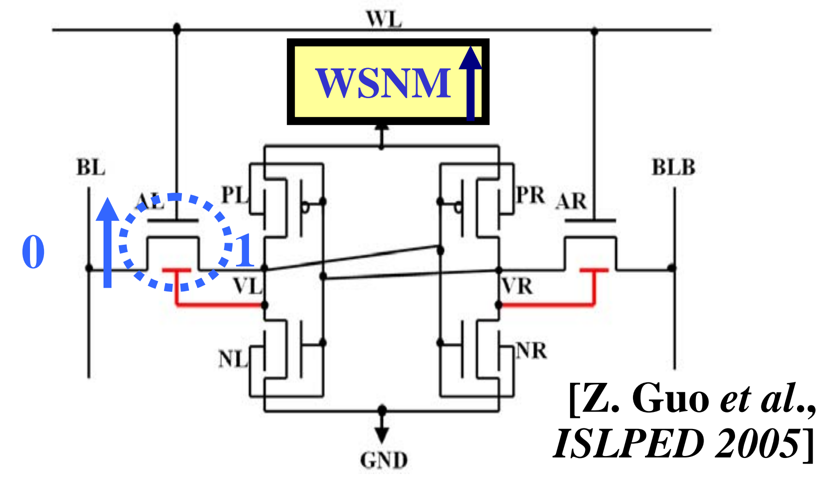


Cell (II) : Ying-Yang feedback



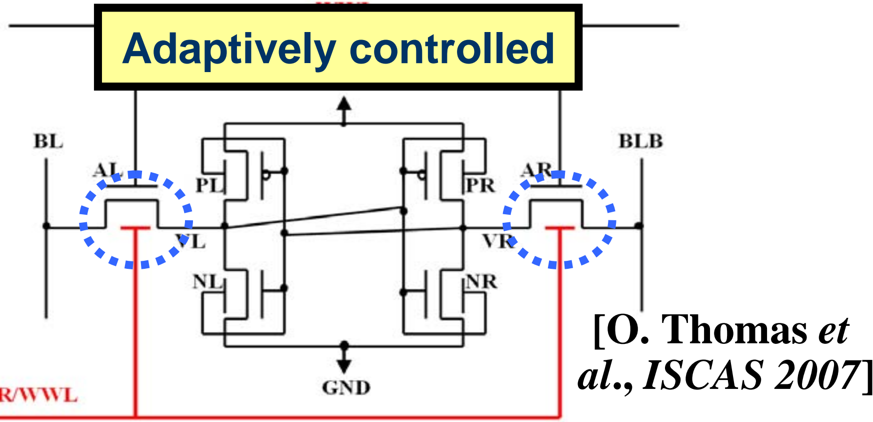
[M. Yamaoka *et al., Symp. VLSI Circuits 2004*]

Cell (III) : Improved Ying-Yang feedback



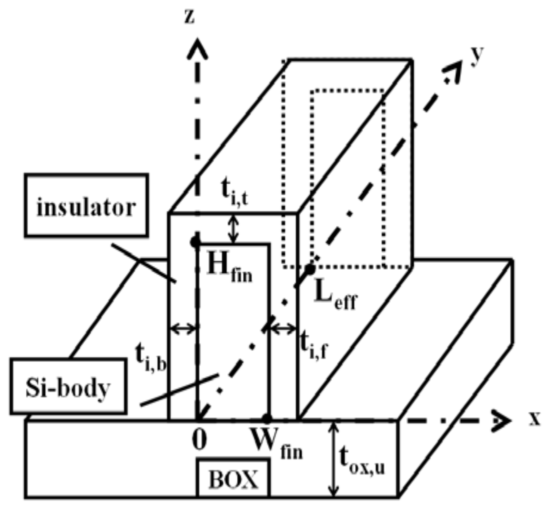
[Z. Guo *et al., ISLPED 2005*]

Cell (IV) : Doubled-WL



[O. Thomas *et al., ISCAS 2007*]

Analytical FinFET Subthreshold Model



$$\phi(x,y,z) = \phi_1(x) + \phi_2(x,z) + \phi_3(x,y,z)$$

$$\phi_1 = -\frac{qN_a}{2\varepsilon_{si}}x^2 + ax + b$$

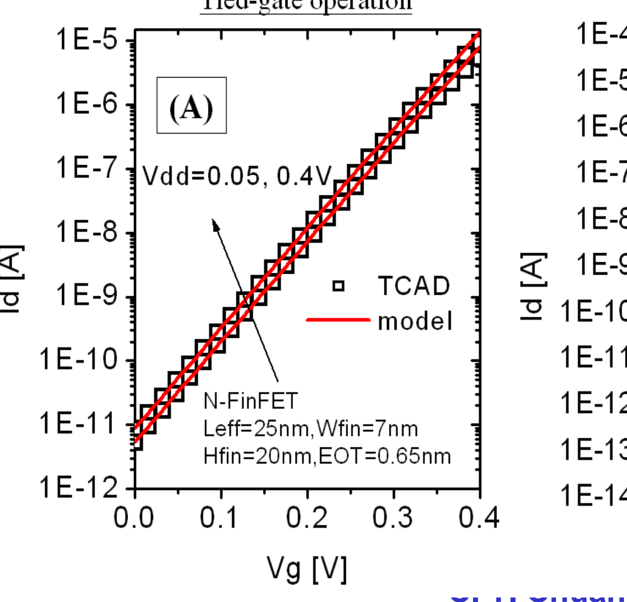
$$\phi_2 = \sum_{i=1}^{\infty}\left\{\left[c\sinh\left(\frac{i\pi}{W_{eff}}z\right) + c'\sinh\left(\frac{i\pi}{W_{eff}}(W_{eff}-z)\right)\right]\cdot\sin\left(\frac{i\pi}{W_{eff}}x\right)\right\}$$

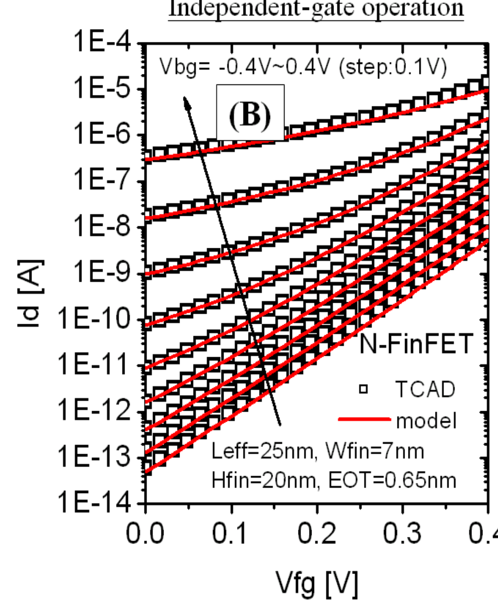
$$\phi_3 = \sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\left\{\left[e\sinh(k_y y) + e'\sinh(k_y(L-y))\right]\cdot\sin\left(\frac{m\pi}{W_{eff}}x\right)\sin\left(\frac{n\pi}{H_{eff}}z\right)\right\}$$

The drain current can be calculated using the channel potential solution $\phi(x,y,z)$:

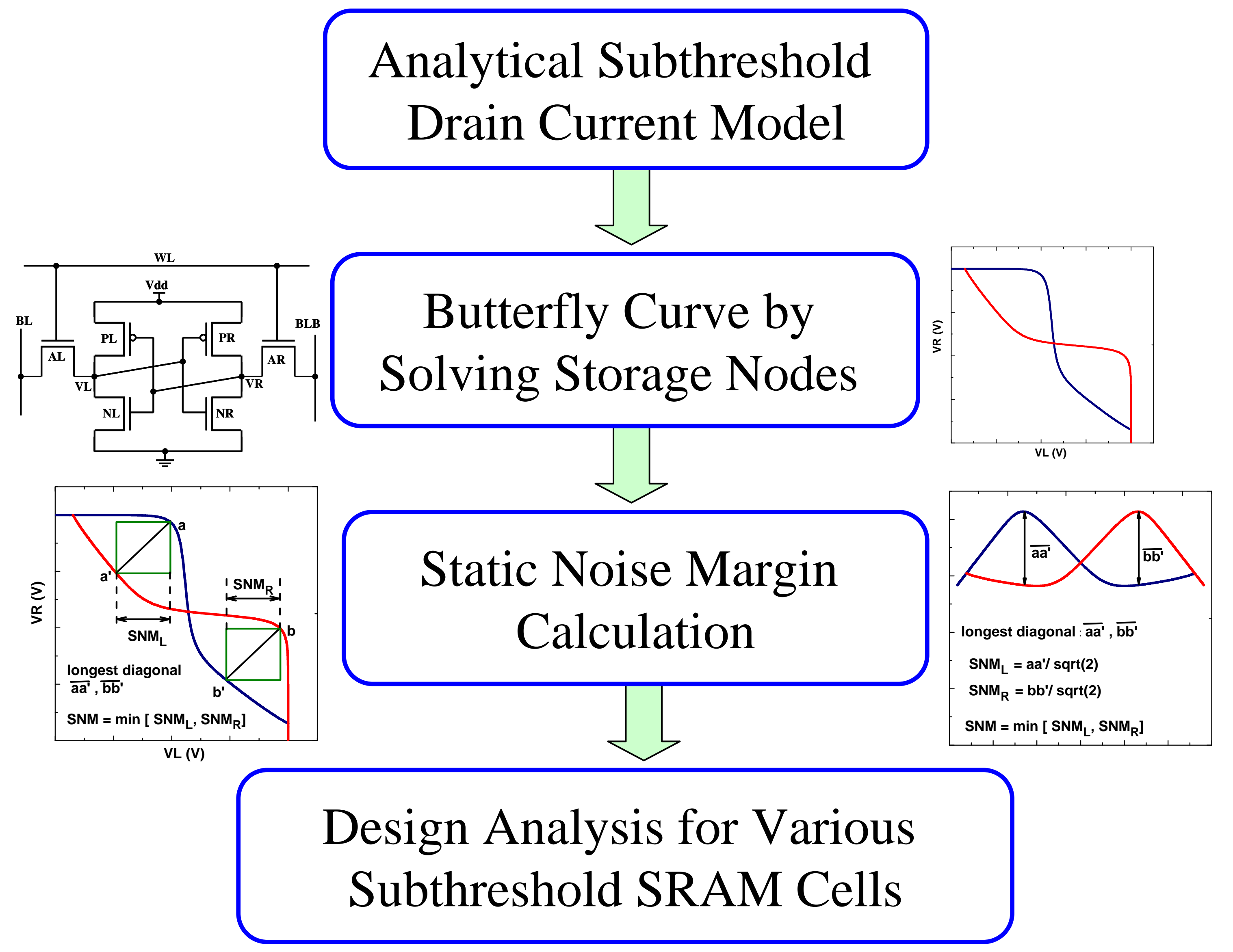
$$I_{DS} = \frac{q\mu_n\left(\frac{kT}{q}\right)\left(\frac{n_i^2}{N_a}\right)\left(\exp\left(\frac{-V_S}{kT/q}\right) - \exp\left(\frac{-V_D}{kT/q}\right)\right)}{\int_0^{L_{eff}}\frac{dy}{\int_0^{H_{fin}}\int_0^{W_{fin}}\exp\left(\frac{q\phi(x,y,z)}{kT}\right)dxdz}}$$

[Y. Wu and P. Su, *IEEE TED*, Nov. 2008]



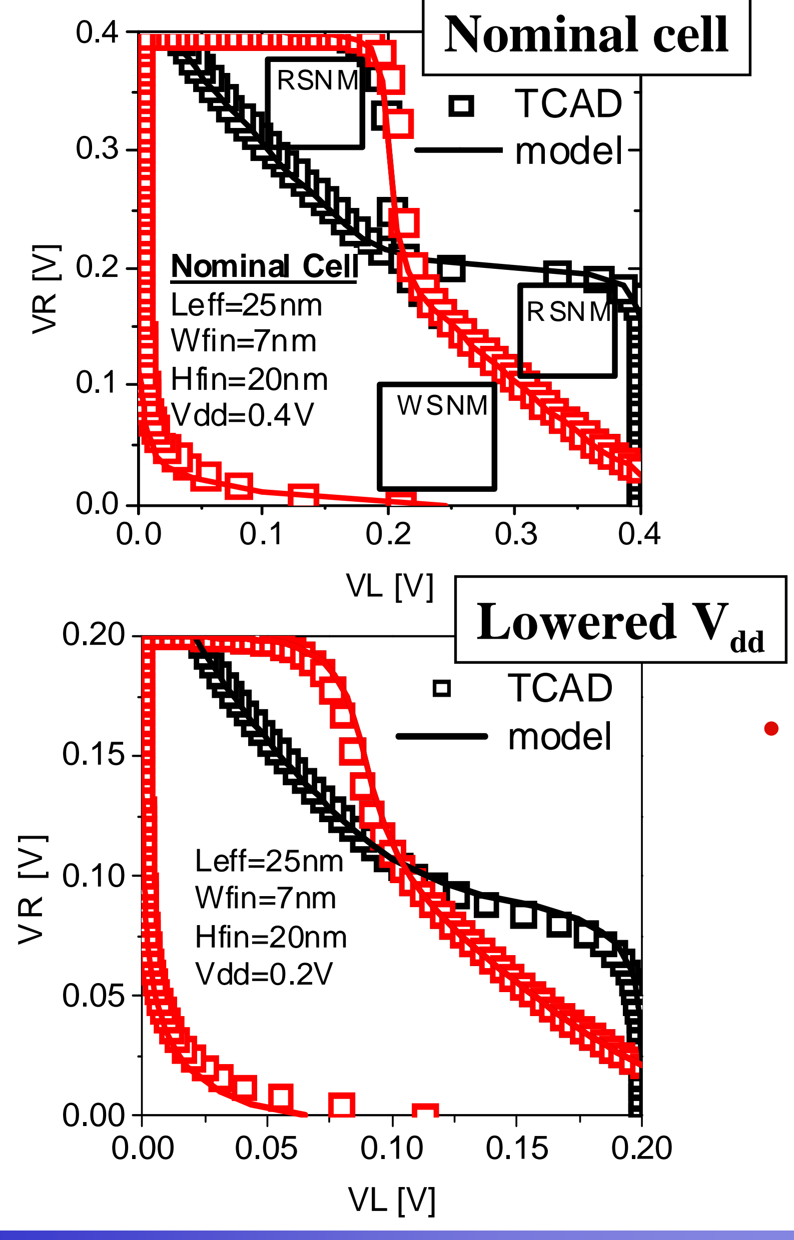


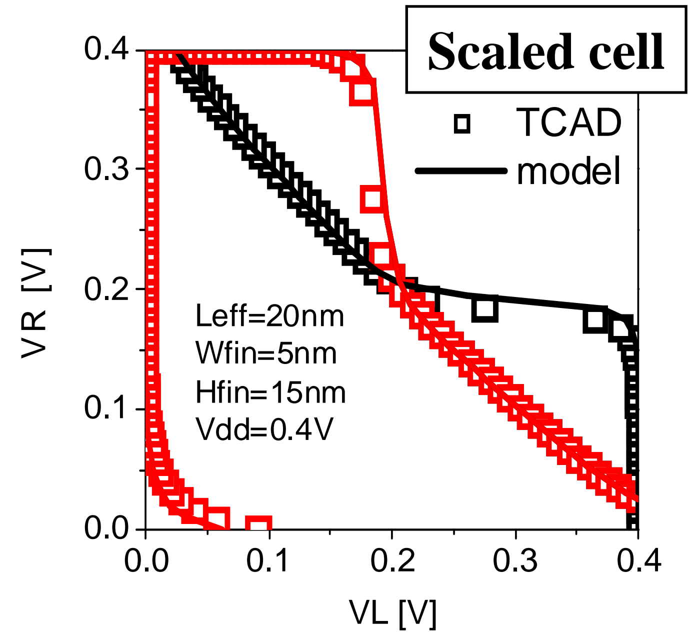
Analytical FinFET/UTBSOI Subthreshold SRAM Framework



[V. P.-H. Hu *et al.*, *IEEE TED*, Sep. 2009]

Verification – Scalability & Efficiency

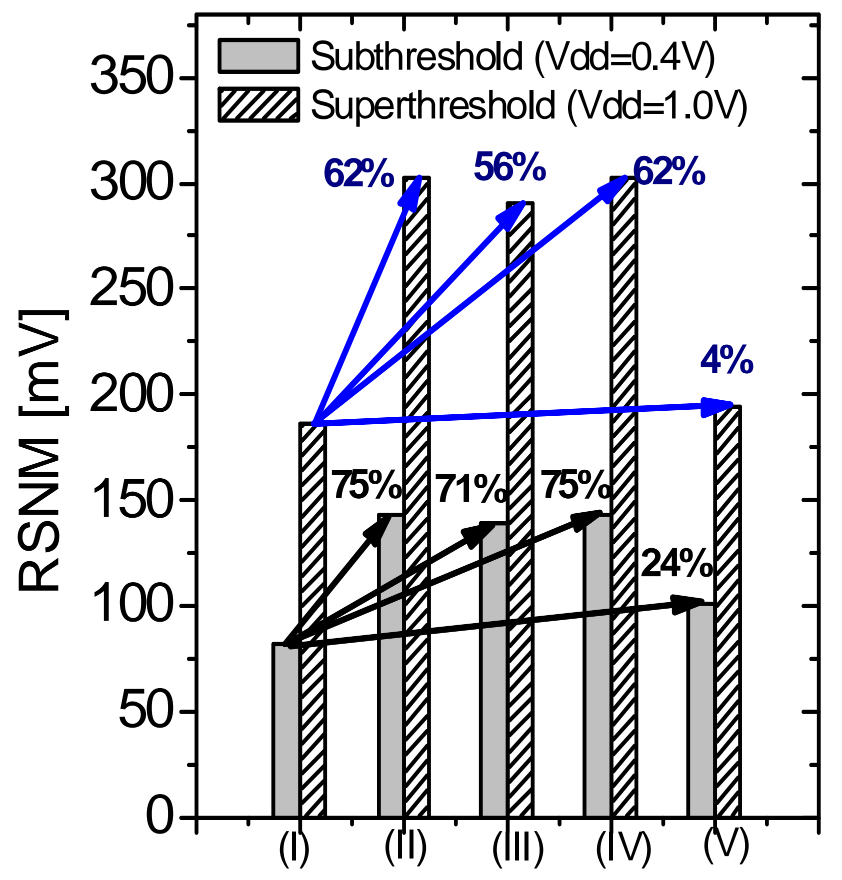




- **Analytical approach not only shows better efficiency than TCAD mixed-mode simulation, but also enables an assessment for sensitivity to process variations.**

[M.-L. Fan *et al.*, *IEEE SOI Conf.*, Oct. 2009]

RSNM Comparison of 6T FinFET SRAM Cells

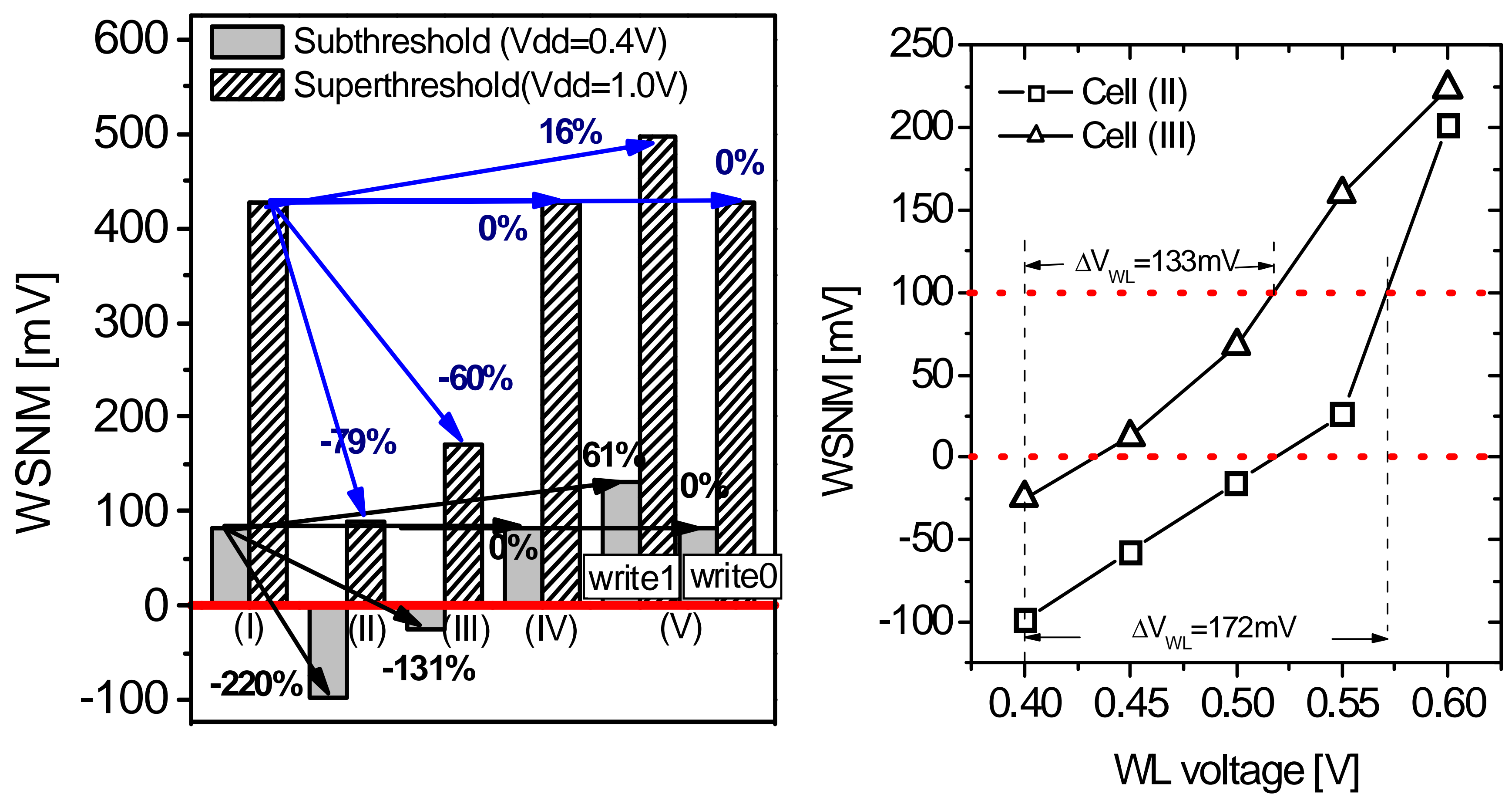


[M.-L. Fan *et al.*, *VLSI-TSA*, April 2010]

(I)	Standard tied-gate 6T
(II)	Ying-Yang feedback
(III)	Improved Ying-Yang feedback
(IV)	Double word-line structure
(V)	Asymmetrical cell

- **Cell (II), (III) and (IV) show significant RSNM improvement as compared with cell (I).**
- **The percentage improvement in RSNM is larger for Subthreshold than Superthreshold.**
- **R/W WL voltage control is effective to improve the cell stability of subthreshold SRAM.**

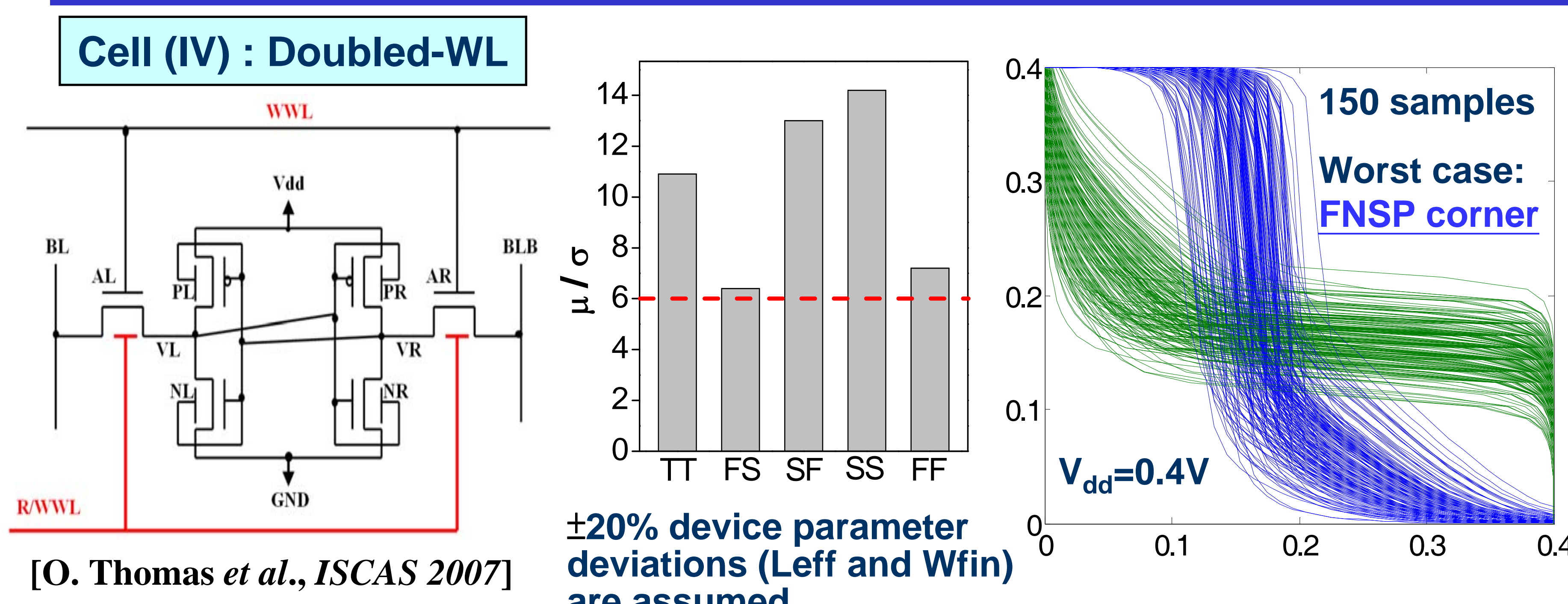
WSNM Comparison of 6T FinFET SRAM Cells



- Cell (II) and (III) fail to WRITE at V_{dd} =0.4V. Boosted WL technique is needed to restore the Write-ability.
- The Write-ability of Cell (IV) is not degraded.

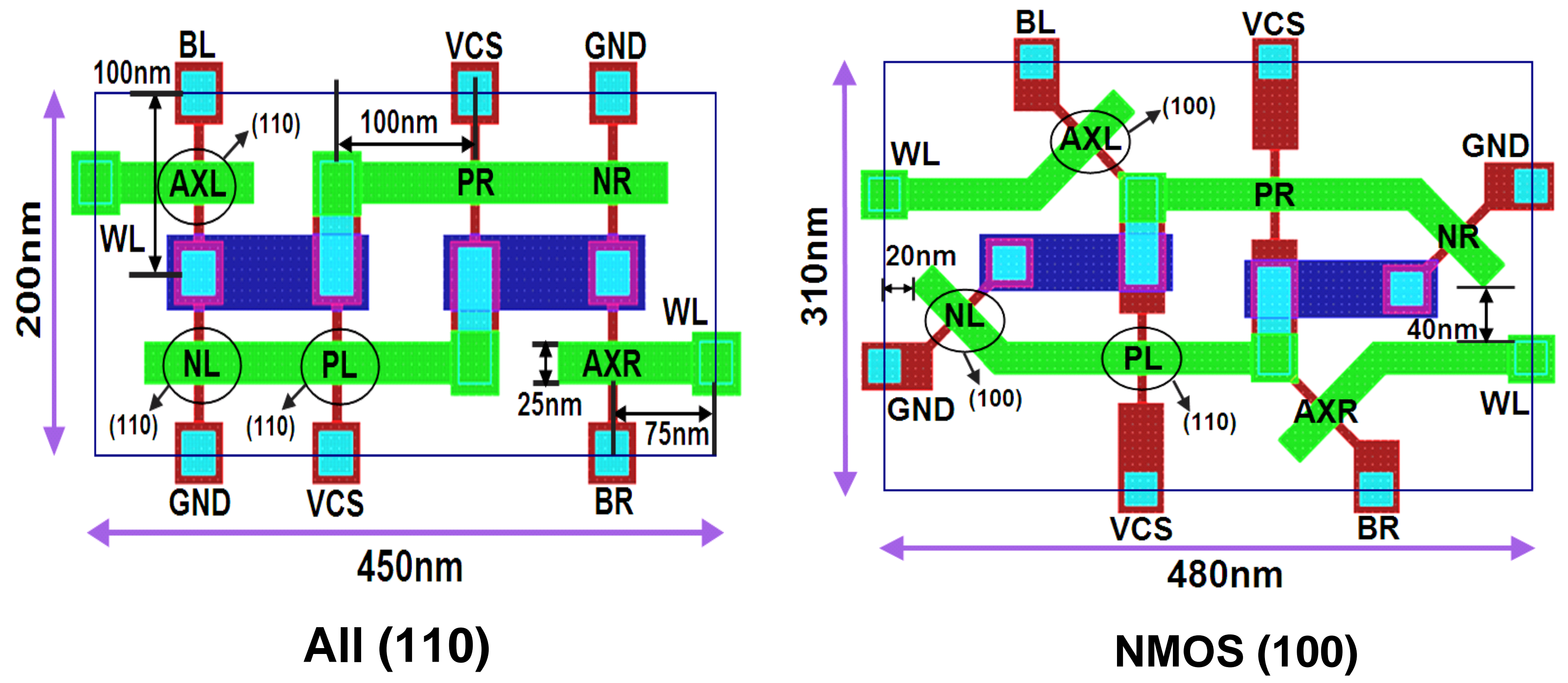
[M.-L. Fan *et al.*, *VLSI-TSA*, April 2010]

Stability of Double-WL FinFET SRAM Cell



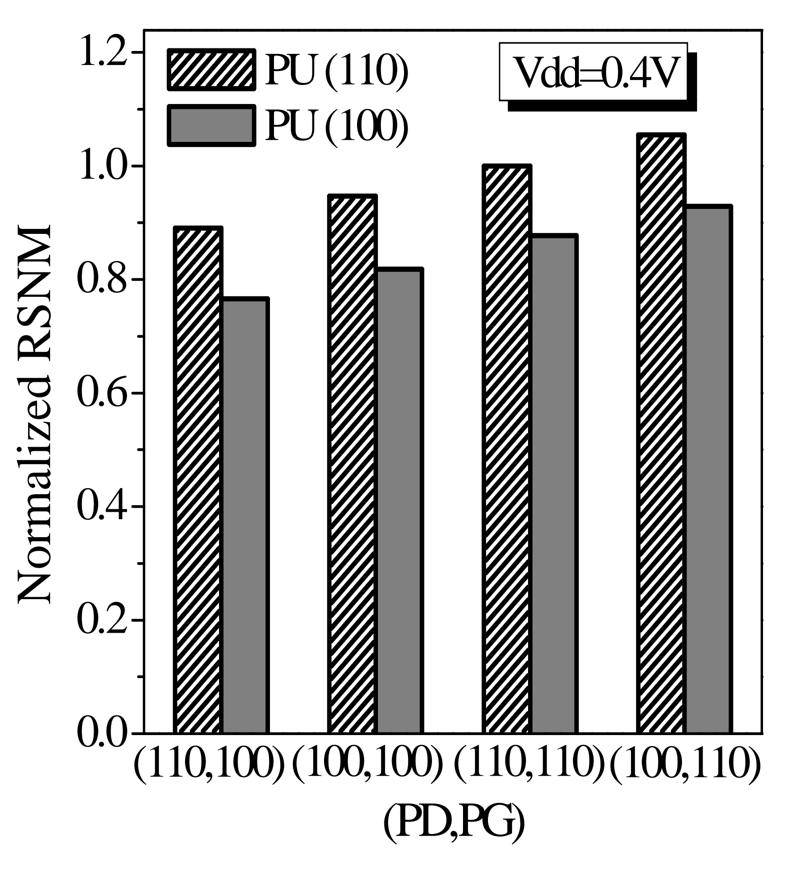
- Local random variation (Fin LER) together with global process variations (process corners) are considered by Monte Carlo simulations.
- Double word-line SRAM cell with adequate nominal RSNM can provide sufficient μ/σ ratio in RSNM for various process corners (TT = 10.9, FS = 6.4, SF = 13, SS = 14.2, FF = 7.2) at V_{dd}=0.4V.

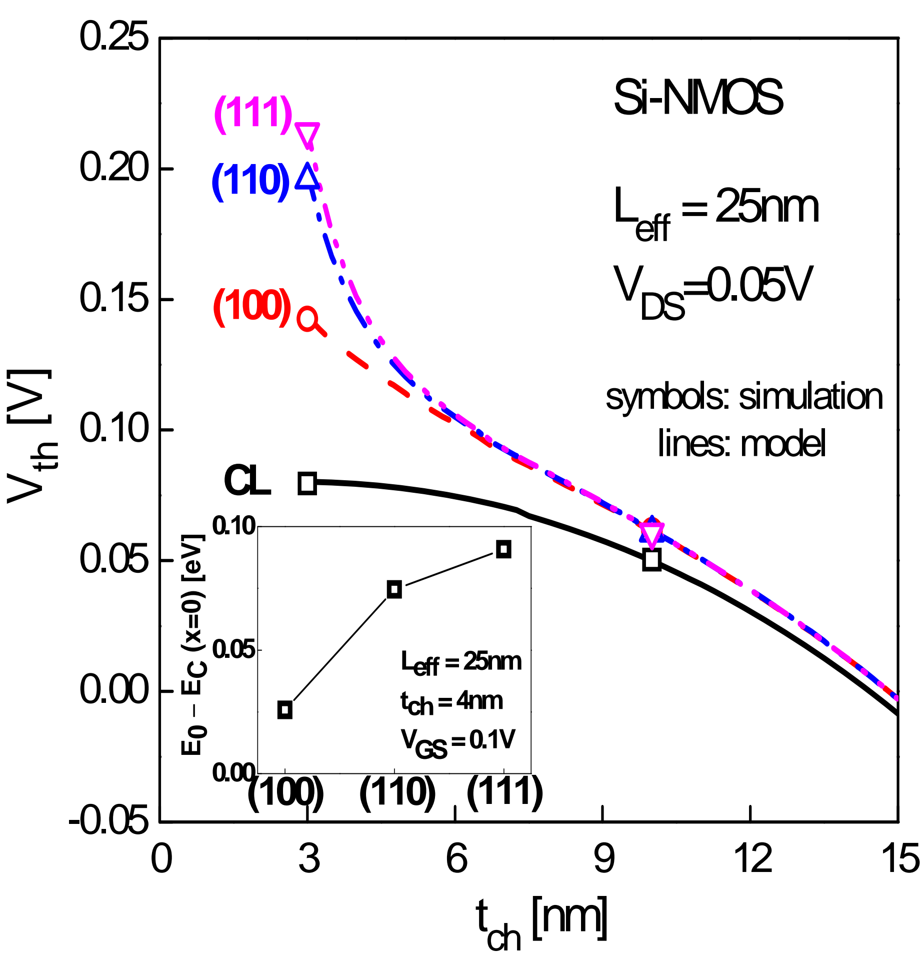
Impact of Surface Orientation on FinFET SRAM Cell



- **For FinFET, the conventional sidewall conducting (110) surface orientation can be rotated by layout to improve the cell stability.**

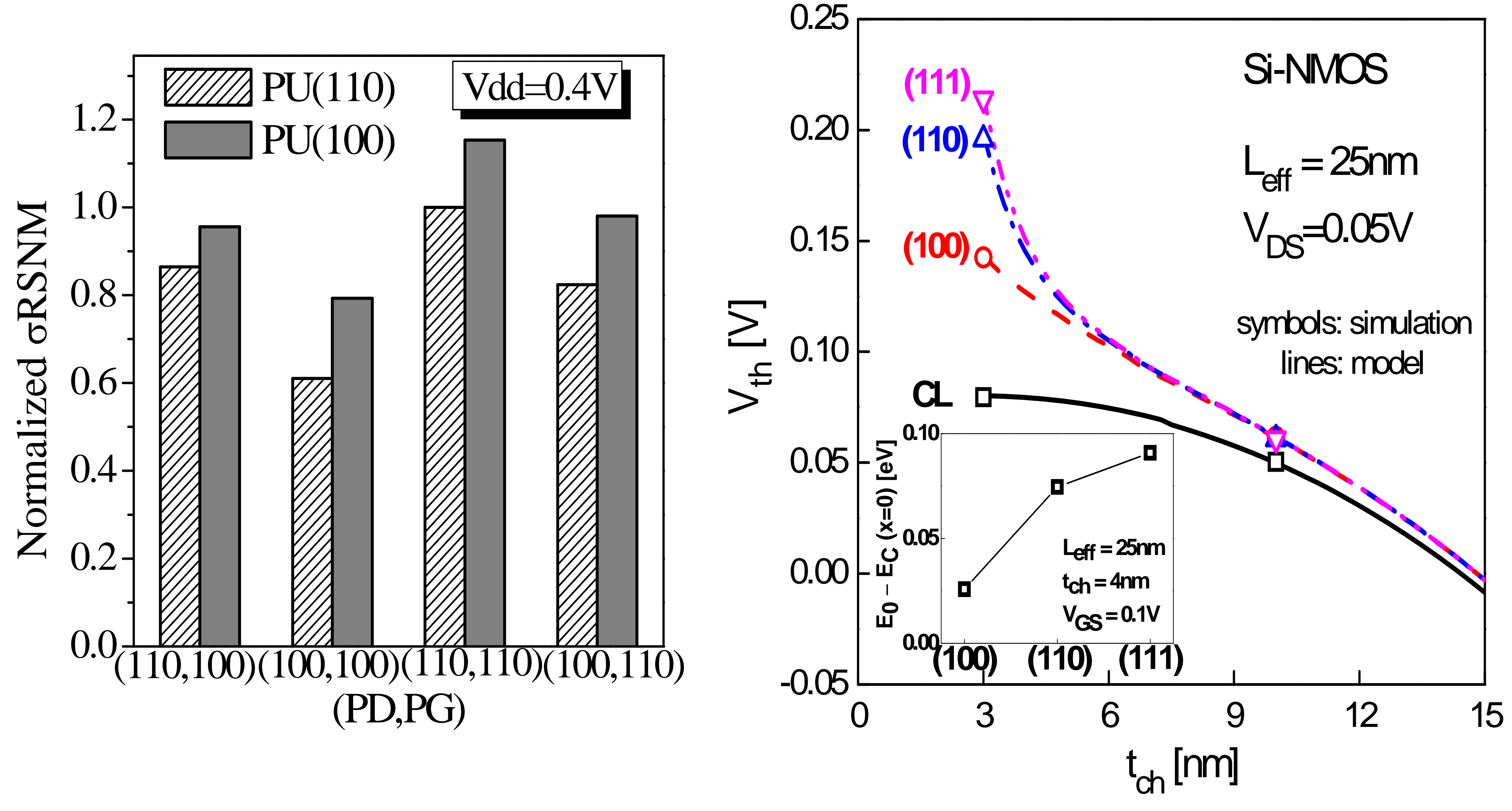
Impact of Surface Orientation on FinFET SRAM Cell





C. T. Chuang and P. Su, 04/2010

Impact of Surface Orientation on FinFET SRAM Cell



Conclusion

- With superior electrostatic integrity, suppressed random dopant fluctuation, independent-gate control capability and surface-orientation optimization, FinFET SRAM cell can be more robust than the Bulk counterpart.