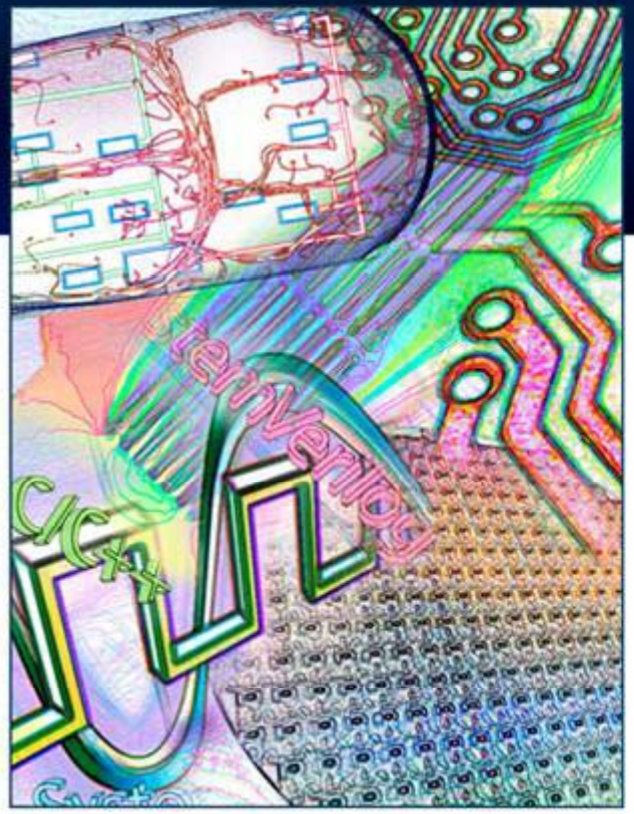
Variability, Friend or Foe?: An EDA perspective



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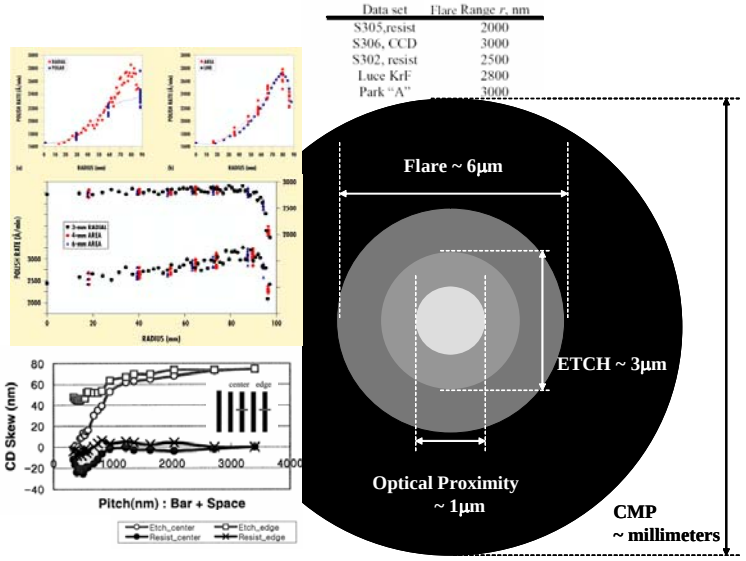
Mentor Graphics

Outline

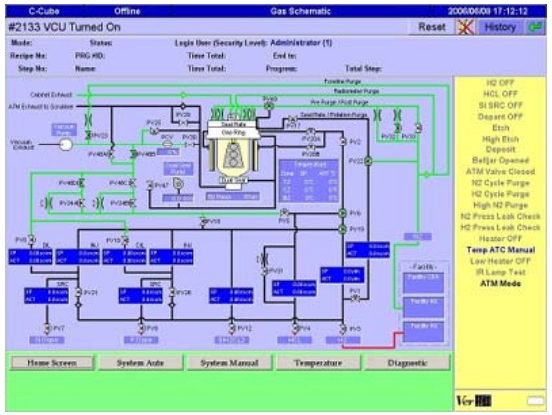
- Variability
- **Foe** of yield
- **Friend** of innovation
- Why does it matter to:
  - IC manufacturers
  - Vendors (i.e. EDA)
  - Academia

Variability… what kind?

- All of it!
  - Litho
  - CMP
  - Particles
  - Etch
  - Rapid Thermal Annealing



- Process control is neither trivial nor perfect



Variability as Foe of Yield

- Foe
  - A thing that is harmful to or destructive to something [1]
- Variability meets the requirement:
  - It is harmful and destructive to product yield.
  - It does not have any redeeming qualities.
    - It cannot be harnessed.
    - It is not useful.
    - It cannot be eliminated from the process.
- What is being done?
  - Reduce semiconductors product's sensitivity to manufacturing variability
    - Robust/Redundant logic (i.e. SRAM)
    - Corner/Statistical modeling
    - Layout regularity
    - New devices/manufacturing processes (i.e. FinFETs)

Source: [1] dictionary.reference.com/browse/foe

Is regularity a silver bullet? … litho

- No. It is more of an enabler, and there is plenty to work to be done

Process variability source	Benefits of regularity	Challenges	Research
Lithography	Reduces the number of patterns that need to exhibit the same response to process variations. Higher layout densities can be achieved.	Which layout patterns are optimal? 1D grids are not uni-dimensional when arbitrarily distributed spatial discontinuities are inserted.	**Composability:** Ability to guarantee methods in which previously validated layout remains valid. **Compatibility:** Ability to determine the set of layout structures for which a composable solution exist.

Is regularity a silver bullet? … CMP

- Easy to define for base-layers, not for interconnect.

Process variability source	Benefits of regularity	Challenges	Research
CMP	Density and perimeter are the main drivers of electroplating and polishing differences. Regular designs with same pattern density and perimeter are likely to exhibit low thickness variation.	While regularity can be easily enforced in base layers, not so at interconnect level. Fill structures that deliver the necessary layout composition to homogenize the metal layers across the wire stack.	**Placement:** Currently guided mainly by routing requirements. Needs to be jointly optimized with routing to achieve optimal robustness. **Fill:** Ability to determine the set of fill structures which remain litho compatible and provide CMP homogeneity

Is regularity a silver bullet? … Particles

- Critical area: The oldest of the approaches and ignored many times.

Process variability source	Benefits of regularity	Challenges	Research
Particles	Critical area assessment turns into a simple area calculation since all layout is homogeneous.	Several sources of particles. Becomes main yield limiter for large designs since it is not possible to make the probability of a short zero when a non-zero particle distribution exist.	**Electrical awareness:** Only active layout (and not dummy or fill structures) need to be taken into the consideration of CAA.

Is regularity a silver bullet? … Etch

- More emphasis due to Double Patterning dependency on Etch/resist freezing

Process variability source	Benefits of regularity	Challenges	Research
Etch	Microloading effects reduced. LUT modeling approaches become viable.	Most DP techniques assume that Etch does not affect lithography enough. However without maintaining layout density between complementary masks this may no longer be a valid assumption.	**Etch regularization:** Lithography has sub-resolution assist features to mitigate the effect of iso-dense biases. Etch does not have any equivalent regularization technique. Given the scale difference between litho and etch they are not compatible to be run at the same time for runtime requirements

Is regularity a silver bullet? … RTA

• Also depends heavily in reflection of the surface. It has been referred to as the “only” yield-killer during the DFM hype.

Process variability source	Benefits of regularity	Challenges	Research
RTA	Homogenizes reflectivity of the substrate that in turn homogenize the thermal profile of the die.	Not clear that simple fill pattern insertion is sufficient. Do we need models? Maybe not.	**Adaptive fill patterns:** Given the dependency of litho, etch, cmp and RTA to layout structures, there is a need to make sure that any fill pattern somehow considers all these three major effects. In addition methods to reduce floating capacitance due to fill structures need to be investigated.

Variability as Friend of Innovation

- Friend
  - An ally in a fight or cause; supporter [2]
- Variability meets the requirement:
  - The creed of the semiconductor industry has been: Faster, Smaller, Cheaper.
  - Process scaling has been able to provide advantages in all these three areas.
    - But variability has limited the benefit of migrating to a new node.
  - It used to be that innovation in process technology as all we needed.
    - But now that level of innovation is required in logic and physical design in order to maintain overall product profitability.

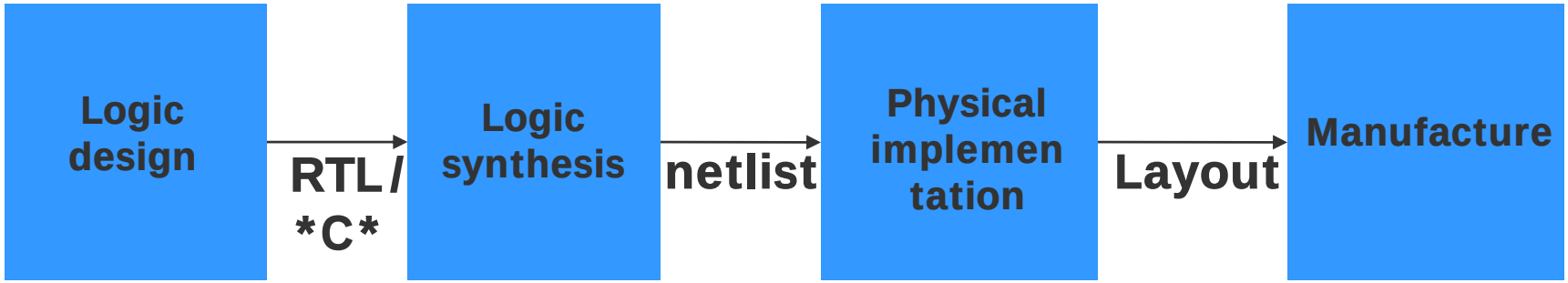
Source: [2] www.thefreedictionary.com/friend

Pattern Matching Vs Process-model for physical verification

Pattern Matching Advantages	Pattern Matching Challenges	Process-model Advantages	Process-model challenges
Runtime. Can be fast.	Limited on its ability to predict outside the pattern library used during training.	If the model is sufficiently complete, it can predict conditions which can jeopardize yield integrity.	While more complete than pattern matching models remain at the mercy of gaps in the understanding of the process.
Easy to define from known failure patterns.	Fuzzy pattern match techniques are “fuzzily” defined as long as the fuzzy pattern creation is defined on individual pattern basis		Runtime-wise: Very expensive
Deterministic and consistent (Integer space)			Possibly inconsistent (Real space)

There may be alternatives that bring the best of both worlds. Most major EDA companies working on their own versions.

Open questions for streamlined manufacturing aware design



Regularity questions:

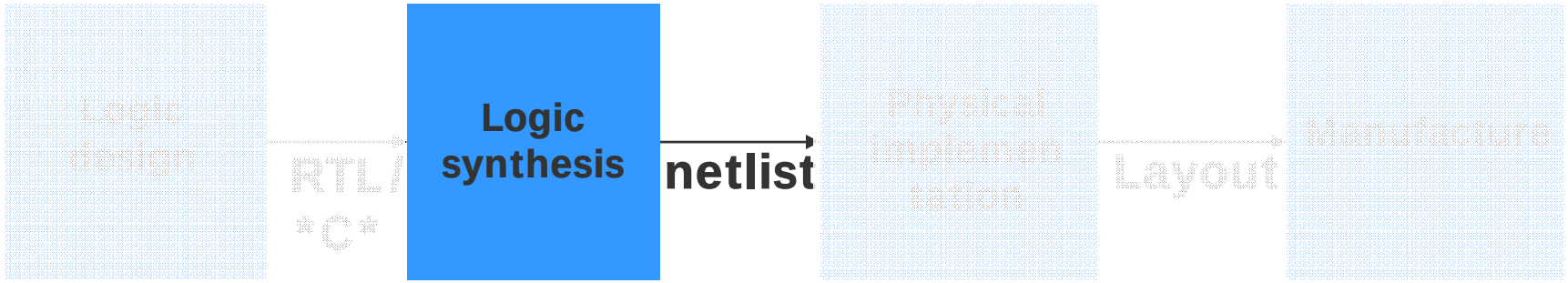
Opportunity:

a) Once we answer these questions we can implement a prototype flow of ultra regular designs from physical design to manufacture.

b) We could open the possibility of providing better and more accurate physical information to RTL synthesis tools.

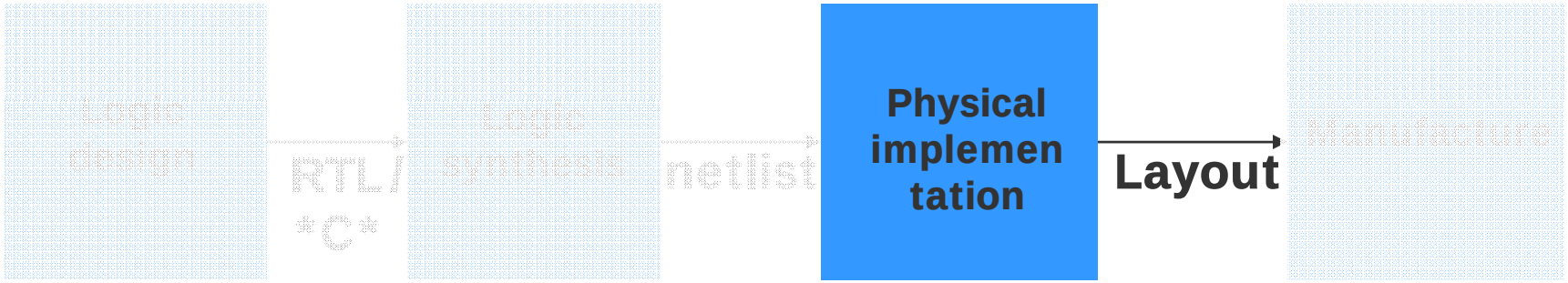
1) **How do we define "regular" designs in an useful and applicable way?**
2) **Can pattern matching tools be used to fully identify unwanted topologies?**
3) **Can regularity open new ways to verify, simulate and correct designs?**
4) **How do we define patternable and composable standard cells?**
5) **How do we impose place and routing restrictions?**
6) **Do we need contours or can effects be modeled without them?**

Logic Synthesis



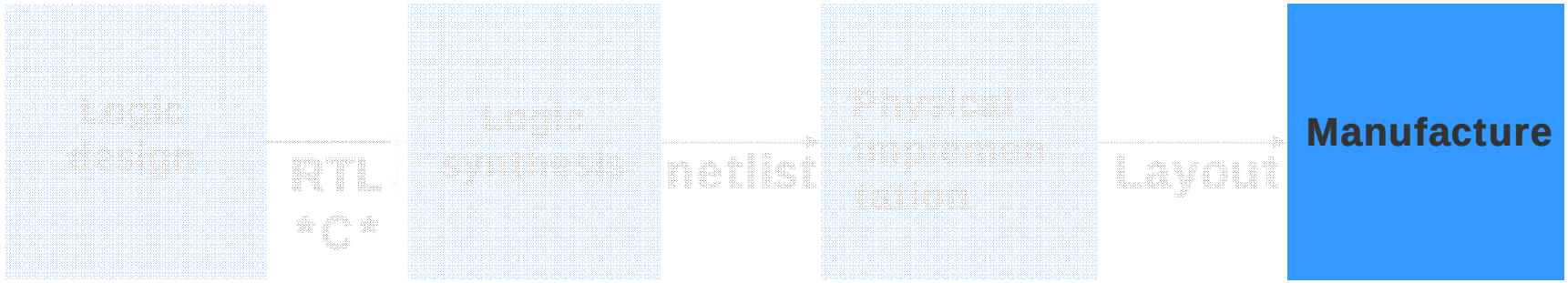
- Determine logic opportunities in architectural changes when regularity exists
- SSTA can now be done simply since all the regular designs have the same signature and there will be only a random component.
- Determine the effects of stress effects in fully regular devices and determine what is a regular layout from the point of view of stress and what are the characteristics needed to guarantee composability.
- Explore the possibility to do power, timing and thermal analysis using a netlist representation assuming it is possible to make inferences of the final layout at this stage.

Physical Implementation



- **Leverage knowledge in low power design in FPGA to determine the best implementation of low power characteristics in regular designs.**
- **Determine the possible efficiencies or challenges in regular interconnect layers.**
- **Study the impact of regular designs in thermal integrity and derive rules of composability to guide upstream logic decisions.**

Manufacture



- **Use model based or empirical process data to determine how many types of configurations are needed to achieve a maximum level of manufacturable degrees of freedom.**
- **Determine the possibility of composability rules that allow maximum variation-hardening.**
- **Investigate runtime efficient methods to perform RET in very regular designs**

Keep your friends close and your foes closer.

- IC manufacturers
  - — Specially true for fabless companies: Process does not differentiate enough a product.
    - – Focus on design for maximum benefit
    - – Consider variability for maximum predictability
- Vendors
  - — Industry-wide migration to fabless/foundry models is an opportunity to implement and deliver more streamlined design systems which are process aware.
- Academia
  - — The focus is no longer in feasibility of new technologies.
  - — The interest of Industry is in developing techniques to acknowledge variability and provide the most cost-effective design flow that meet product specifications.

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