Vertically Integrated Test/Calibration and Reliability Enhancement for Systems with RF/Analog Content

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Outline

- Trends and challenges they bring
- Post production calibration with a global view
- Defect-based screening
- Reliability modeling issues and reliability enhancement
- Vision

Trends

- Integration of digital, analog, RF subsystems
- Increasing process variations
- Increasing defect rates
- Reducing mean-time-to-failure
- Continuous optimization of processes for digital performance
- Increasing digital processing capability

Challenges for Analog/RF Circuits

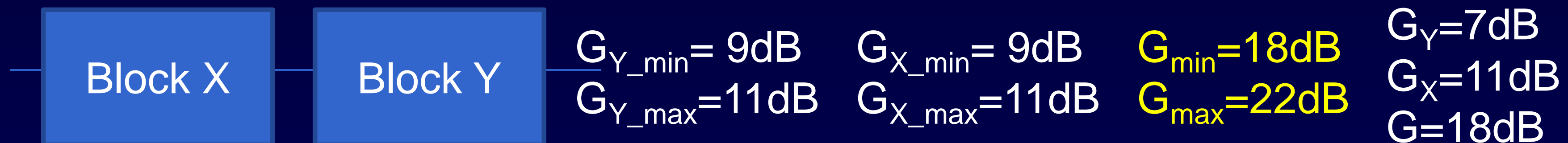
- Process variations introduce uncertainty into performance
  - Post-production calibration is necessary not just of high-resolution operations, but for all functionalities
- Increasing defectivity requires defect-based screening techniques
  - Screening techniques need to be analyzed in terms of defect coverage
- Continuous process optimization
  - Learned behavior and/or correlations need to be revised through product lifetime
- Reducing lifetime
  - Analog/RF subsystems may become single points of failure

Post-production Calibration

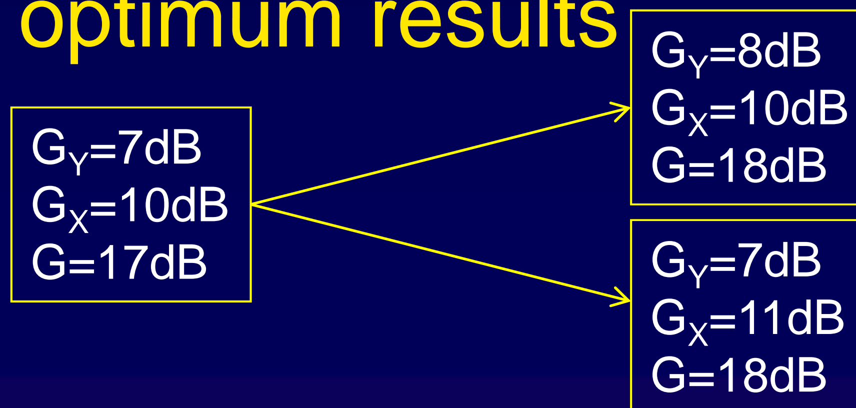
- Analog designers have been dealing with process variations
  - Many specific techniques exist to calibrate performance to within specifications
    - ADCs, PLLs
  - Few generally applicable techniques exist
    - Bias tuning with bias banks or DC voltage control
    - Bias tuning with negative feedback
    - Frequency tuning with banks of passive devices or voltage controlled passives
    - Adjustment of matching networks with capacitor tuning
    - Adjustment of transistor width
- Trade-offs almost always exist
  - Tuning for one performance parameter may degrade another one
  - e.g. gain vs. linearity or linearity vs. power consumption

Calibration in the Context of Complex Systems

- System is made up of many blocks, compensation effects need to be taken into account



- Local calibration may not always produce optimum results



Digital Processing

- With millions of transistors available, digital processing capability increases
- Digital compensation becomes more affordable
- Examples of digital compensation exist
  - e.g. pipelined ADCs
  - e.g. Compensation of IQ mismatch in transceivers
- Well, it is not free!
  - Processing capability is there but it most certainly has other uses
    - Computational overhead of compensation
  - Digital circuits are slow
    - Latency of compensation
  - Any additional operation adds power consumption
    - Yet another power/performance trade-off

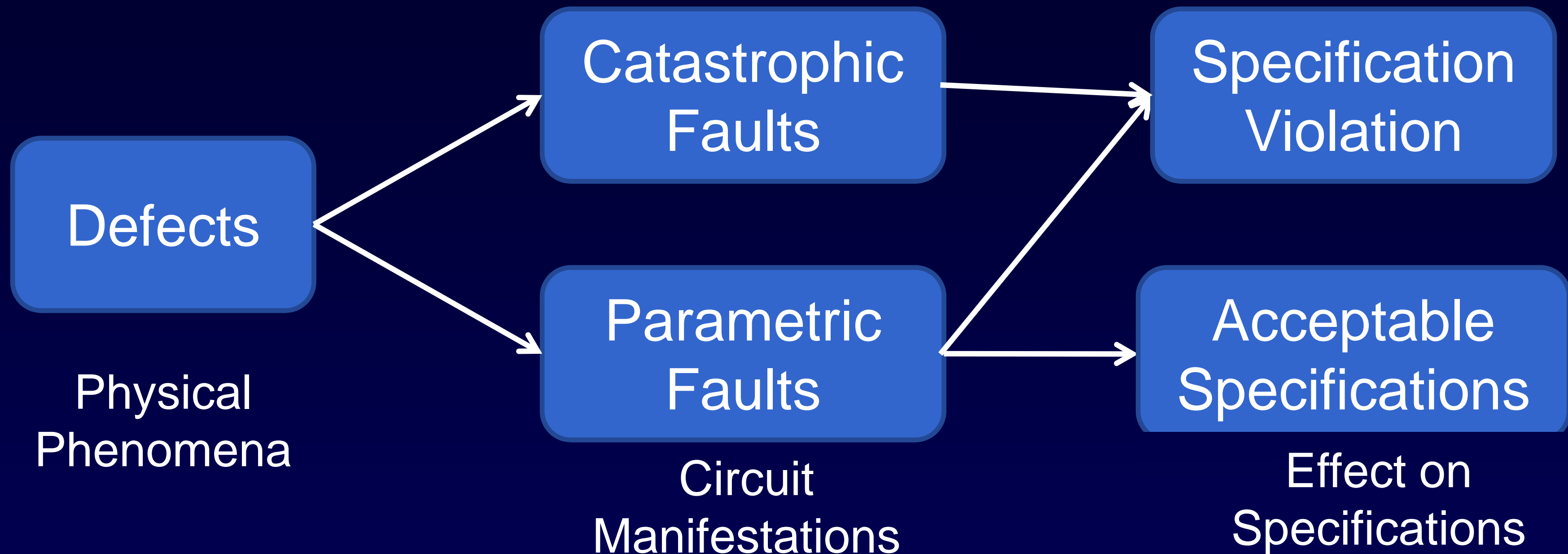
Calibration in the Context of Complex Systems

- Local calibration needs to work in conjunction with system-level optimization
  - Trade-offs of each calibration scheme
  - Trade-offs at the system level
  - Trade-offs and limits of digital compensation
  - Optimization process that decides what level of calibration and/or compensation

Increasing Defectivity

- Use of high-end digital processes for analog/RF circuits introduces higher defectivity
  - Hard defects
  - Parametric deviations beyond process tolerance

Defect Manifestation



- Most physical defects will result in complete loss of functionality
  - e.g. most open-circuit or short circuit defects that fall in the signal path
- Some defects result in a shift in the overall behavior
  - e.g. broken finger of a transistor
  - e.g. inductor coil shorts

How do defects affect the test process

- Traditional specification-based testing
  - If all specifications are measured, then there is no problem with *initial* quality
  - Almost certainly will not be the case
  - Test selection is typically based on learned statistical information
  - Defective circuits do not follow the statistics
  - Defect-based selection techniques are needed
- New techniques for testing
  - Techniques that rely on the measurement of correlated parameters (e.g. bias current, or DC voltages)
  - Techniques developed for BIST applications (e.g. sensor-based testing)
  - Techniques that rely on correlations among specifications (e.g. machine-learning based testing)
  - … need to be evaluated for defect response

Continuous Process Optimization

- Conclusions drawn from early samples (characterization data) may not be valid later on
- Adaptive test/calibration techniques are needed
  - Re-learn through process shifts
  - Mechanisms of learning need to be continuously refined

Reliability

- Not much attention has been paid to analog/RF circuit reliability
- Device reliability has been extensively studied
  - E.g. electromigration, oxide breakdown
  - Some research still needed for other analog components (inductors, capacitors)
- Existing aging models are generally based on digital circuits

Analog Circuit Wearout vs. Digital Circuit Wearout

- Using models and techniques from the digital domain is a start
- However, wearout patterns may be significantly different
  - constant bias vs. smaller stress on Vgs
    - Does this suggest electromigration is more of an issue than oxide breakdown?
  - Wearout is not uniform
    - e.g. RF choke in a power amplifier vs. input inductor in an LNA

Analog/RF Reliability

- Wearout monitors are needed
  – Local monitors
    - Bottom-up approach
    - Duplicating the operating conditions on critical components may be too costly (area, power)
    - Diagnosis is easy but monitoring is hard
  – System-level monitors with local diagnosis
    - Top-down approach
    - Analog diagnosis is very challenging but possible
    - Monitoring is easy but diagnosis is challenging

Reliability Enhancement

- Handle degradation in performance at the system level (compensation)
- Re-calibrate at the circuit-level
- Replace degraded unit
- Same issues?

Re-calibrating for Reliability Enhancement

- Can we use the same post-production calibration schemes?
- Sometimes, but not always
  - Calibration schemes may be counter-productive for reliability
  - e.g. LNA
    - Degradation of inductor $\Rightarrow$ reduced gain $\Rightarrow$ increase bias current $\Rightarrow$ faster degradation
- Need to perform system-level trade-off analysis
  - e.g. can we off-load some of the work of the degraded building block to another building block?

Replacement/Reconfiguration

- If degradation is beyond a certain level, replacement is needed
- Replacement of complete functionality is optimal from performance perspective
  - e.g. replace the complete receiver chain
  - But, costly in terms of hardware
- Replacement at the lower levels is possible
  - Loading, noise injection
  - How to turn off the component not being used?

Vision

- Research is needed at multiple levels of hierarchy
  - Circuit-level calibration
  - System-level compensation using digital computation
  - Defect-based testing and test evaluation
  - Reliability monitoring
  - Reliability enhancement
  - Re-configuration
  - Global optimization that takes all trade-offs into account