Doping of Atomic-scale Processed Materials and Devices:
a view from the present into the next decade

Michael Current

1. **A (very) brief look at roadmaps**
   Best taken with several grains of salt……
2. **Present day challenges for planar CMOS doping**
   Reduce defects by making *more* damage during implants…
3. **New metrologies for dopant activation, carrier mobility and leakage current**
   Two old ideas (Hall mobility and junction photo-voltage) revisited…
4. **Personal views on the characteristics of atomic-scale materials &switches**
   10 years out is a photonic world. The road is always long and winding…

Note: All data shown is in open literature.

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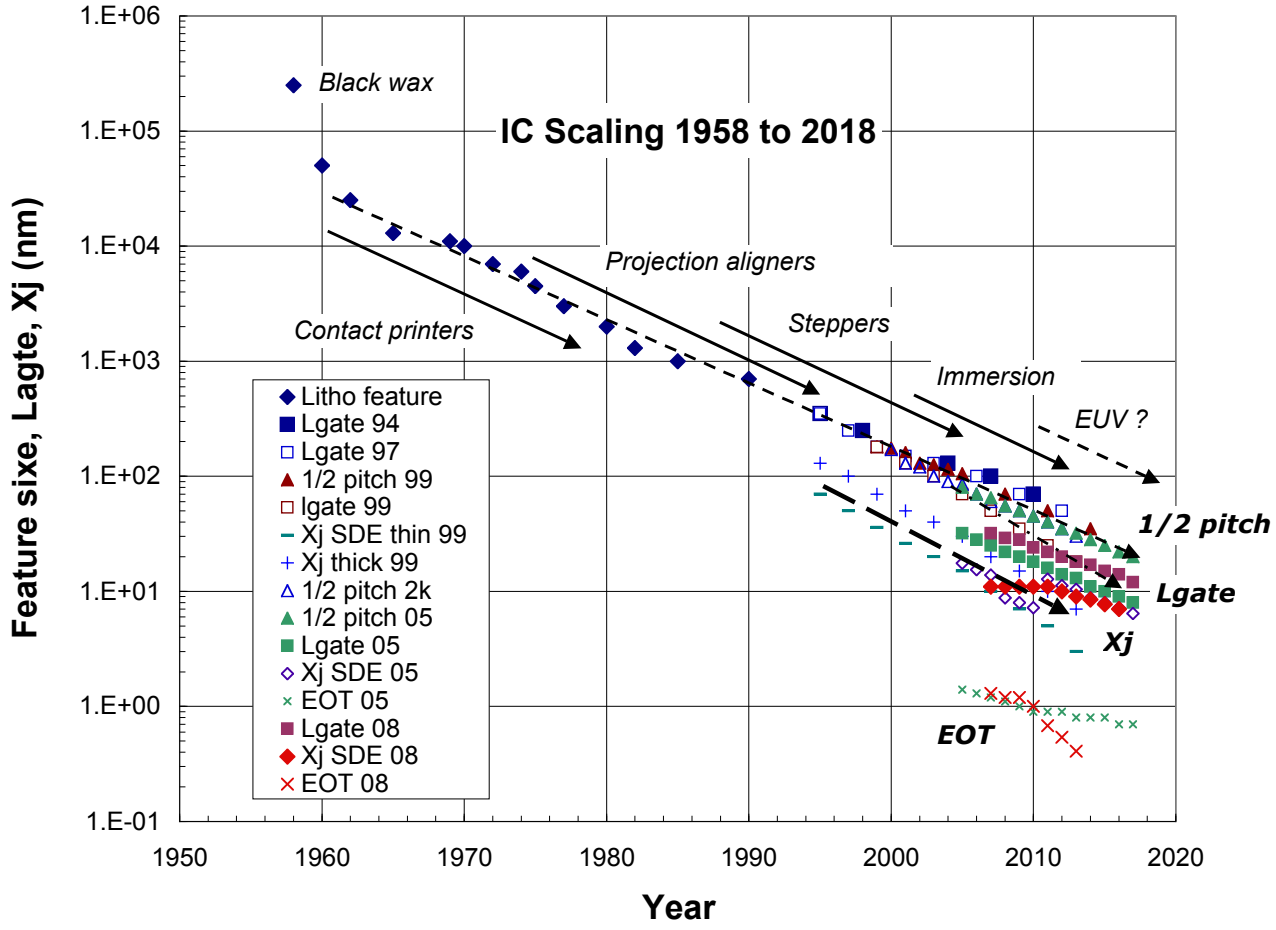
Roadmap Scaling:

60 years of exponential shrinks



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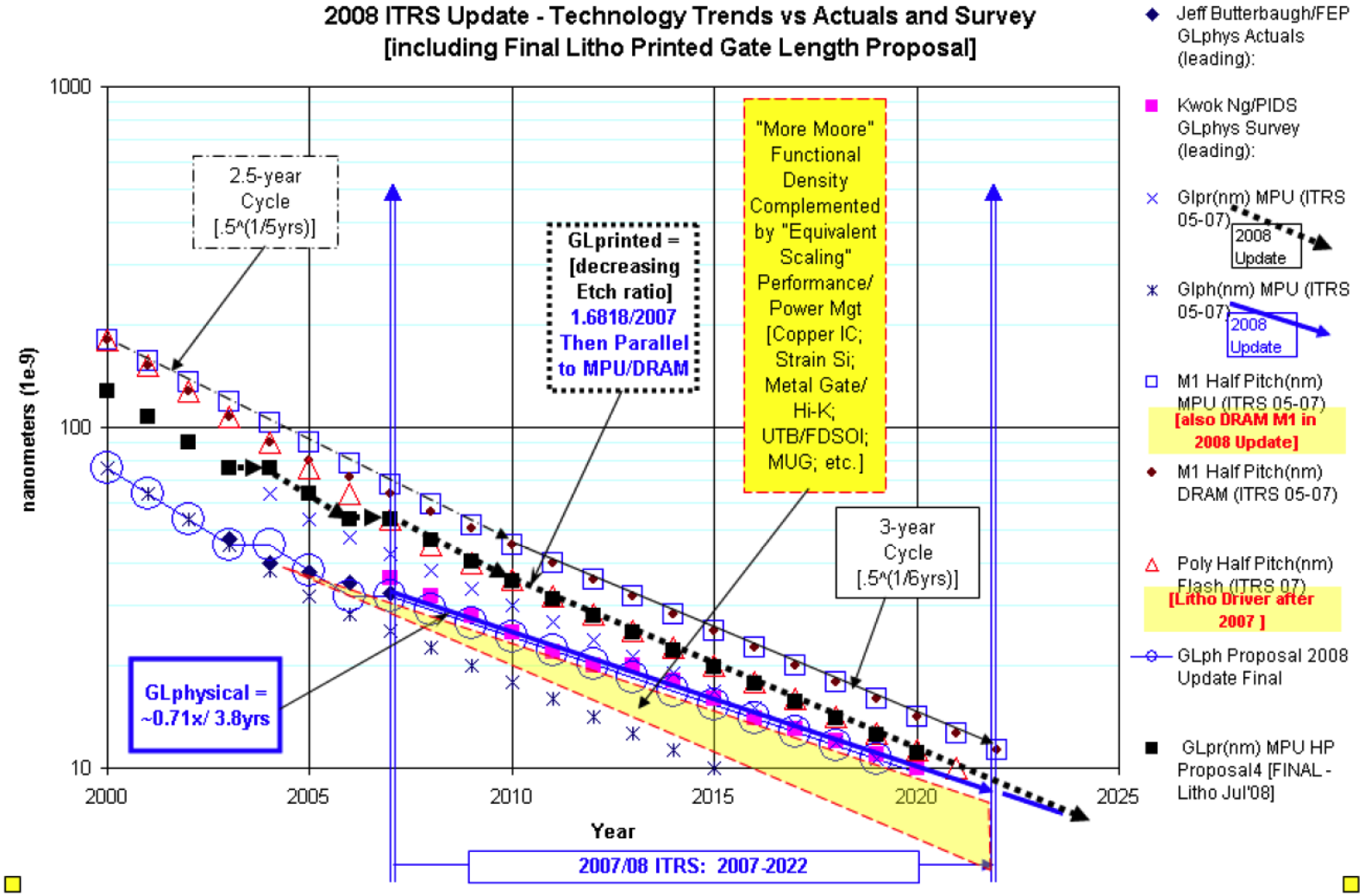
ITRS08 Update: SLOWER....



What Roadmap?

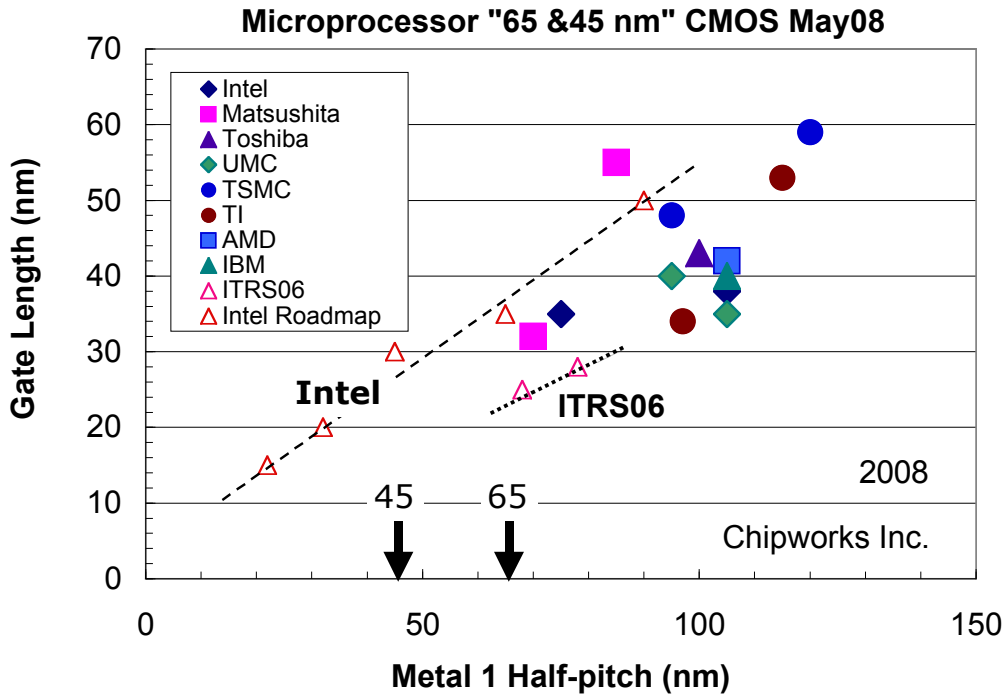
Everyone for themselves....

In the “real” world:

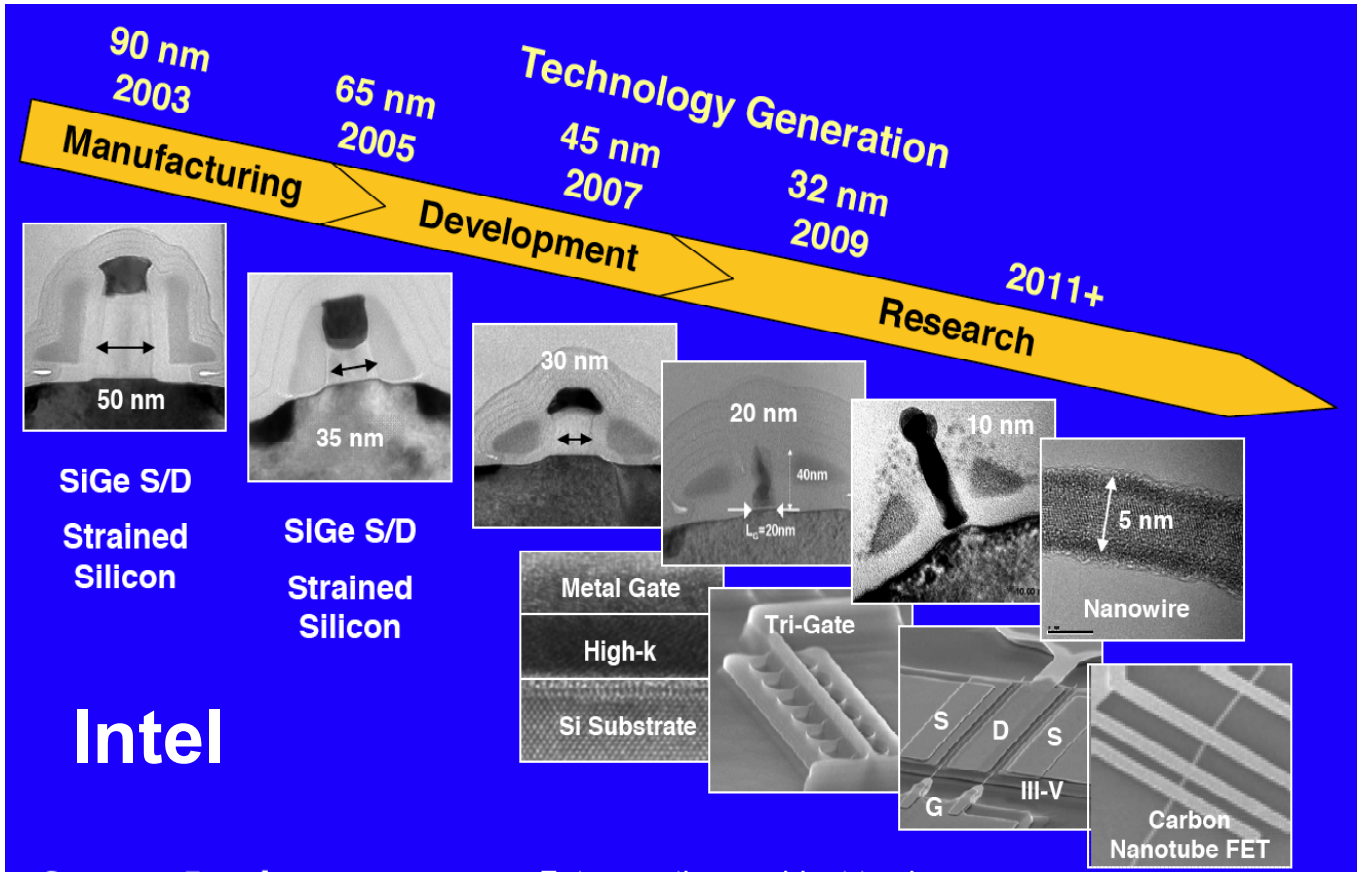
Metal pitch and gate length “lag” the labels.

Measured L_{gate} and metal pitch are only “loosely” correlated.

Individual product designs, not roadmaps, define MPU dimensions.

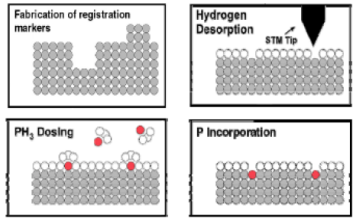


CMOS Roadmaps: Implementations & Options



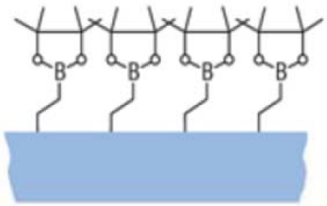
Deterministic Doping Options

STM Dopant Placement



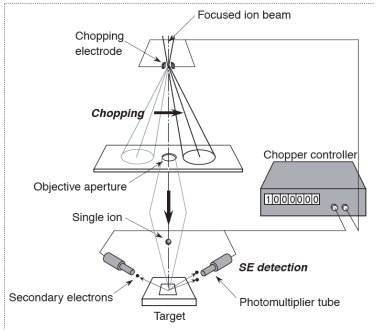
Simmons, UNSW

Monolayer Doping



Javey, UCB

Single Ion Implant



Shinada, Waseda

2010 Challenges to Planar CMOS Doping

Challenges:

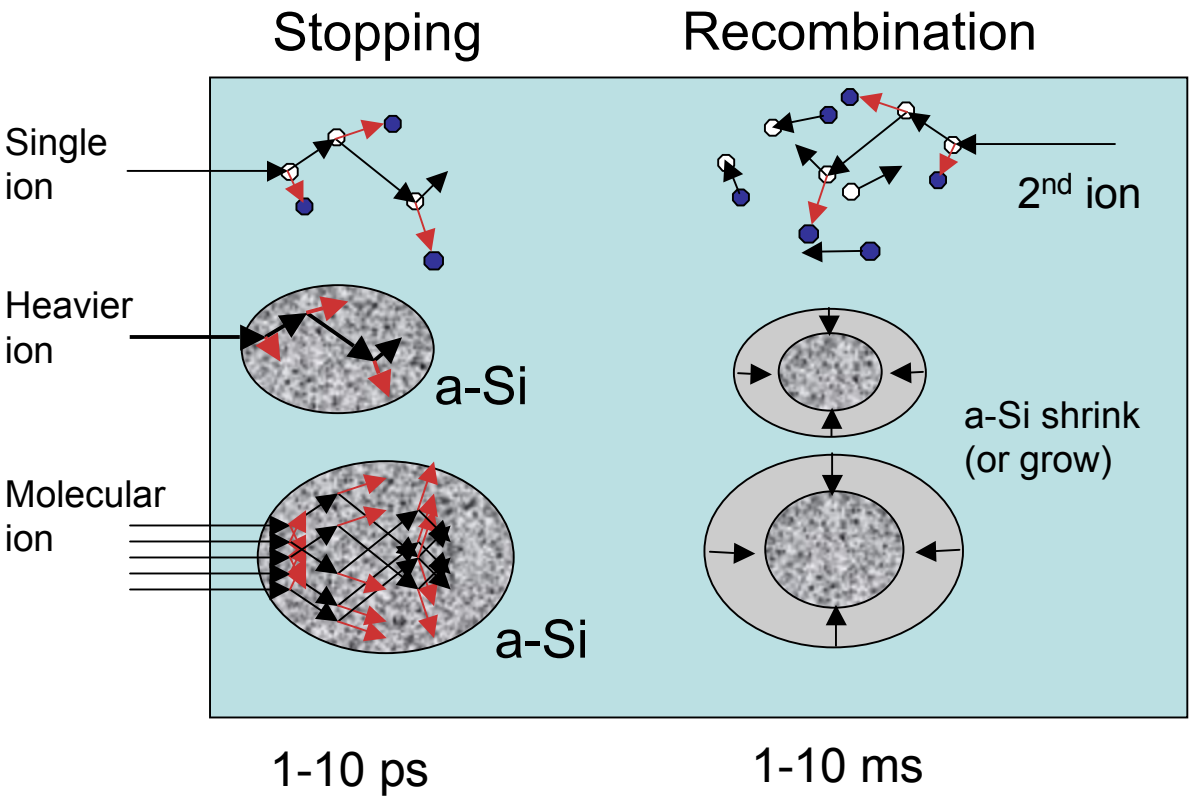
1. Enhance dopant activation in SDC, SDE and at metal contacts while scaling Xj <10 nm.
2. Reduce defect-driven contributions to junction leakage.

Active Areas of Innovation:

- Revisit the use of “cold” (-30 to -100 C) wafers to enhance damage accumulation during implant.
- Expand the use of large dopant count molecules ($B_{36}H_{44}$).
- New metrologies for carrier activation, mobility and junction leakage current.

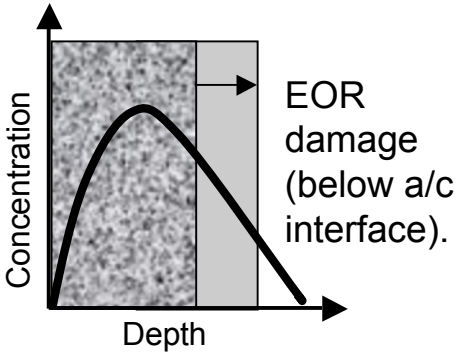
Enhanced Damage Accumulation:
Many Paths

Factors: *Ion mass, ion flux rate, multiple-atom ions, wafer temperature, energy/atom (for large, 10^4, clusters).*



Thicker a-Si layer:

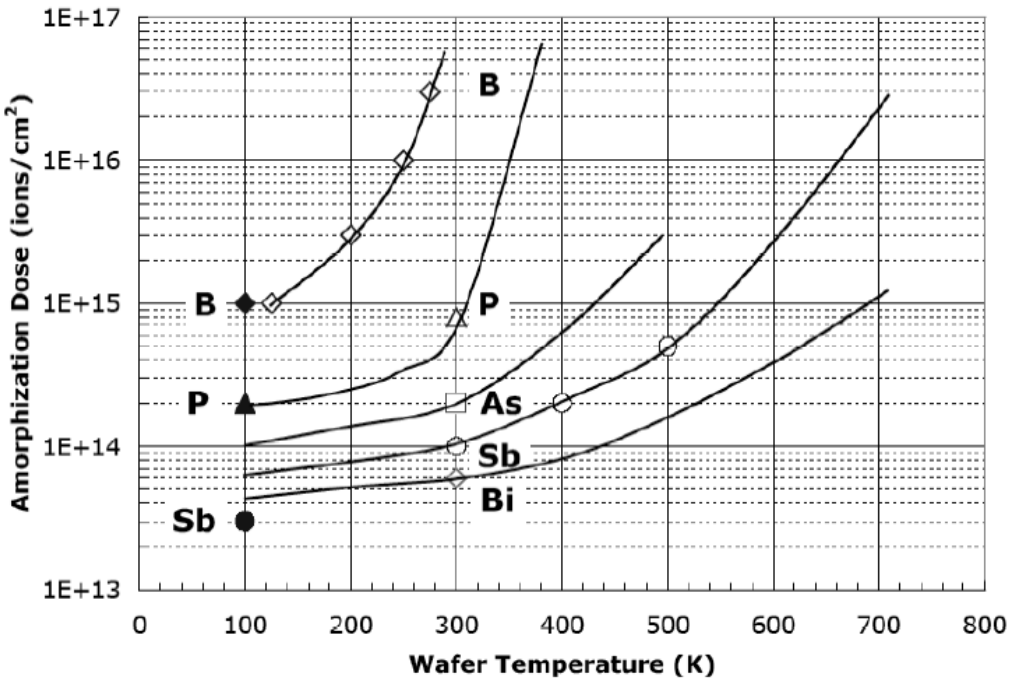
1. More dopants in a-Si (more active dopants after anneal).
2. Less deep damage (??) (less EOR damage after anneal = lower leakage (???).



Cryo-Implants: An idea from the '60's

Ion dose required to create an amorphous layer is lower for:

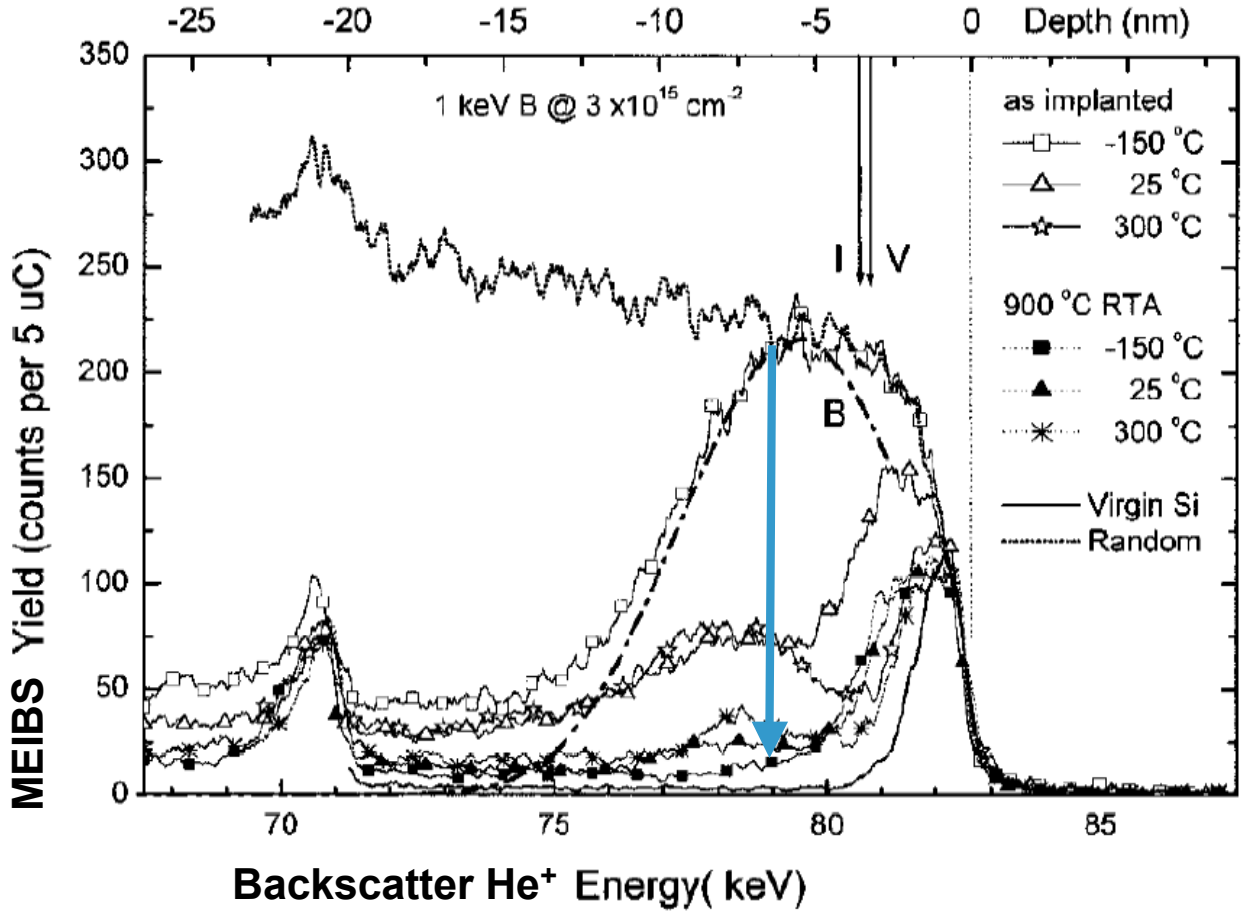
1. **Heavier ions** (denser damage cascades)
2. **Lower temperatures** (reduced defect diffusion and recombination during implant)
3. **Higher beam current density, slow scan rates** (not shown here).



Cryo-Implants: 1 keV B @ -150 C

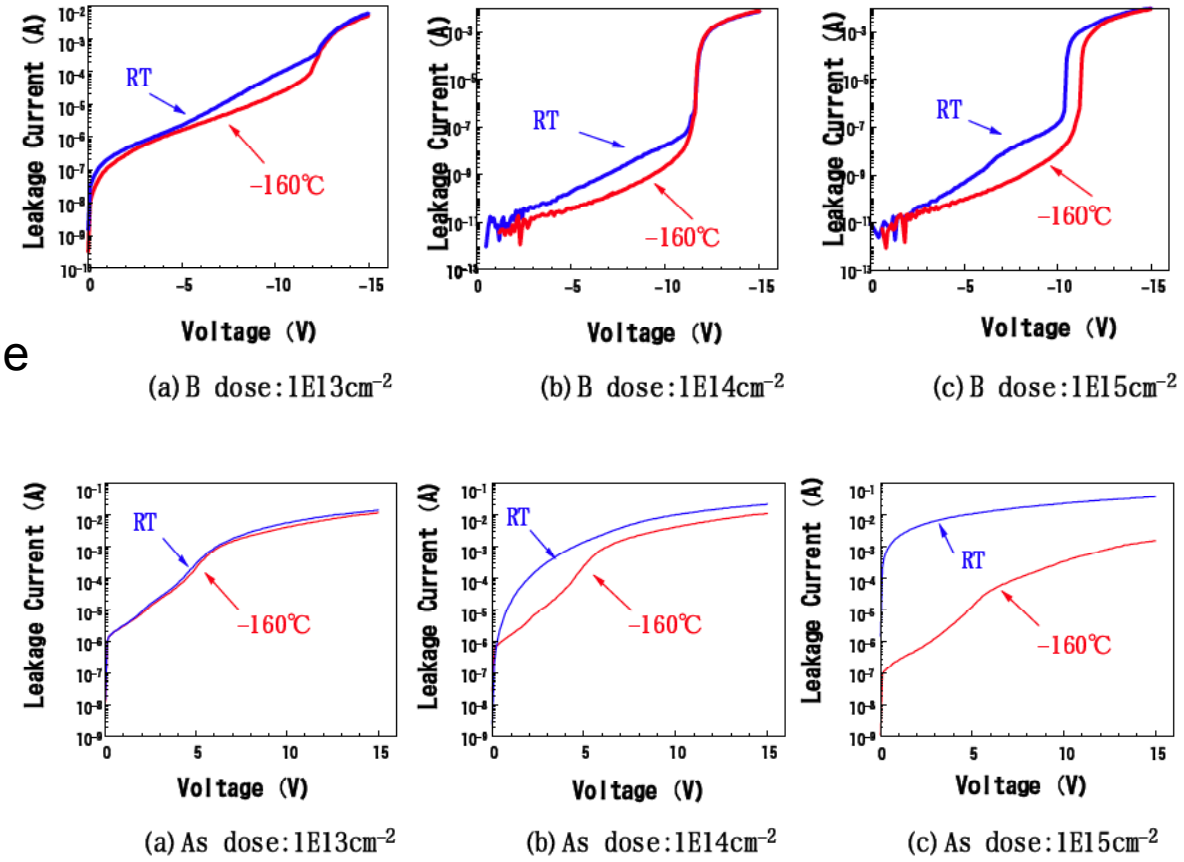
Deep a-Si layer with 1 keV B^+ at -150 C.

Low residual deep damage after RTA for -150 C implant.



Cryo-Implants: Diode Leakage: Toshiba, 2001

Low reverse bias leakage for -160 C implants



Leakage Current: Defects

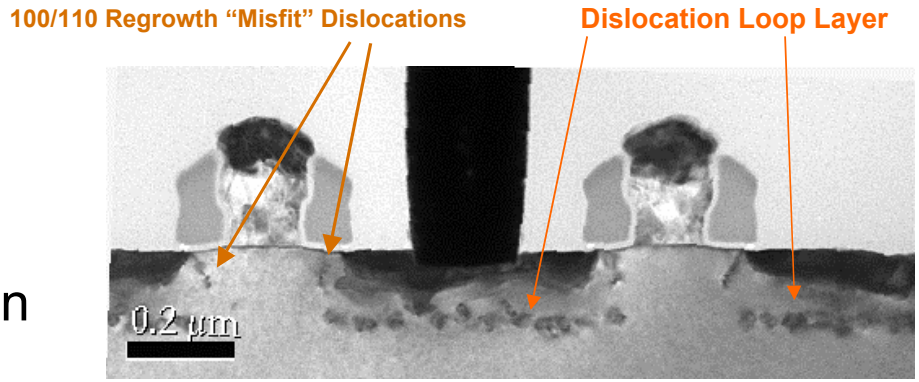
Defects in junction depletion zone drive process-related leakage.

Leakage Mechanisms:

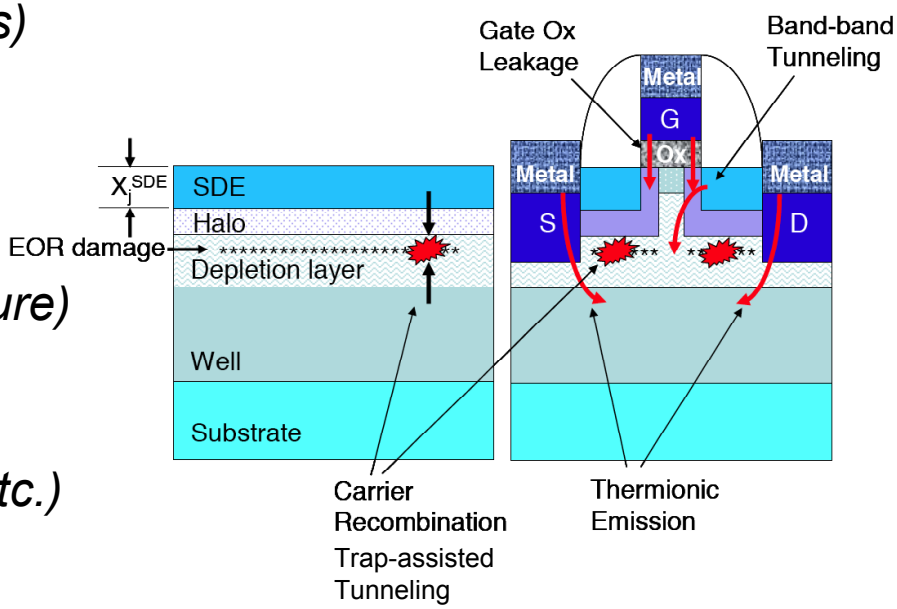
* Carrier recombination/generation *(Shockley-Read-Hall)*
* Trap-assisted tunneling *(TAT).*
* Band-to-Band tunneling *(reverse bias)*

Process Options:

* **Implant damage & sequences** *(ion type/energy/dose, beam current/scan rate/wafer temperature)*
* **Anneal conditions** *(peak temperature, time, ambient, temperature ramp rate, base temperature, etc.)*



XTEM Pentium Transistors (Courtesy of Intel)



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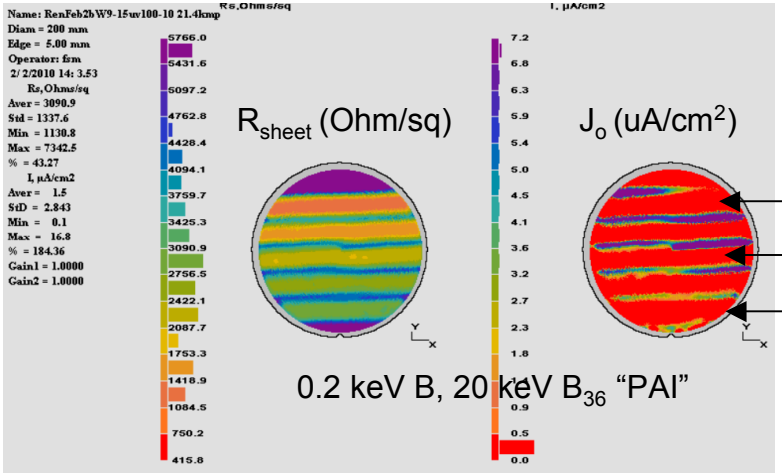
Deeper a-Si = Lower R_{sheet}

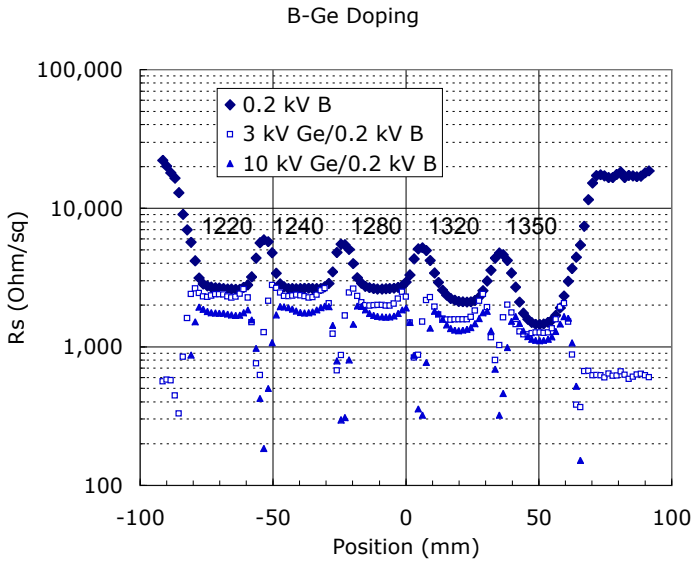
Deeper a-Si layers, in this case, by higher energy Ge PAI, gives:

lower R_{sheet}

but

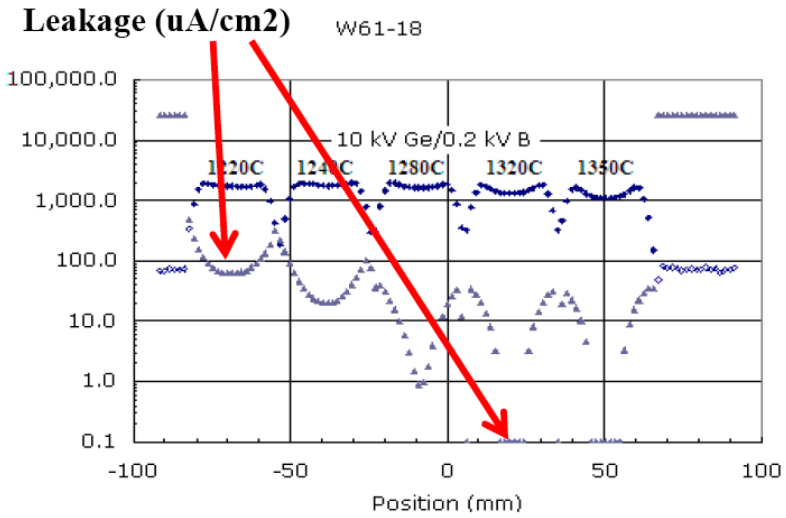
***higher* leakage current.**
(a common condition).



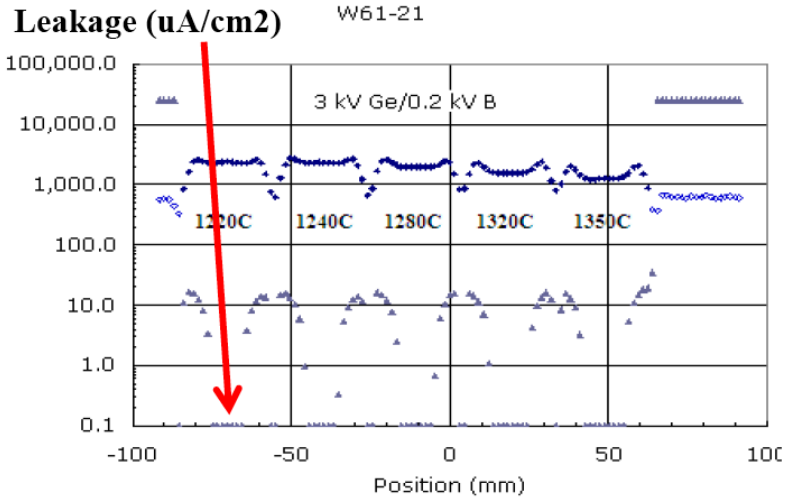


RsL Line Scans: Rs & Jo
0.2 keV B (and Ge PAI): no Halo

Deep (10 kV) Ge PAI has **much higher** leakage ***(x10^3)*** than shallow (3 keV) Ge.



Width of low leakage much thinner than good activation (Rs), implying intra-scan anneal temperature variations for laser anneal.



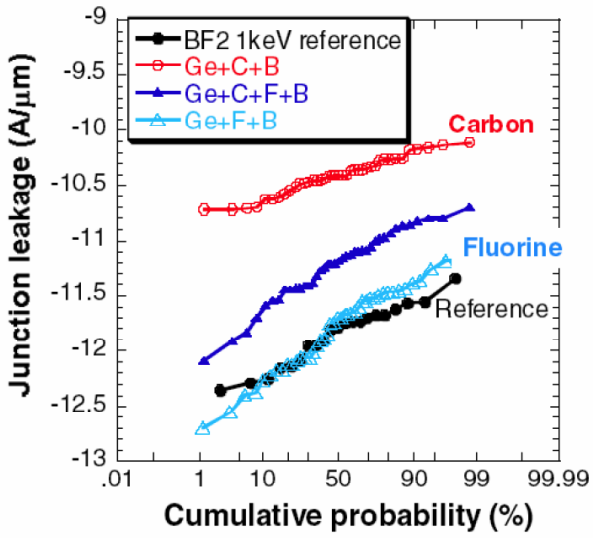
Leakage Current: Implant Ion Effects

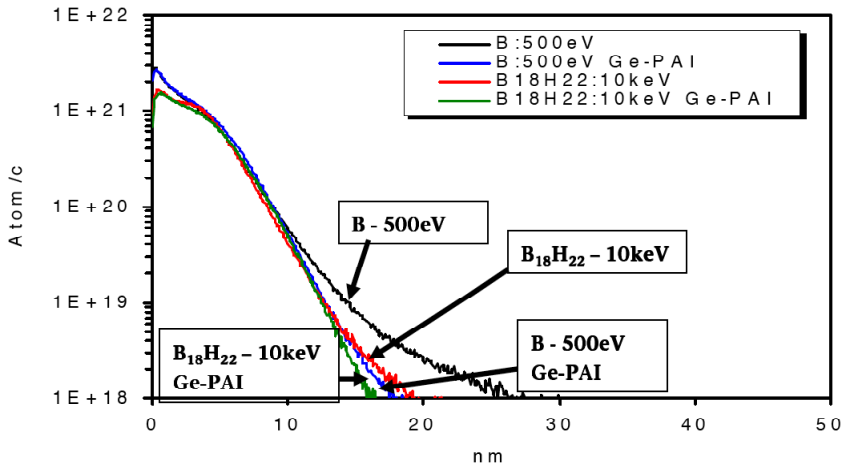
Specifics matter:

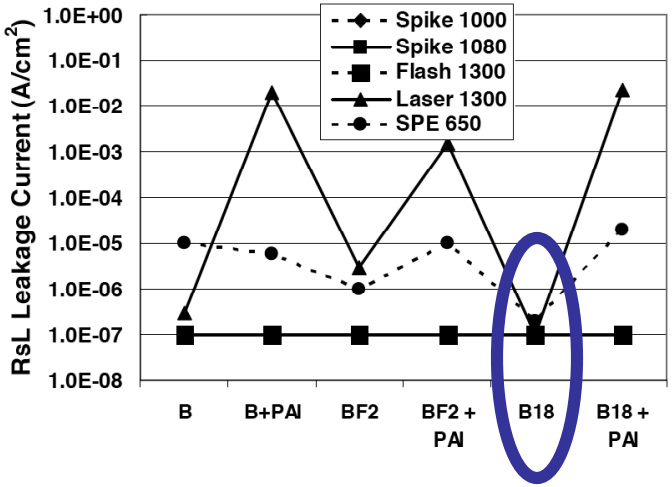
* Cocktail atoms at Xj (high leakage).
* C-defects have higher leakage than F.
* PAI leaves deep defects (high leakage).

Diffusion-less anneals (laser, flash, SPE) have higher risk of leakage than RTA.

Molecular ions (B_{10}, B_{18}), with no PAI, give low process-related leakage (shallow damage).



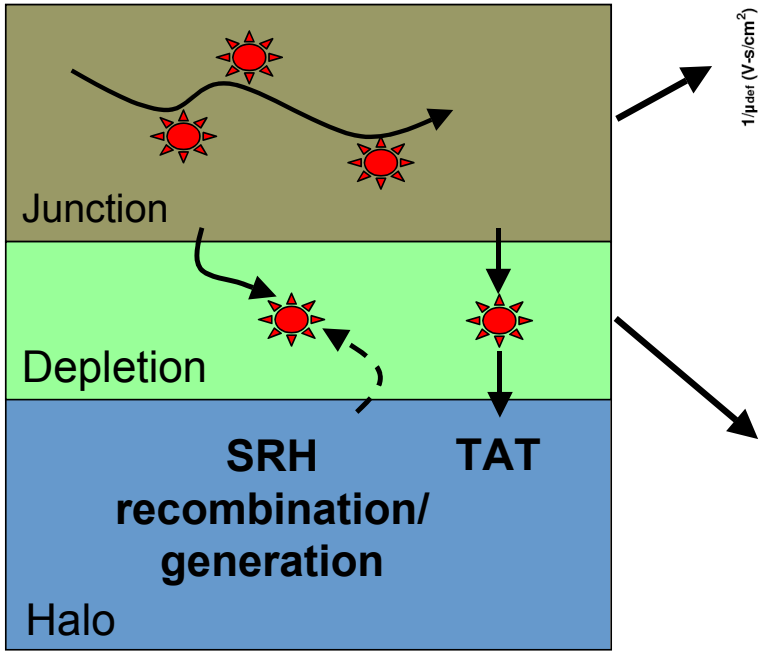


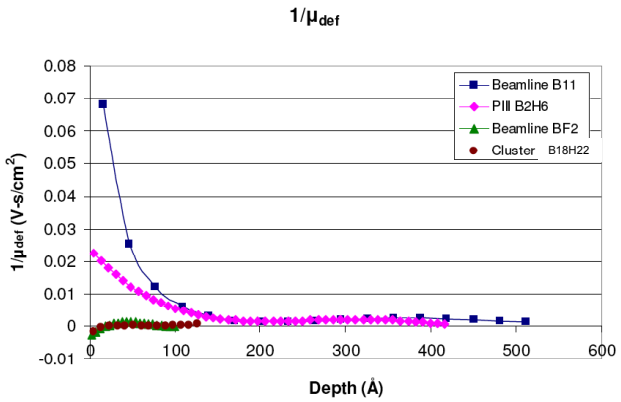


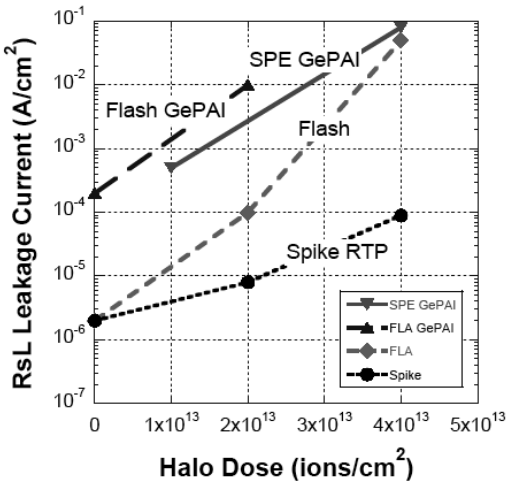
Summary Message: CMOS challenges

1. The quest for lower R_{sheet} and lower junction leakage for 10 nm Xj is now focused on **enhanced damage accumulation** (thicker, denser a-Si layers).
2. Dopants annealed along with a-Si layer regrowth have higher fraction of active dopants (lower resistivity and R_{sheet}).
3. Leading methods being worked on to enhance damage accumulation are:
    1. implants with large atom-count ions ($B_{18}H_{22}$, C_7H_7, As_4,etc.)
    2. implants at cryo (-30 to -100 C) wafer temperatures
    3. high ion flux rates (dense, slow scan beams, PIII).
4. ***Lessons learned may be useful in processing of atomic-scale processed materials.***

"New" Metrologies for Junction Defects
(Based on "old"ideas: Hall Effect and Photo-voltage)

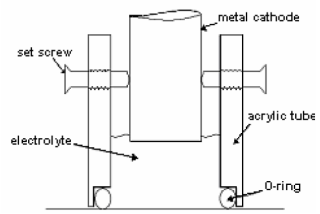






"New" Metrologies:1: Hall Profiling

1. **Automated Differential Hall Profiles** (using anodic oxidation).



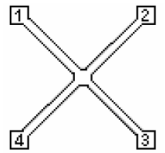


FIGURE 1

Measures:

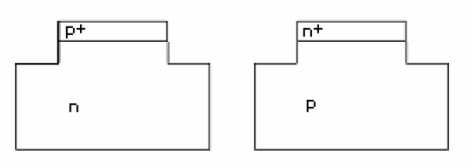
1. Resistivity (carrier concentration)
2. Hall mobility (dopants & defects)

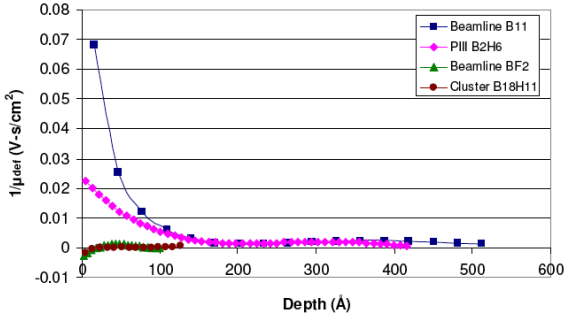
$$\frac{r}{\mu_H} = \frac{1}{\mu_o} + \frac{1}{\mu_{def}}$$

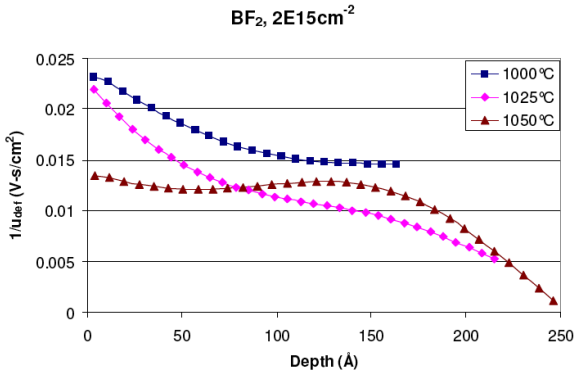
S. Prussin, UCLA M. Tanjyo, Nissin Ion

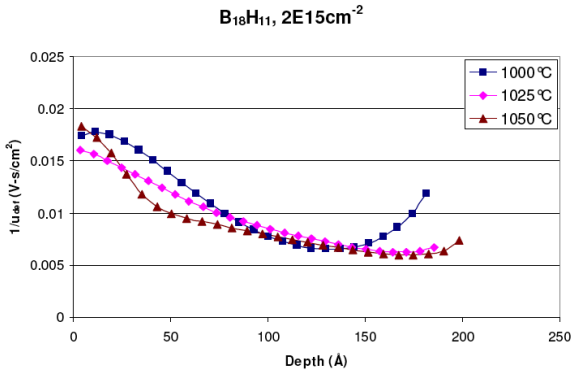
Si Prussin (left) @ RTP10

pru@ee.ucla.edu

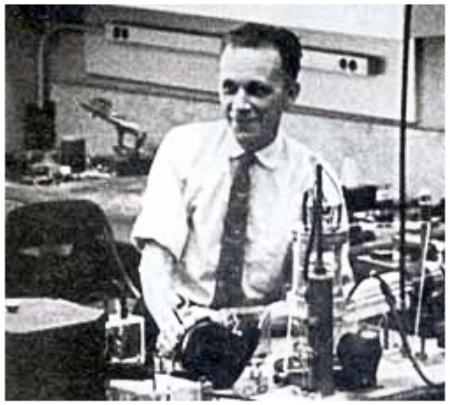








"New" Metrologies: 2
Photo-voltage for R_{sheet} and Leakage

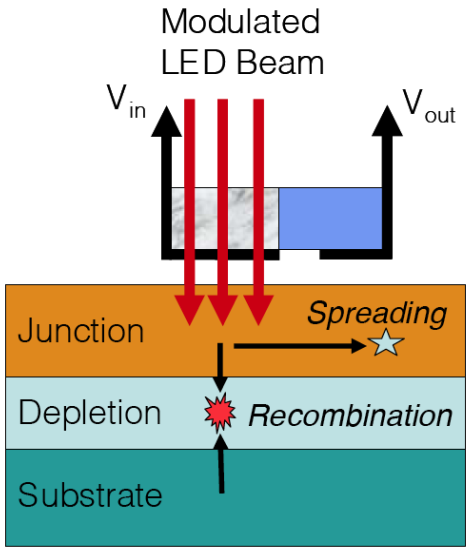


Russel Ohl @ Bell Labs 1940

pn junctions

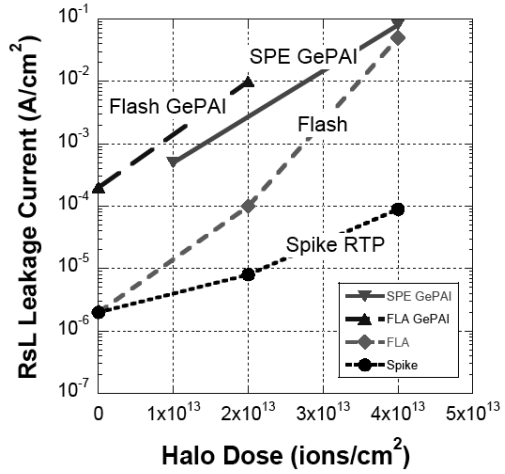
photo-voltage effect

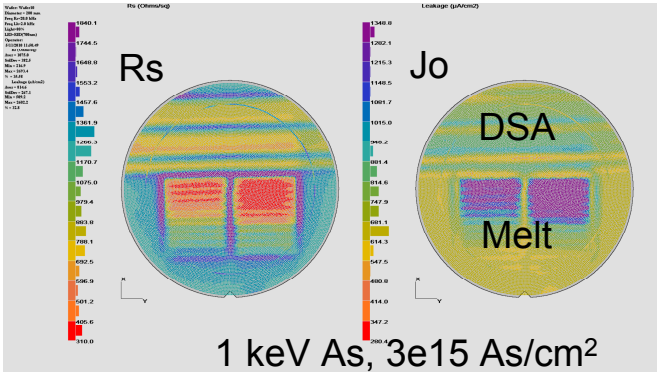
ion implant in 1950

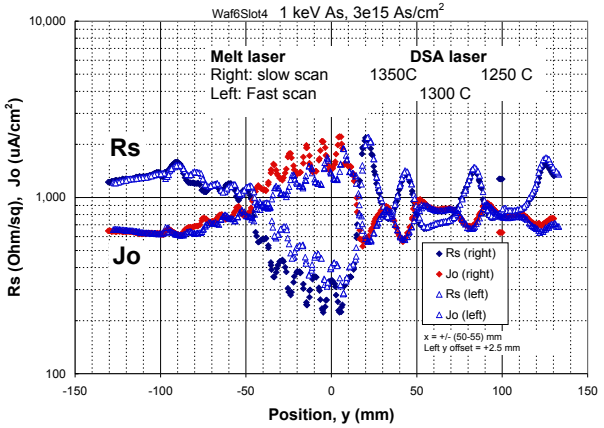


R_{sheet} (Ohm/sq)

Jo (A/cm²)







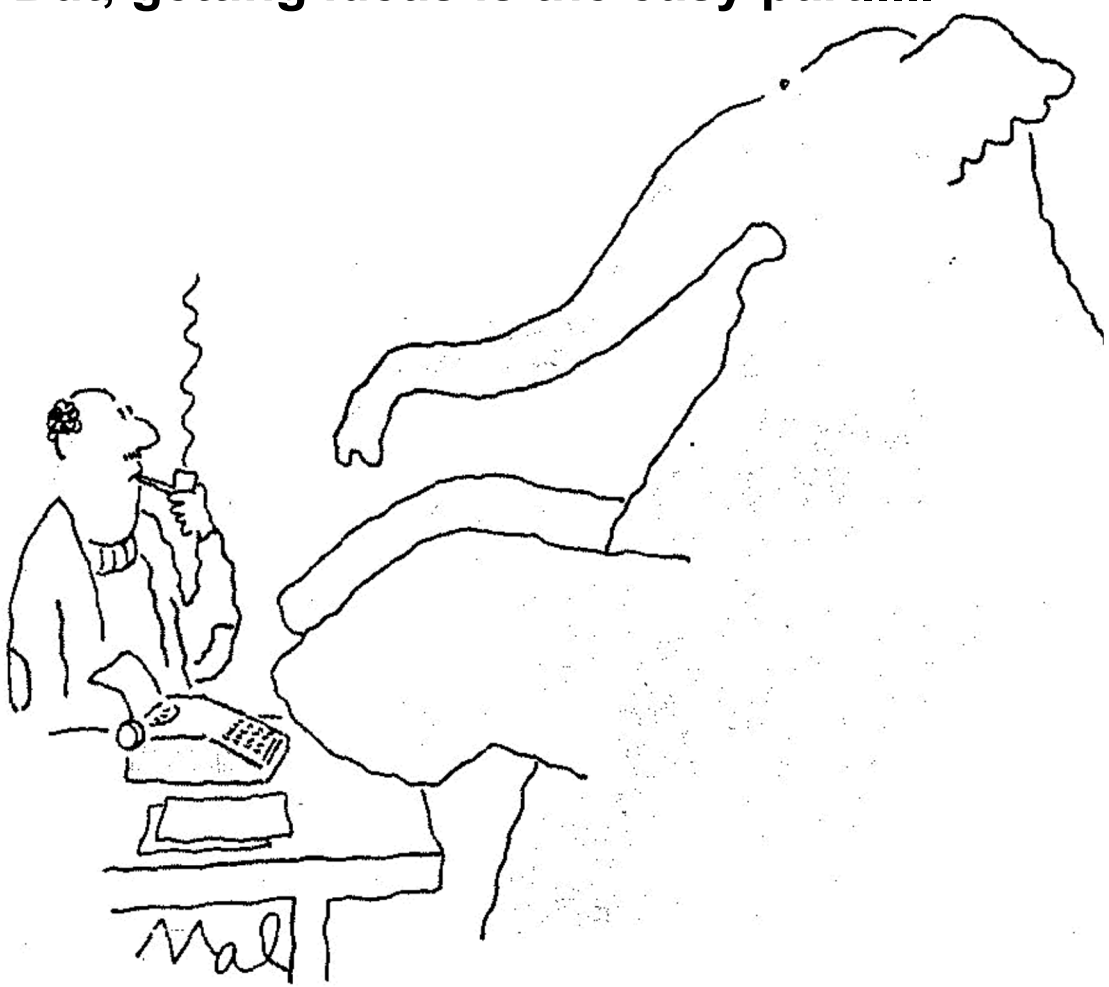
Summary Message: "New" Metrologies

1. New/old technologies are being developed to measure dopant activation, mobility (defect scattering) and junction leakage current. JPV metrologies are available from two commercial vendors. DHE is still a university (UCLA) tool.
2. Both metrologies need to be miniaturized for on-wafer (300 and 450 mm) probing. These and similar metrologies can play a role in evaluating *highly-ordered doping arrays* in junctions.
3. **Ways need to be found to fund and develop innovative metrologies for use with atomic-scale materials and devices.**

Overall Summary: A Personal View

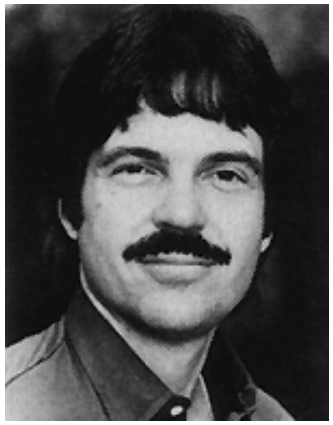
1. Materials specifications and proto-type device structures need to be developed and *articulated* to engage the inventiveness of the “doping” community.
2. Ways need to be found to develop (and fund) “radically innovative” metrologies to serve the evolution of atomic-scale processed materials ands devices.
3. Implantation will continue to become more selective and precise, with added focus on materials modification.
   Much like CVD has evolved towards ALD.
4. Any 10-year out “solution” needs to have devices that play well in the “photonic” world of integrated phonon and electron signal processing and communication.

But, getting ideas is the easy part.....



"Getting the ideas is easy . . . the hard part is hitting one key at a time."

Food for thought….



- GUI (Graphic User Interface)
- Smalltalk
- Laptop computers
- Object oriented programming

Alan Kay @ CHM 2009

"The best way to predict the future is to invent it."

Alan Kay, Xerox/PARC ~1971-81.

"Don't worry about what anybody else is going to do…
The best way to predict the future is to invent it.
Really smart people *with reasonable funding* can do just about anything that doesn't violate *too many* of Newton's Laws!"

Ion Implantation Process Engineering:

a practical textbook by M.I. Current

Preface: book scope, level, plan, commercial history of ion implant tool sales 1970 to 2007.
1. IC transistor doping basics:
Implant profile characteristics: depth, dose, profile shape, stopping (SRIM, TRIM-BASIC).
Damage accumulation, sputtering, sputter-limited dose, channeling
Masking basics: PR "economics", thickness, outgassing & carbonization, mask-edge effects
Principal doped regions for Bipolar-CMOS transistors
Roadmap trends for gate size, junction depth, channel doping, transistor speed, leakage
ULSI issues: channel doping and gate length fluctuations, poly-gate depletion,
"Ultimate" CMOS devices: FD-SOI, FinFET doping.
2. Ion implantation technology:
Evolution of basic system architecture
Ion sources (Freeman, Bernas, Button, RF/micro-wave)
Mass analysis, bend angles, resolution, source noise effects
Beam transport: emittance, perveance
Accelerator column design, beam scanning, decelerator electrodes
Wafer scanning geometries, beam incidence angle variations
Scanned area fraction vs beam size for x-y scan, spinning wheel, pendulum, ribbon beams
Faraday designs, single and multiple loop, noise & sampling ranges
Charge control systems: electron, ion & plasma flows
Throughput calculations; beam current, scanned area, wafer loading, beam tuning
Plasma immersion: sources, throughput, energy control, non-planar targets
3. Annealing:
Annealing effects: Damage annealing, electrical activation, diffusion
Furnace operations: push/pull, ambients, wafer strain effects/slip
RTP operations: temperature profiles, lamp pattern effects
ms-anneals: radiant energy coupling, surface temperature transients, stress/slip, laser scanning

4. Process characterization techniques
5. Dosimetry
6. Ultra-pure processing
7. Channeling
8. Charging
9. Damage accumulation and annealing
10. Operational efficiencies
11. Safety and environmental issues
12. Advanced topics: PIII, SOI, etc.

CD-ROM materials (options)
1. Safety: toxic, electrical, radiation, mechanical hazards
2. Ion source materials: ionization characteristics, etc.
3. Ion profile codes: guide to TRIM, TRIM-Dyn, SRIM, PRAL, UT-MARLOWE,
4. Short-course foils for major topics
5. Full-text and figures in pdf; text searchable.