Executive Summary

Title: Doping of atomic-scale processed materials and devices: a view from the present into the next decade
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Introduction

The continued success of doping technologies based on ion implantation and annealing to enable CMOS scaling over the last 3 decades has lead to a general feeling, among "road-mappers", that such continual progress is "automatic". The reality for transistor doping, as planar CMOS devices approach 22 nm characteristics, is that both implantation and annealing techniques face significant challenges. The general nature of these challenges; increasing dopant activation, controlling dopant diffusion and minimizing junction leakage current, are certain to remain relevant as transistor/switch design extends towards atomic-level materials and designs. New metrologies for characterization of junction leakage and defect contributions to carrier mobility can offer significant assistance for efforts to achieve atomic-scale devices.

The progress of selected topics over the past five years including your results

The present day challenges for implant-based doping technology include finding methods to increase dopant activation, as measured by junction sheet resistance, while minimizing defect-driven leakage current factors. The most active fronts in this effort are focused on methods to enhance the damage accumulation during implantation for SD extension and contact doping through the use of high dopant count molecular ($B_{36}H_{44}$) ions and/or use of cryogenic (-30 to –100 C) wafer temperatures during implantation. The active areas in the complementary activities for annealing include work on low thermal budget processing by ms-timescale energy pulses from flash lamps and lasers as well as investigations of very low (<500 C) thermal processing with micro-wave radiation.

Beyond the central role of implantation and annealing technologies for doping, the use of non-dopant ions for materials modification of ICs is increasing towards 1/3 of the implant process steps in a modern CMOS flow. These applications start from Ge implants for amorphization, C implants for diffusion controls and PR hardening implants to improve line edge definition towards new applications such as high-dose C implants (with molecular ions) to set up nMOS channel tensile strain. One can expect the number of these materials modification applications to increase as a wider range of films and structures are incorporated into CMOS processing and that the lessons learned will be instructive in the quest for atomic-scale switches.

Another area of recent innovation that can prove useful going forward is the development of metrologies focused on defect effects on junction leakage and carrier mobility. Two complementary methods are particularly relevant for the development of high-activation, low-leakage shallow junctions.

The first is the revitalization of differential Hall effect (DHE) measurements, where high-precision depth profiling is achieved by anodic oxidation of the junction surface between measurements (S. Prussin et al., IIT10 and RTP10). Comparisons of the defect scattering contribution to carrier mobility in the junction show clear effects of the choice of implantation methods (single ion beamline, plasma immersion (PIII) and molecular ($B_{18}H_{22}$) ions) (Fig. 1, upper right). Systematic studies of other doping conditions can guide the choice of implant and anneal technologies aimed at increasing dopant activation and minimizing junction resistance.

The second technique uses the recently developed methods for analyzing junction photo-voltage (JPV) measurements to provide non-contact measurements of sheet resistance (through carrier spreading between two capacitor electrodes) and junction leakage (through analysis of JPV dependence on light modulation frequency). Junction leakage measurements track the effect of defect sites below the junction interface, in the depletion layer. In its present commercial embodiment, R_{sheet} maps have been demonstrated with sub-mm resolution (M. Current et al., IIT08).

Further development of both DHE and RsL towards minimization of probe size, using MEMS-based techniques, needed for product-wafer probing on 450 mm wafers, can also be directed towards use in evaluation of atomic-scale processed materials.

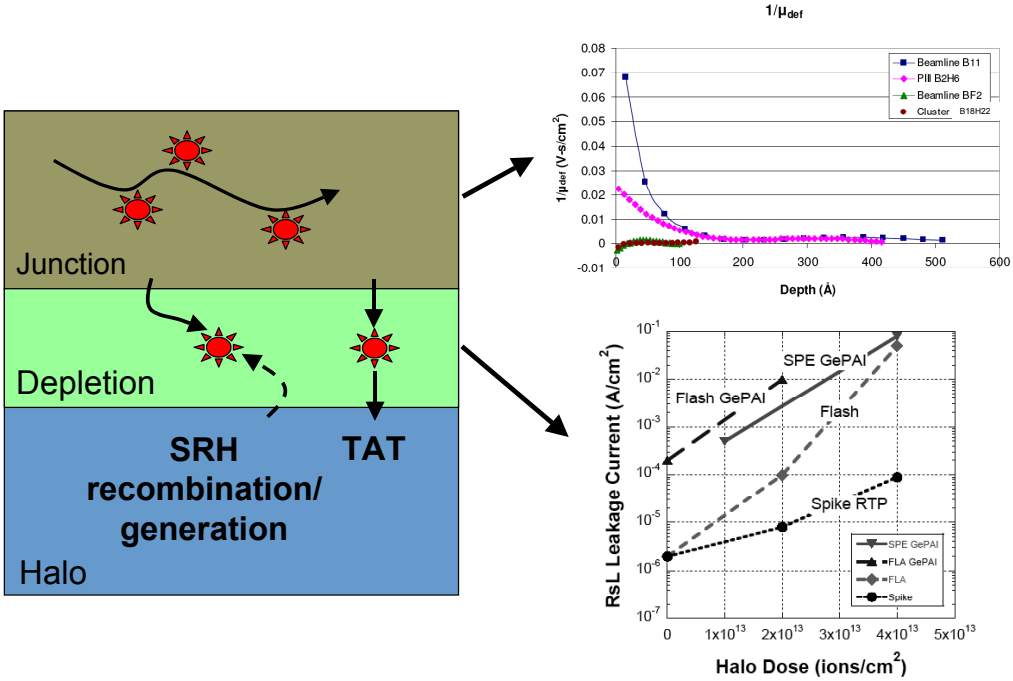

Figure 1. Cartoon of a p-n junction (left) including depletion layer and halo doping and defect scattering profile data from DHE (upper right) and photo-voltage (RsL) leakage (lower right) measurements. Defect centers are indicated by "stars".

Potential application opportunities, if possible (What is the potential impact on ITRS?)

The implant and annealing community, and its associated group of metrology developers, continue to provide vigorous and inventive responses to recognized challenges. But the challenges need to be defined and recognized.

Of particular value to the "doping community" from this SRC group (and others) would be an evolving articulation of the materials goals and definition of proto-type device structures (with specific doping and materials properties) along the path towards atomic-level designed materials and devices.

A parallel effort should also be found to encourage development of suitable metrology methods to provide characterization data from atomic-level processed materials and structures. Of particular importance is the development of radically innovative metrology methods to deal with the specific needs of these new materials and devices as they are developed and pushed towards large-scale fabrication.

The difficult challenges and potential solutions for the next 10 – 15 years

My personal view is that any range of "solutions" looking out 10 years or more must include a significant amount of integration of electronic and light-based signal processing and communication. The development of atomic-scale switches, a major focus of this SRC workshop, should keep an eye towards exploiting properties that play well in "photonic" systems.

And, certainly with a 10 year span to consider, one can expect ion implantation methods to evolve to be more selective and precise, along the analogous evolution of CVD to ALD processing…and beyond.

As Alan Kay famously wrote in 1971, "Don't worry about what anybody else is going to do… The best way to predict the future is to invent it. Really smart people with reasonable funding can do just about anything that doesn't violate too many of Newton's Laws! "