Executive Summary

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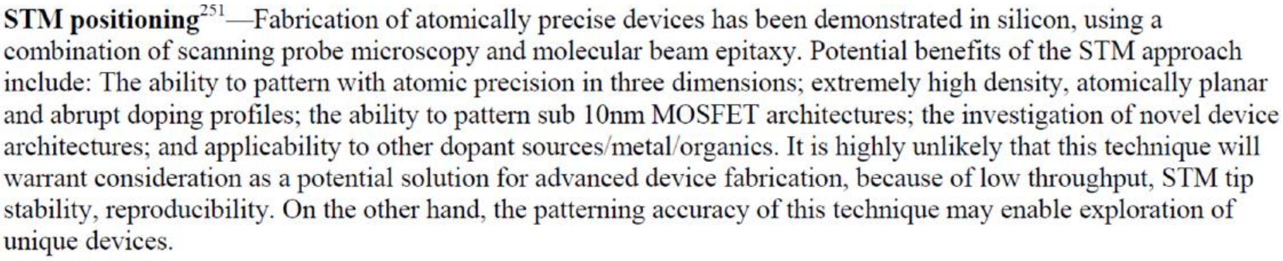
Introduction



STM positioning[251]—Fabrication of atomically precise devices has been demonstrated in silicon, using a combination of scanning probe microscopy and molecular beam epitaxy. Potential benefits of the STM approach include: The ability to pattern with atomic precision in three dimensions; extremely high density, atomically planar and abrupt doping profiles; the ability to pattern sub 10nm MOSFET architectures; the investigation of novel device architectures; and applicability to other dopant sources/metal/organics. It is highly unlikely that this technique will warrant consideration as a potential solution for advanced device fabrication, because of low throughput, STM tip stability, reproducibility. On the other hand, the patterning accuracy of this technique may enable exploration of unique devices.

From the 2009 ITRS roadmap STM positioning was identified as state-of-the-art for dopant positioning. Whilst not yet manufacturable, this technique allows investigation of atomically abrupt, highly doped, shallow source and drain junctions with gate lengths less than 10nm; junctions resistances of ≤1KΩ/□; junction depths down to 5nm and lateral junction abruptness of ~0.2 nm/decade. It also allows the fabrication of unique device architectures in silicon with atomic precision in all three dimensions and singl dopant architecture for electron spin based qubits.

The progress of selected topics over the past five years including your results

Within the field of STM positioning of dopants Prof. Simmons has led a large experimental team that has demonstrated a unique strategy for the fabrication of electronic devices in silicon with atomic precision. Using a combination of scanning tunneling microscopy (STM), phosphine as a gaseous dopant source and molecular beam epitaxy (MBE) her group have been able to controllably place P dopant atoms in Si devices with atomic precision. With ~100 papers in the past 6 years her group leads this field internationally. Key highlights include:

- The demonstration that single phosphorus (dopant) atoms can be positioned into silicon with atomic precision (*Phys. Rev. Lett.* ***91****, 136104 (2003)*; *Phys. Rev. Lett.* ***93****, 226102 (2004)).*
- The demonstration of a method to make reliable electrical contacts to buried STM-patterned source/drain and gate regions (*Nano Letters* ***4 (10)****, 1969 (2004).*
- The demonstration of the versatility of this technique to produce a range of devices at the nanoscale, including: simple tunnel junction transistors (*Physical Review B* ***75****, 121303(R) (2007)*), single electron transistors (*Small*, ***3***, *563 (2007)*) and ordered dopant arrays (*IEEE Transactions on Nanotechnology*, ***6*** *(2), 213-217 (2007)*).
- The demonstration that this technology can produce the narrowest conducting wires in silicon to be used as local in-plane epitaxial gates for qubit architectures (*Small*, ***3***, *563 (2007); Nano Letters* ***9,*** *707 (2009)).*
- The demonstration of electrical transport through STM-patterned few donor (*Nature Nanotechnology* 5, 502 2010) and most recently single P atoms in Si.

This work has the potential to realise a scalable silicon-based quantum computer and all epitaxial 3D transistor architectures.

Potential application opportunities, if possible (What is the potential impact on ITRS?)

The key benefit of this technology is that it allows the investigation of planar transistor with atomically abrupt, shallow source-drain junctions that meet all the requirements of the 2021 year of production. It also allows the investigation of novel device architectures at the atomic-scale.

The difficult challenges and potential solutions for the next 10 – 15 years

Challenges in STM-based technology long term are to turn this into a manufacturing technology. This requires the formation of stable STM tips, feedback control patterning and reduced patterning times. Research in our group along with international collaborators is currently addressing these issues.

Experts and expertise with references

STM lithography:

J.W. Lyding: Appl. Phys. Lett. 64, 2010 (1994)

J.N. Randall: Microelectronic Engineering 87, 955 (2010).

Device concepts:

B.E. Kane: Nature 393, 133 (1998).

J.R. Tucker: G. Qian, Y. Cung-Chang and J.R. Tucker, Phys. Rev. B 71, 045309 (2005).

V.V. Zhirnov: IEEE Transactions on semiconductor manufacturing 15, 157 (2002).

Monolayer Doping:

J.C. Ho: Nano Letters 9, 725 (2009).

S.McKibbin: Appl. Phys. Lett. 95, 233111 (2009)

K.E.J. Goh: Phys. Rev. B 73, 035401 (2006)