# Executive Summary

Title: Doapnt Activation in Si and Ge by Low Temperature Microwave Anneal

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## Introduction

For the state-of-the-art CMOSFETs technology, the junction depth and resistivity of source and drain regions of critical important to the development of the aggressively scaled CMOS technology for short channel effect control and high devices performance. Therefore, as considering these two simultaneous concerns of the source/drain concentration level and reducing the junction depth for ultra shallow junctions, a lower temperature anneal process is necessary. In addition, mobility enhancement techniques are also required for breakthrough the scaling limit of CMOSFETs. Since the mobility of Ge is 2x for electron and 4x for hole. The results after anneal on the SiGe or pure Ge substrate are very important. First of all, by using a low-temperature microwave anneal, one could suppress the sheet resistance and prevent the boron from diffusion and expansion on the $Si/Si_{0.2}Ge_{0.8}/Si$ substrate, as shown in Fig. 1. This would not induce any dislocations or defects at the interface of the $Si/Si_{0.2}Ge_{0.8}/Si$ heterogeneous substrate, as shown in Fig. 2 [1]

On the other hand, $P^{31}$ activation in the pure Ge film by conventional anneal would be companied with serious diffusion. Therefore, $P^{31}$ in germanium epitaxy atop Si wafer by low temperature microwave annealing technique was also investigated in this study. This work has demonstrated that $P^{31}$ in single crystalline germanium thin films can be activated and the dopant diffusion could also suppressed by low temperature microwave anneal technique. By SIMS and SRP analysis, as shown in Figs. 3-4, radiation damage caused during implantation process could be repaired by microwave annealing and the severe dopant diffusion could be suppressed due to the lower temperature process as compared with conventional RTA process [2].

Furthermore, strained Si by global or local stress could also enhance the channel mobility. That by capping $SiN_x$ to enhance the device mobility is a low-cost material and easier fabricates process for strained Si or SiGe channel. Rapid thermal annealing (RTA) and microwave annealing (M.A.) for the $SiN_x$ film strain enhancement are compared in our studies. Using microwave annealing, the Rs could attain to 94.5Ω/sq. ($P^{31}$ at 15KeV with a dose of $5\times10^{15}$ $cm^{-2}$) and dopant diffusion could be also suppressed as compared with those by using high temperature RTA. In addition, $SiN_x$ films processed by low temperature M.A. depict higher tensile stress, as summarized in table 1. The characteristics of diffusionless dopant distribution and higher tensile stress $SiN_x$ film would be useful in contact etch-stop layer (CESL) or stress memorization technique (SMT) in the fabrication of small pitch nano-scaled nMOSFETs [3]. More microwave power would enhance the tensile strain, effectively, but the strain eventually becomes saturated, as shown in Fig. 5. Low temperature annealing can expand the potential application of contact etch-stop layer (CESL) or stress memorization technique (SMT) in lower heatproof materials or high-K/metal gate process.

Finally, nanoscale p-MOS TFTs with a TiN gate electrode were realized using a novel microwave dopant activation technique. We compared both low-temperature microwave annealing and rapid thermal annealing (RTA), as shown in Figs. 6. We successfully activated the source/drain region and suppressed the short-channel effects using low temperature microwave annealing. This technique is promising from the viewpoint of realizing high-performance and low-cost upper-layer nanoscale transistors required for low temperature 3D-IC fabrication. Different dopant activation conditions are compared for various annealing techniques. The punch-through characteristics and short channel effect were suppressed by using a low-temperature microwave dopant activation technique, as demonstrated for nanoscale gate p-MOS TFTs.

References:

[1] **Yao-Jen Lee**, Fu-Kuo Hsueh, Shih-Chiang Huang, Jeff M. Kowalski, Jeff E. Kowalski, Alex T.Y. Cheng, Ann Koo, Guang-li Luo, and Ching-Yi Wu," A Low-Temperature Microwave Anneal Process for Boron-Doped Ultra-Thin Ge Epi-Layer on Si Substrate," IEEE Electron Device Letters, vol.30, no.2, pp.123-125, 2009

[2] Yu-Lun Lu, Zheng-Chang Mu, Fu-Kuo Hsueh, Tz-Yen Cheng ,**Yao-Jen Lee** , Tien-Sheng Chao, and Ching-Yi Wu," Dopant Activation in Single Crystalline Germanium by Low Temperature Microwave Annealing," submitted to EDL

[3] **Yao-Jen Lee**, Shang-Shiun Chuang, Fu-Kuo Hsueh, Ho-Ming Lin, Shich-Chuang Wu, and Ching-Yi Wu,"Nanoscale p-MOS Thin-Film Transistor with TiN Gate Electrode Fabricated by Low-Temperature Microwave Dopant Activation," accepted by EDL

[4] Yu-Lun Lu, Fu-Kuo Hsueh, Kuo-Ching Huang, Tz-Yen Cheng, Jeff M. Kowalski, Jeff E. Kowalski, **Yao-Jen Lee**, Tien-Sheng Chao, and Ching-Yi Wu,"Nanoscale p-MOS Thin-Film Transistor with TiN Gate Electrode Fabricated by Low-Temperature Microwave Dopant Activation," IEEE Electron Device Letters, vol.31, no.5, pp.437-439, 2010

[5] **Yao-Jen Lee**, Yu-Lun Lu, Fu-Kuo Hsueh, Kuo-Chin Huang, Chia-Chen Wan, Tz-Yen Cheng,Ming-Hung Han, Jeff M. Kowalski, Jeff E. Kowalski, Dawei Heh, Hsi-Ta Chuang, Yiming Li,Tien-Sheng Chao, Ching-Yi Wu, and Fu-Liang Yang,"3D 65nm CMOS with 320°C Microwave Dopant Activation," reported in the 2009 IEDM , USA (Dec.7~9, 2009)

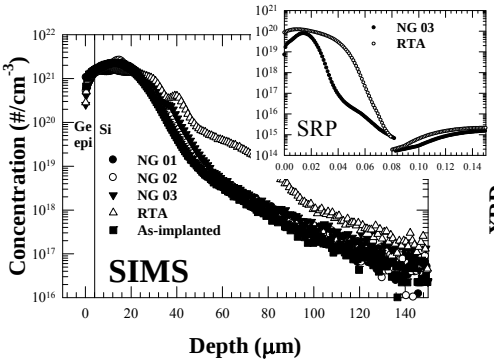


Fig. 1. The SIMS profile of boron concentration. The boron distribution after the RTA of 900 °C for 30 seconds depicts a deeper boron distribution. The insert in Fig. 1 is the carrier concentration, which indicates the profile of dopant activation concentration, measured by SRP for the splits of NG03 and RTA.

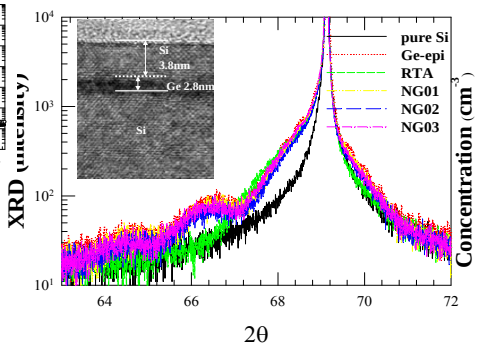


Fig. 2 High-resolution double-crystal symmetrical ω/2θ scans of Ge-epi layers and planar Si substrate. The inset in Fig. 2 is a TEM image of the split of NG03, and the structure consists of Si/Ge/Si layers, with the thicknesses of Ge and Si capping layers as 3.8 and 2.8 nm, respectively.

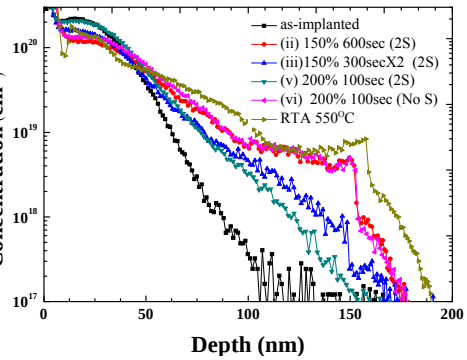


Fig. 3 SIMS profiles of implanted P in Ge before and after microwave annealing in different conditions and RTA at 550°C for 60 seconds.

| Anneal type | Max. Temperature (°C) | Initial strain (Gpa) | After anneal (Gpa) | Sheet resistance (Ω/sq.) |
|---|---|---|---|---|
| M.A. 3P. 600s | 493 | Tensile (0.287) | Tensile (1.68) | 94.53 |
| | | Compressive (-0.113) | Tensile (1.228) | |
| M.A. 3P. 100s | 420 | Tensile (0.321) | Tensile (0.944) | 102.6 |
| | | Compressive (-0.114) | Tensile (1.024) | |
| M.A. 3P. 100s by 6 cycles | 420 | Tensile (0.321) | Tensile (1.51) | 94.47 |
| | | Compressive (-0.114) | Tensile (1.31) | |
| RTA 900°C 30s | 900 | Tensile (0.32) | Tensile (1.57) | 56.78 |
| | | Compressive (-0.154) | Tensile (1.6) | |
| Spike 1000°C | 1000 | Tensile (0.133) | Tensile (1.645) | 66 |
| | | Compressive (-0.081) | Tensile (1.571) | |

Table 1 Comparisons of the characteristics of $SiN_x$ film strain and Rs by M.A. and RTA

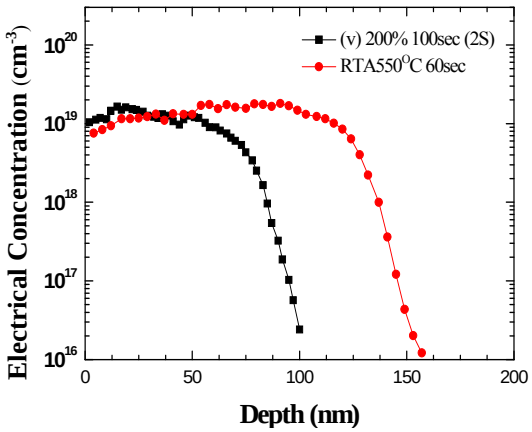


Fig. 4 SRP depth profiles of $P^{31}$ in Ge from sample (v) and RTA.

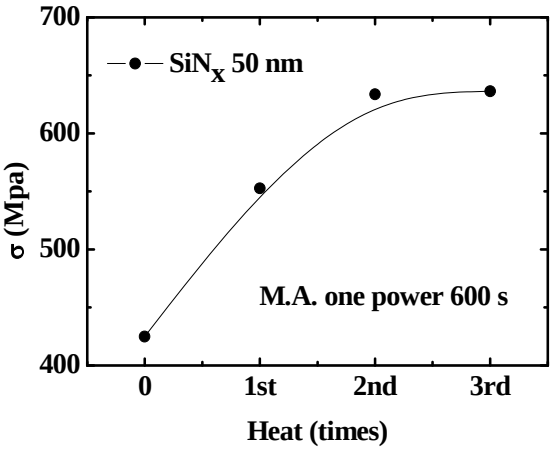


Fig. 5 50nm $SiN_x$ thickness, microwave power is 600~700W. The strain magnitude becomes saturated.

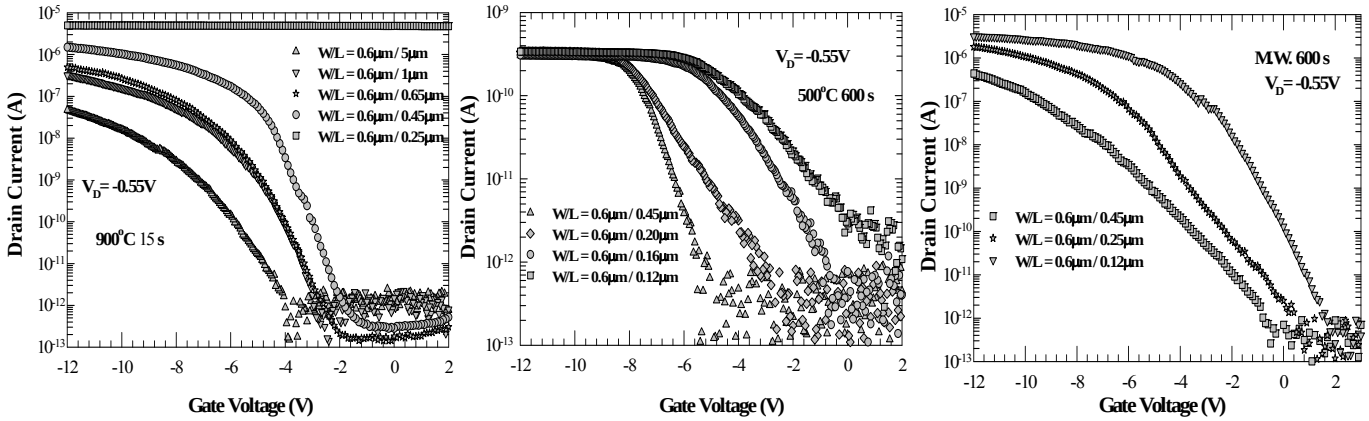


Fig. 6 Discussion of characteristics ($I_D$-$V_G$) of p-MOS TFTs was annealed by RTA and microwave annealing. (a) RTA at 900°C for 15 s, and (b) furnace at 500°C for 500 s. (c) microwave annealing for 600 s. In (a) as the gate length is below 0.2 μm, punch-through effect dominants the transfer characteristics, and in (c) the $I_{on}/I_{off}$ ratios are about $10^8$ for p-MOS using microwave anneal for 600 s with W/L = 60nm / 120nm.

The progress of selected topics over the past five years including your results

1. Nano-scaled CMOS-TFTs fabrication.
2. Low temperature dopant activation in Ge film
3. SiNx film tensile strain enhancement by low temperature microwave anneal

Potential application opportunities, if possible (What is the potential impact on ITRS?)

1. Low temperature dopant activation in ($P^{31}$, As, and B) in Si, SiGe, and Ge substrate.
2. Ultra-thin silicide formation.
3. Nano-scaled poly-Si TFTs fabrications.

The difficult challenges and potential solutions for the next 10 – 15 years

1. Workfunction shift of metal gate after anneal?
2. Defect density after ion implantation and anneal.
3. Uniformity impacted by metal gate density.

Experts and expertise with references

1. T. L. Alford, K. Sivaramakrishnan, and A. Indluru," T. L. Alford, K. Sivaramakrishnan, and A. Indluru," Mater. Res. Soc. Symp. Proc. Vol. 1245
2. E. L. Pankratov,"Redistribution of dopant during microwave annealing of a multilayer structure for production *p−n* junction," JOURNAL OF APPLIED PHYSICS 103, 064320 (2008)
3. Keith Thompson, John H. Booske, and Reid F. Cooper," Electromagnetic Fast Firing for Ultrashallow Junction Formation," IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING, VOL. 16, NO. 3, AUGUST 2003