Transport metrology for ultra-scaled MOSFETs

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I INTRODUCTION

Modern transistors get so small that it is increasingly difficult to use traditional techniques for their study and their characterization. Different groups have recently investigated the effects of ultra-scaling in silicon Field Effect Transistors (FETs) geometries [1-7] and results of extreme interest have emerged. In particular:

-M. T. Björk *et al* [1] have shown that the decrease of doped silicon wires radius can cause substantial increase on the ionization energy of the dopant and this has profound implications for the design of future FETs.

-M. Pierre *et al* [2] and Wacquez *et al* [3] have shown that the presence of a single dopant in the channel dramatically influences electrical characteristics even at room temperature. As a consequence of this, the possible use of orbital atomic (valley) degrees of freedom for new quantum logic functionalities has been suggested [2-5] and demonstrated [4].

-M. Fueschsle *et al* [6] have studied the peculiar effects that arise on bands of single-crystal silicon structures in which the source, the drain and the gates are fabricated using an atomically sharp doping procedure [6] and the consequences of ultra-scaling are taken at the extreme limits. Therefore these authors have also evidenced the importance of the valley degree of freedom in CMOS devices.

-M. Tabe *et al* [7] have demonstrated that, even in the presence of a dopant rich environment, it is possible to observe effects having the single dopant signature.

Overall these recent studies have all allowed the better quantification of the knowledge necessary for the design of future CMOS devices while approaching the ultimate single atom transistor limit [3-11]. Furthermore, these new findings could allow the implementation of not yet envisaged concepts of logic [4,5]. Following these lines of research, we have developed several methods that can be used for a better understanding of the transport mechanisms in FinFETs and to demonstrate atomic impurity metrology [5,8-11]. In fact, as from one side [5], through correlation of experimental data with multimillion atom simulations in NEMO 3-D, the impurity's chemical species can be identified and their concentration, local electric field and depth below the Si/SiO_2 interface can be determined. From another side, the extension of the dopants in the source/drain (S/D) regions can be measured by spectroscopy of confined states in the channel. Finally, the effective cross section of the channel can be determined by mean of thermionic emission theory [10] that reflects the evolution of the effective channel cross section at different gate voltages (V_G) in undoped FinFETs. Therefore, a new set of metrology techniques to be used for ultra-scaled CMOS devices has been developed.

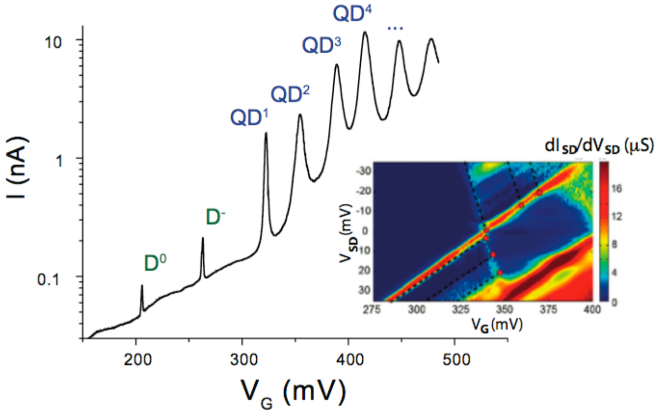

Figure 1. Coulomb blocked transport in a FinFET transistor. Two separate charge islands can exist inside the transistor; a quantum dot confined by the triangular potential at the gate interface and residual barriers in the access regions between source/drain and channel and a donor/well system confined by the donors Coulomb potential and a well at the interface [5]. QD^n and D^0/D^- denote the localized states formed in these charge islands respectively. Inset: Stability diagram with the typical diamond-shaped region associated with Coulomb-blocked transport between the D^0 and D^-.

The FinFET devices used in this study are fabricated at IMEC [12]. Transport measurements on an ensemble of devices at a temperature of 4 K are performed in order to search for the fingerprints of isolated donors diffused from source and/or drain contacts. A single donor's fingerprint is characterized by a pair of resonances in the I_{SD} versus V_G characteristics at low V_{SD}. While we almost always find a quantum dot (QD) [13] in the channel [8-

9], only about one out of seven devices has an isolated donors fingerprint. The positive identification of the single donor resonances is based in the determined binding energy, charging energy and the odd-even spin filling [8]. Next, the excited energy levels of the one-electron (D^0)-state are determined by sweeping both the V_G and V_{SD} biases and by measuring the differential conductance [10] in the appropriate bias space. In this so-called stability diagram (see inset Fig. 1), the typical diamond-shaped region associated with Coulomb-blocked transport between the D^0 and D^- states is observed [11]. Finally, the measured level spectrum is compared to a multimillion-atom tight-binding (TB) NEMO 3-D calculation [14,15] of the system taking two possible chemical species, *As* and *P*, into account. Based on the fits, we can assume that the donors active in our devices to be *As* with a local *As* concentration of about 10^{18} cm^{-3}. An excellent quantitative agreement between the measured and modeled level spectra is observed [11], giving us good confidence that we can determine the chemical species and local field of single impurities in Si FinFET transistors. The conduction pattern typically measured (see Fig. 1) develops also a series of peaks that can be attributed to Coulomb Blockade of electrons in a QD created in the channel by two tunnel barriers of the low-doped access regions. From this, information's about the S/D extensions, as supported by the observed channel-length dependence of the peak spacing [9], can be obtained and this is again a point of strength of our method. Finally, the presented method offers opportunities for non-invasive characterization down to a single donor and could be a future tool in the guidance of device processing.

In a second approach [10], an evolution of the technique introduced in ref. 9, has been used to study regions of transport in *undoped* FinFET devices. Thermionic emission measurements [9-10] allow the estimation of position and intensity of area of transport in the channel. It is then possible to compare these results with the ones of our self-consistent simulations performed as described in [16-18]. Simulated 2D charge distribution along the profile of the channel under the gate can be obtained (see Fig. 2) and compared with experimental results [10]. We observe a crossover from a situation of weak volume inversion [10] to a different one of transport confined prevalently at the interface (see Fig. 2b). Overall, these results give, for the first time, an experimental insight into the evolution under different V_G's of mechanisms of conduction in *undoped* FinFETs. Even more interestingly, the difference between the experimental and the simulated data can be used to quantify the density of interfaces states [19].

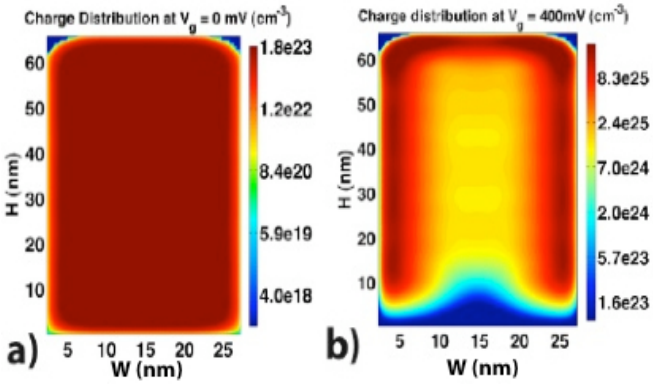

Fig 2. 2D charge distribution obtained using TB simulations [10] for different values of V_g; a) *0 mV*, b) *400 mV*, for a device having the same geometry of our FinFETs, *W= 25 nm* and *H= 65 nm*.

In conclusion, current device research requires input regarding dopant profiles. The combination of tunneling spectroscopy and thermionic measurements allow us to probe the electrical properties of the S/D regions as well as the ones of the channel and to gain atomistic insight into the dopant distribution. Here, we describe the first single impurity metrology study and the first experimental study of the behavior of the active cross-section area in function of V_G for *undoped* FinFETs. From one side we show how we can identify chemical species, electric field and position for a donor present in the channel of a doped FinFET. From another side, for the *undoped* devices, we propose a mechanism of inversion of the bands from flat band to band bending in the interface regions respectively, all as a function of V_G. By doing this, we have demonstrated, transport metrology in nano-scale CMOS devices with atomic precision.

REFERENCES

[1] M. T. Björk *et al.*, Nature Nanotech. **4**, 103 (2009).
[2] M. Pierre *et al.*, Nature Nanotech. **5**, 133 (2010).
[3] R. Wacquez, *et al.*, Symp. VLSI Tech., p. 108, (2010).
[4] M. Klein, *et al*, Chem. Phys. Chem., 10, 162-173 (2009).
[5] G.P. Lansbergen *et al.*, arXiv:1008.1381v1 (2010).
[6] M. Fuechsle *et al.*, Nature Nanotech. **5**, 502 (2010).
[7] M. Tabe *et al.*, Phys. Rev. Lett. **105**, 016003 (2010).
[8] H. Sellier *et al.*, Phys. Rev. Lett. **97**, 206805 (2006).
[9] H. Sellier *et al*, Appl. Phys. Lett. **90**, 073502 (2007).
[10] G. Tettamanzi, *et al*, *IEEE Elect. Dev. Lett,* **21**, 150 (2010).
[11] G.P. Lansbergen *et al.*, Nature Physics **4**, 656 (2008).
[12] N. Collaert *et al*, Symp VLSI Tech., p. 108, 2005.
[13] L.P. Kouwenhoven *et. al.*, "Mesoscopic Electron Transport", edited by L. L. Sohn, L. P. Kouwenhoven, and G. Schön (Kluwer, Dordrecht, 1997).
[14] G. Klimeck *et al.*, IEEE TED, **54**, 2079 - 2089 (2007)
[15] G. Klimeck and M. Luisier, IEEE IEDM 2008.
[16] N. Neophytou, *et al*, *IEEE TED*. **55**, 1286 (2008).
[17] A. Paul *et al*, *13th IWCE* (2009)
[18] S. Lee *et al*, *13th IWCE* (2009).
[19] G. C. Tettamanzi *et al*, submitted to *IEEE Elect. Dev. Lett.*