QUALCOMM CONFIDENTIAL AND PROPRIETARY

REDEFINING MOBILITY

3D Through Si Stacking Technology

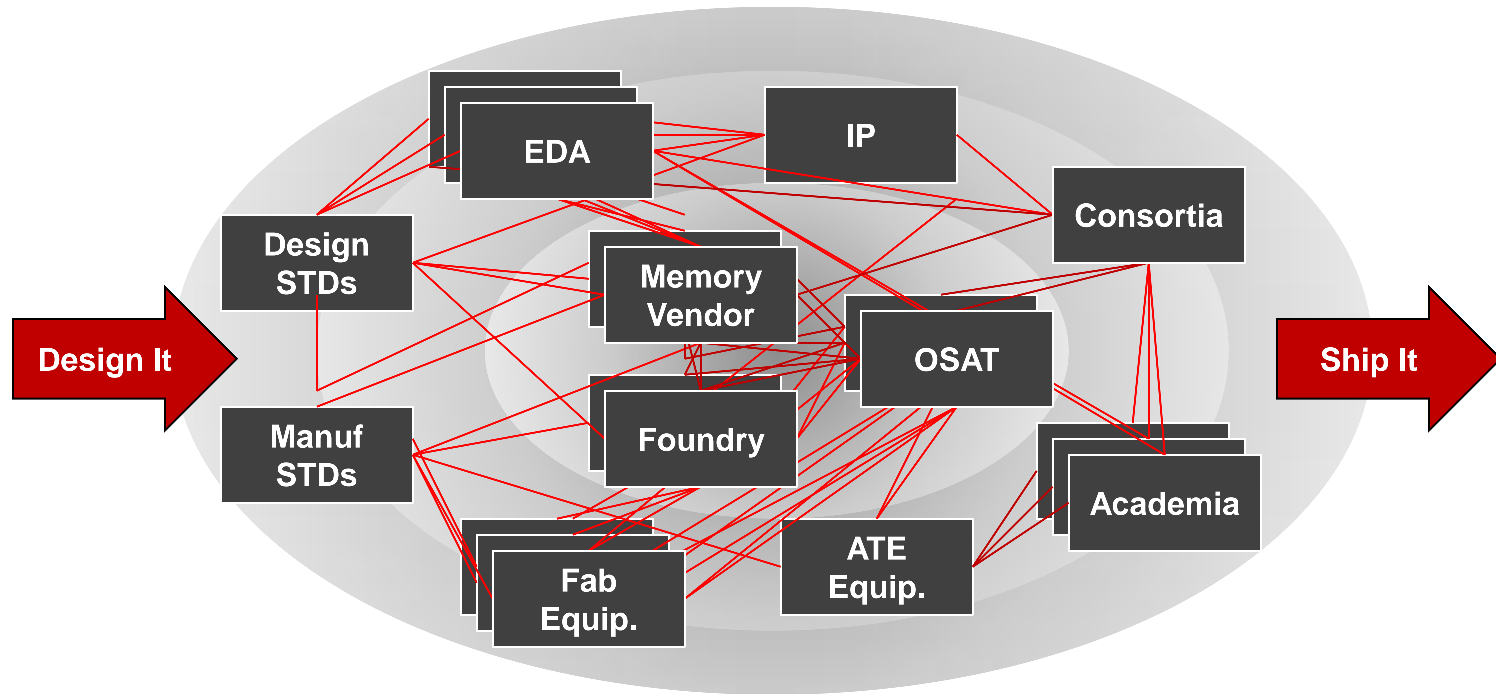
- an IFM Perspective -

RikoR

May 11

Outline

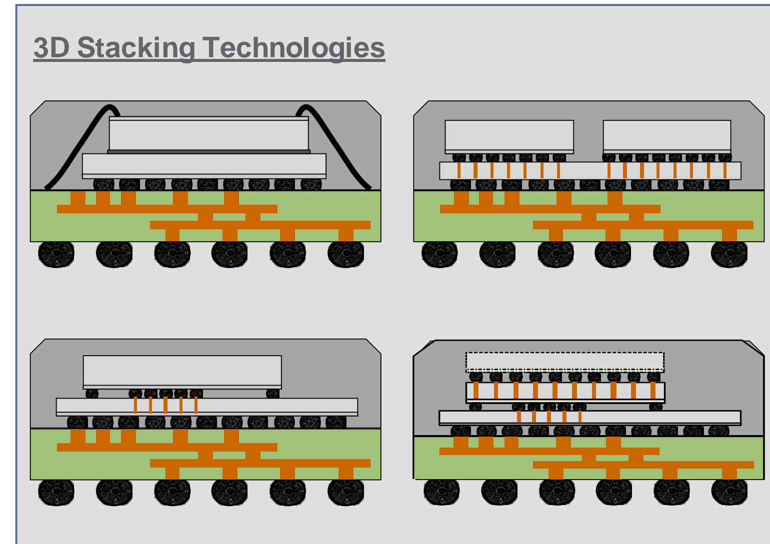
- Perspective from an IFM (Integrated Fabless Manufacturer)
  - Must bring up the Whole Supply Chain

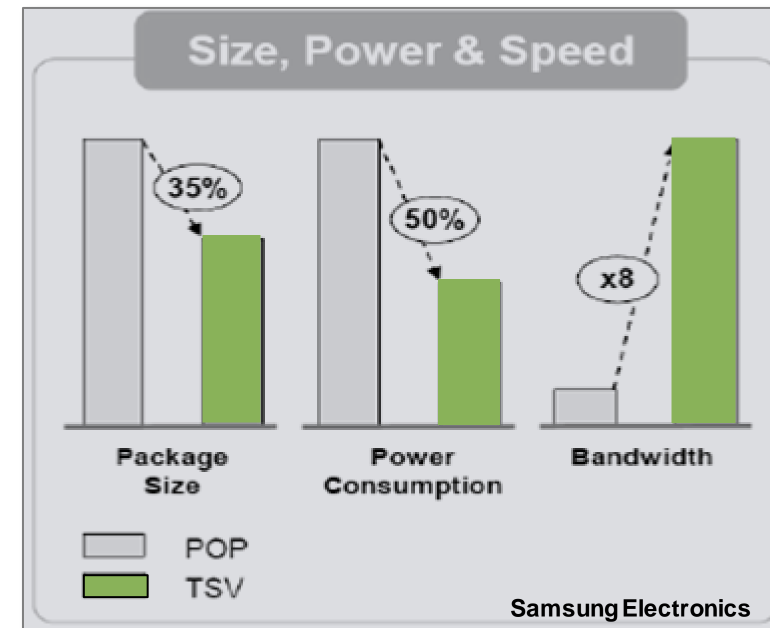


- Focus on Differentiated Design vs. Differentiated Process
- Perspectives on Present & Near Future Opportunities (1 to 3 years)
- Perspectives on Future Opportunities (3 years +)

Why 3D

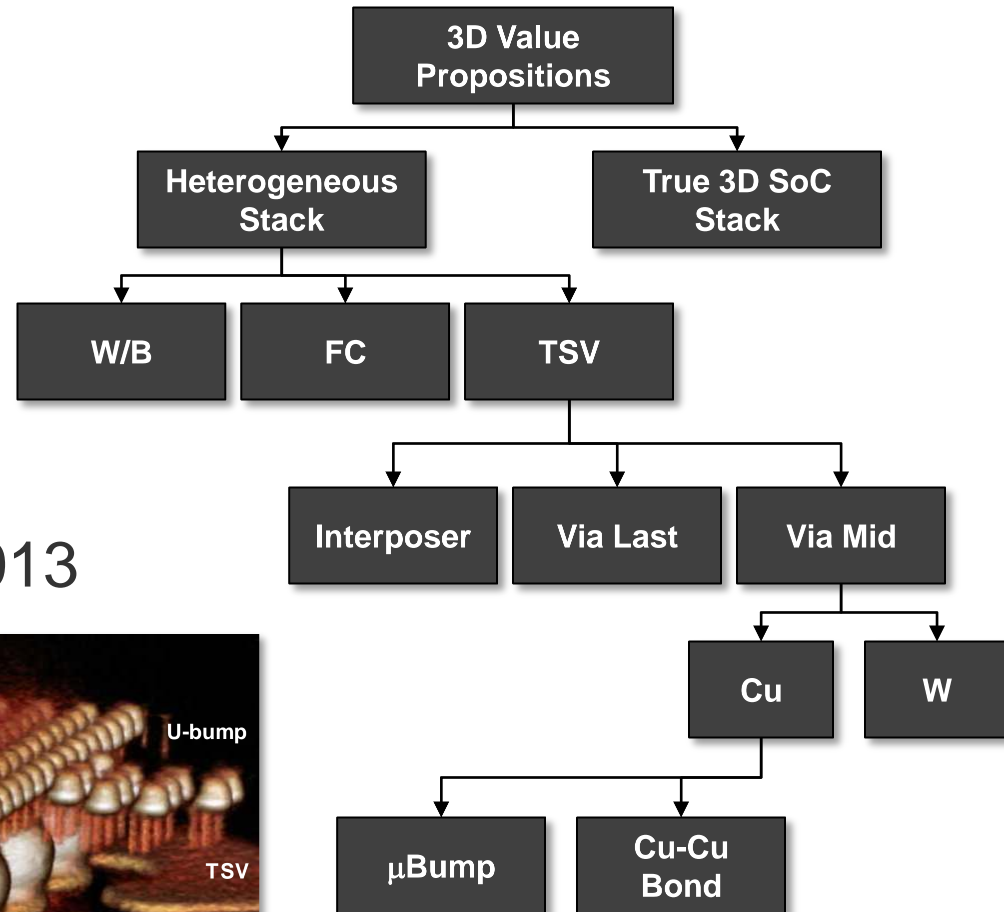
- Multiple 3D Stacking Technologies:
  - Wire Bond based (die-on-die, PiP. …)
  - Interposer based (side-by-side or stacked)
  - Through Si Via Stacking (TSS)
    - Via First / Middle / Last Technology
    - 2 or more die (stacked or side-by-side)
- All 3D Technologies Provide :
  - Better form factor (vs. multiple 2D die)
  - Better performance (vs. driving off chip)
  - Higher Flexibility (vs. single chip SoC)
- High Density TSS Integration Provides:
  - Better Architectures (vs. 2D SoC + PCB Integration)
  - Comparable Cost Structure (at System Level)
    - As Enabled by High Aspect Ratio TSV_{middle}
  - e.g. Wide IO Memory on Logic (+ 3D TSS)
    - Best of All Worlds
    - 3D "Packaging Technology" Benefits
      - » Superior Form Factor and Power (vs. driving off chip)
    - 3D "Integration Technology" Benefits
      - » Superior Bandwidth Efficiency (vs. LPDDRx or Serial)

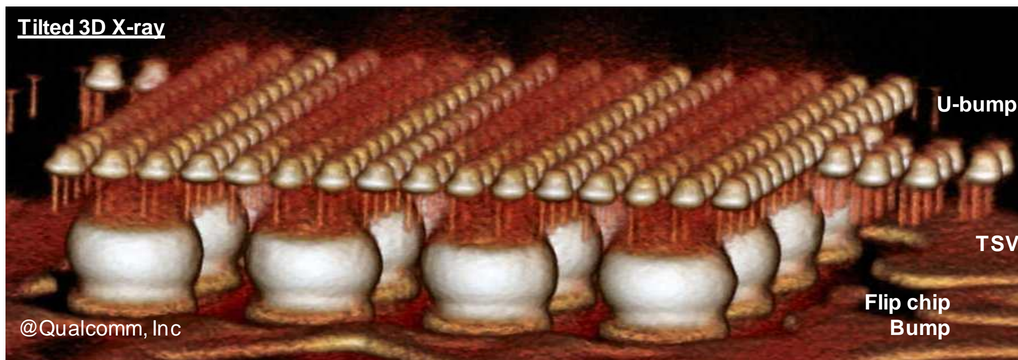




Which 3D Through Si Stacking (TSS)

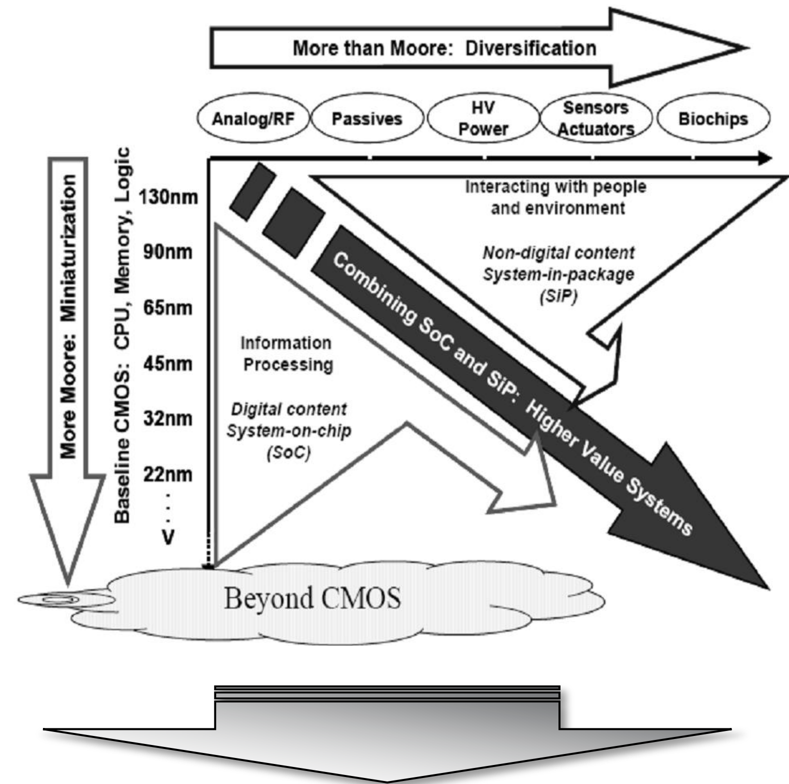
- For High End Smart Phone App
  - In Technical Space
    - Form Factor vs. Interposer
    - Power vs. LPDDRx
    - Risk vs. Cu-Cu, etc..
  - In Business Space
    - Market Growth drives Volume
    - Growths justifies ROI
    - Volume drives Costs
    - Cost Drives Adoption
- Target Implementation ~2013





What is Different about 3D TSS Technology ?

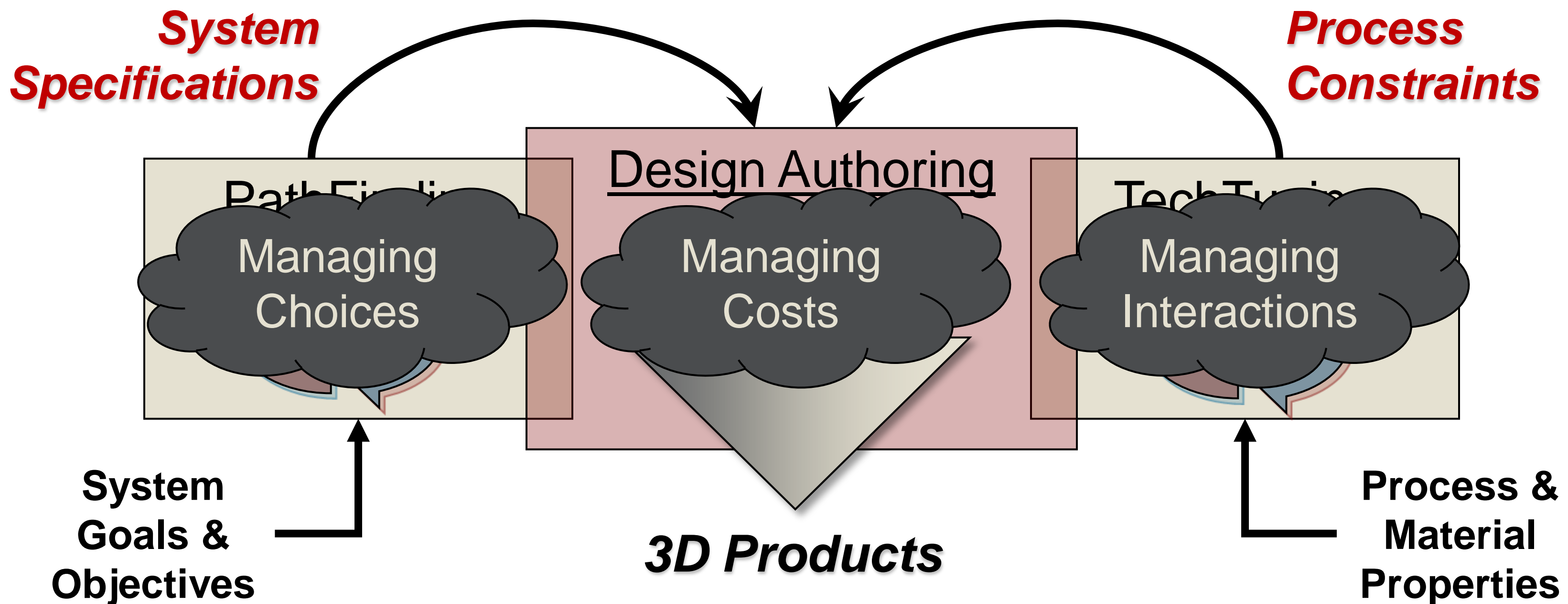
- 3D Core Value Propositions
  - Power – Performance
  - Form Factor
  - Modularity & Flexibility
- 3D Challenges & Opportunities
  - New Degrees of Freedom
    - New Partitioning Choices
    - New Integration Choices
    - Stack Architecture Choices
    - Many Technology Choices
    - TSV Process Flow Choices
  - Die to Die Proximity
    - Electrical Interactions
    - Thermal Interactions
    - Mechanical Stress Interactions



Managing Choices & Interactions

Eco-System for 3D Design

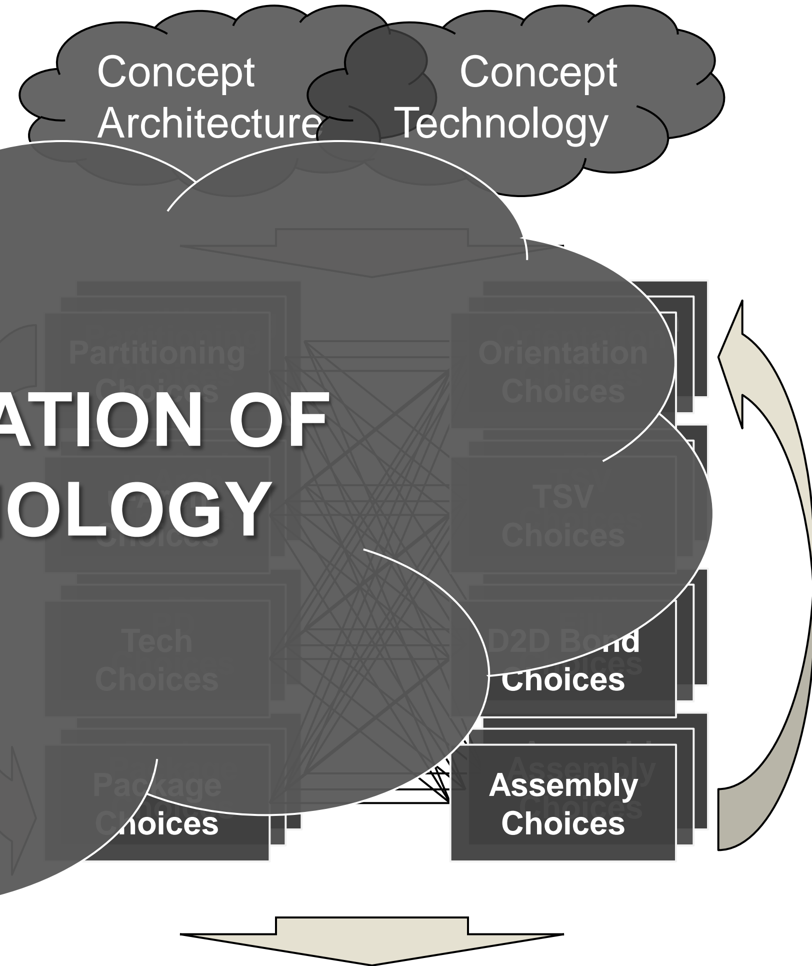
- **Segment Design Eco-System into 3 Buckets to Address 3 Key Challenges**
- ***Design Authoring* – actual chip design**
  - Implement Design via (mostly) Traditional 2D Chip Design Flow (RTL2GDS))
  - Output GDS
- ***PathFinding* – design/technology concept exploration**
  - *Manage Choices* via Cheap, Quick & Dirty Concept Design
  - Output Clean Specs
- ***TechTuning* – physical space exploration**
  - *Manage Interactions* via Cheap, Thermal & Mechanical Chip Simulation
  - Output Clean Constraints



Managing Choices: What Does It Mean for TSS Design ?

- Navigating Choices ….
  - Want to optimize product attributes
  - Cost, power, performance, engineering …
- Need to Co-Optimize Process & Design
  - Winning 3D Product will Be Architected specifically to Leverage 3D Technology
  - Selection o
- Structured Methodology
  - Past experience not applicable
  - Opportunity for paradigm shifts
  - Not tied to Legacy design
  - Process-design co-optimization
- Spatially Aware Methodology
  - Quick and flexible
  - Hi fidelity / low accuracy

NEED CO-EXPLORATION OF DESIGN & TECHNOLOGY OPTIONS

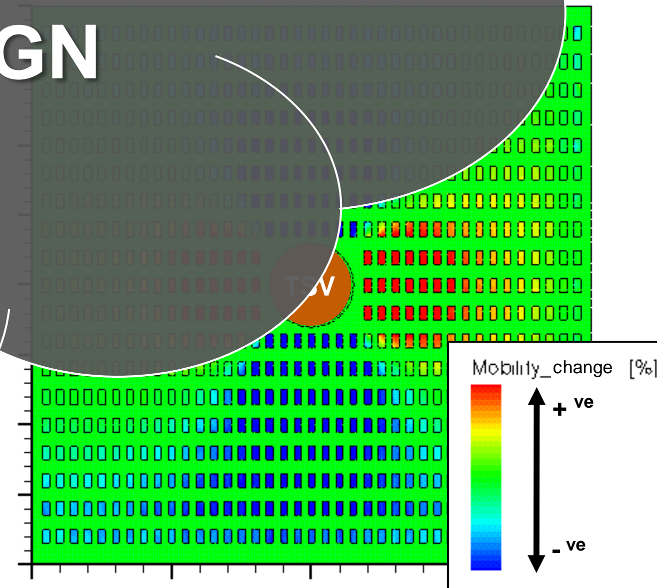


QUALCOMM CDMA Technologies
imec
AutoESL Design Technologies, Inc.
ATRENTA

Managing Interactions: What Does It Mean for TSS Design?

- Managing Interactions
  - Intimate Proximity and Coupling Between Die
  - In Electrical, Thermal & Mechanical Domains
- Electrical Interactions
  - SPICE models, Electrical Analyses Tools
  - PDN, SI Guidelines, Analyses and SignOff
- Thermal Interactions
  - Incorporate Thermal Considerations in Partitioning and Floorplanning Design Decisions
    - Simulation Tools Integrated in Design Environment
    - Import Target Package Thermal Characteristics
  - Thermal Guidelines and Thermal SignOff
- Mechanical Stress Interactions
  - Incorporate Stress Considerations in Floorplanning and Layout Design Decisions
    - Simulation Tools 'understand' Electrical Effects
    - Import Target Package Stress Characteristics
  - Stress Rules and Stress SignOff

NEED INCORPORATION OF THERMAL AND STRESS FACTORS INTO DESIGN PRACTICES



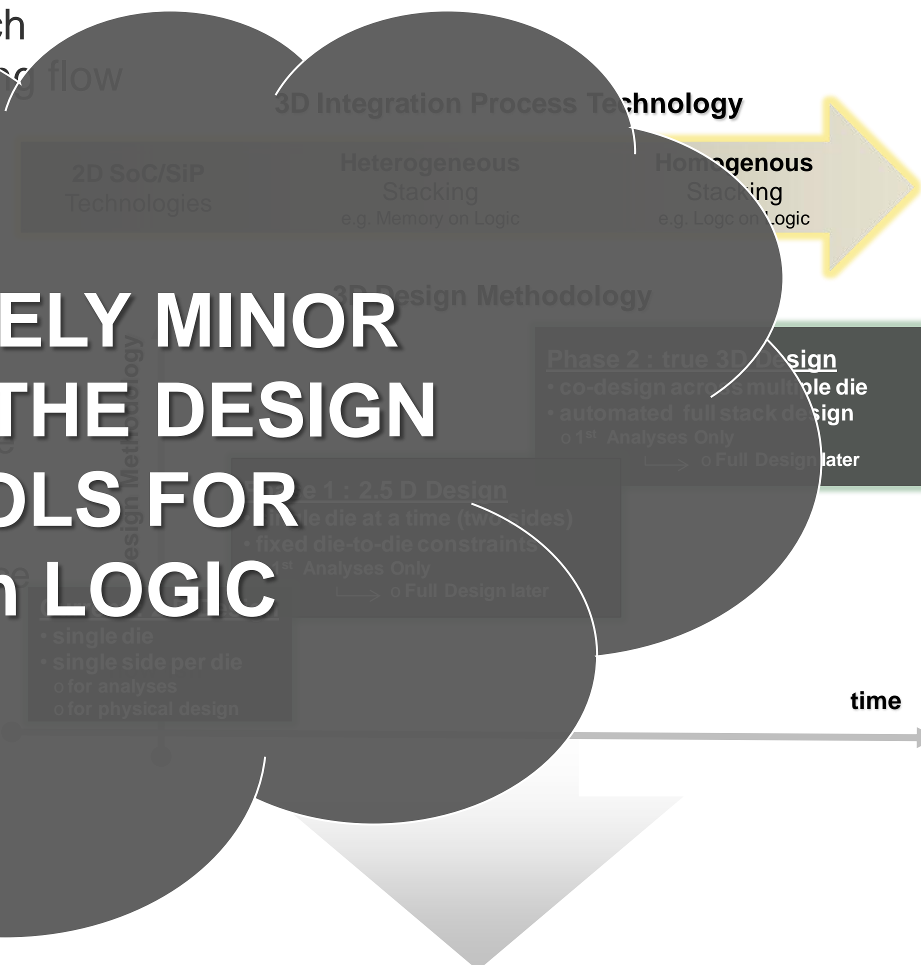
QUALCOMM CDMA Technologies
cadence
synopsys
Mentor Graphics

Managing Costs : What Does It Mean for TSS Design?

- Expect Gradual and Graceful Evolution
  - Process and Design – together and in synch
  - Sensitive to the HUGE investment in existing flow
  - Applications Driven
- Now : Heterogeneous Stacking
  - e.g. Memory (or Std Analog) on Logic
  - Design Methodology Requirements
    - Partitioning
    - Floorplanning: need awareness of the other die
    - Syntheses : 1-die-at-a-time
    - Physical Design : maybe a 2-sided die
    - Physical Verification
    - Verification & Analyses : whole stack

NEED RELATIVELY MINOR UPGRADES TO THE DESIGN FLOW & TOOLS FOR MEMORY on LOGIC

- Next : Integrated Stack Designs
  - e.g. Logic on Logic
  - Design Methodology Requirements
    - Integrated Co-Design
    - System Level (aka PathFinding)
    - Design Authoring – including the Package
    - Manufacturability (aka TechTunung)



Evolution from 2D Design

QUALCOMM CDMA Technologies
Apache
SIGRITY
cadence

Requirements for Heterogeneous Stack Design (now)

Standards

- "Design Exchange Formats"
- Model Formats
- Manufacturing Hand Off & Inspection Standards

TechTuning Methodology

- Methodology
- Models & Material Properties
- Infrastructure

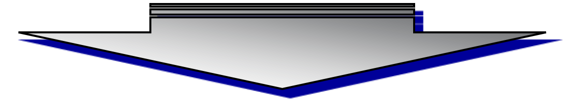
Design Authoring Corner Methodology

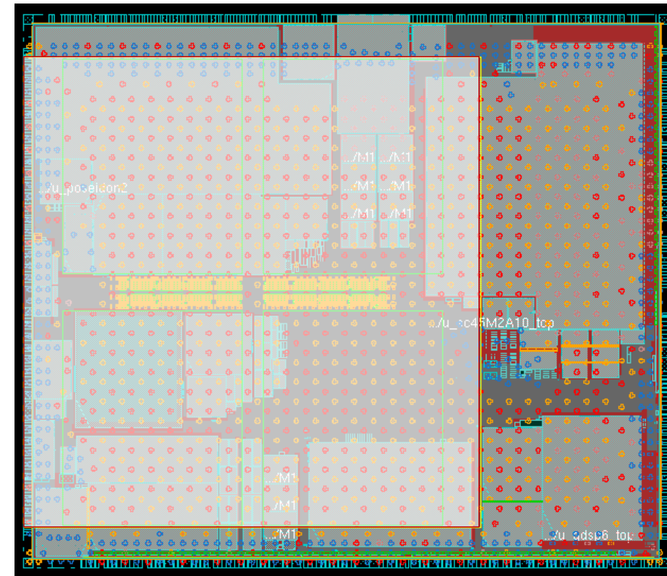
- Thermal & Mechanical Simulation Capability
- Integration of Interactions (esp. Thermal & Mechanical) into Design Environment

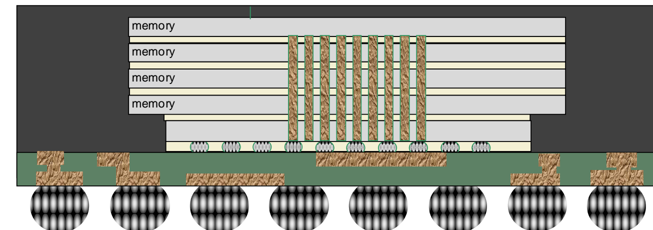
Others

- ESD Protection for Tier-to-Tier pins
- Reliability Landscape

Current TSS Driver







Standardization : Best Opportunity to Bring Down Barriers

- A lot of Ongoing Activities

Tracking of the Overall Industry Status taken on

by

3D Enablement Center

- Need Assignments & Focus
  - Specific Proposals

Work in Progress to Define Exchange Formats taken on by the SRC, GSA & Si2

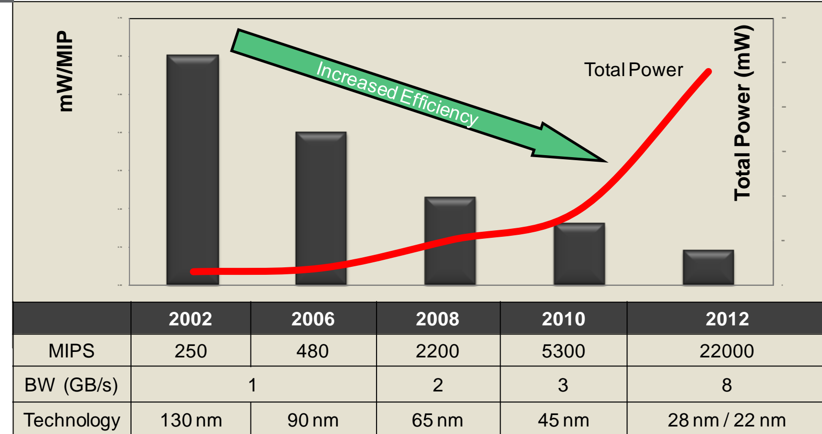
  - Identified a number of Specific

Work in Progress to Define Manufacturing Standards taken on by the 3D Enablement Center & SEMI

Technical Area			Driver	Stds Body
D2D	layout compatibility	Bump Layout	Die Supplier	JEDEC
		Bump Array Layout		
		Bump Assignment		
PDK	modeling compatibility	Electrical model format	GSA & SEMATECH	Si2
		Thermal model format		
		Stress model format	Sematech	
Design	design data base compatibility	PF Exchange Formats	IMEC	Si2
		Stress Exchange Formats	EDA	
		Temp Exchange Formats	EDA	
		PDN Exchange Format	EDA	
		SI Exchange Format	EDA	
		DFT Exchange Formats	IMEC	IEEE
Materials	Material compatibility	Metallurgy pairs	Sematech	Sematech
		Max dT SoA		
		Reliability SoA		
QA	Incoming specs	Metrology (e.g. Warpage)	Sematech	JEDEC
		Die/wafer QA metrics	SEMI	
Flow	Handling specs	Shipping Carrier specs –	Sematech	SEMI
		In-Assembly ESD	OSAT	ANSI/ESDA
Test	DFT & HW Test	KGD / pre-Bond test	IMEC	IEEE
		Probe Cards	IMEC	

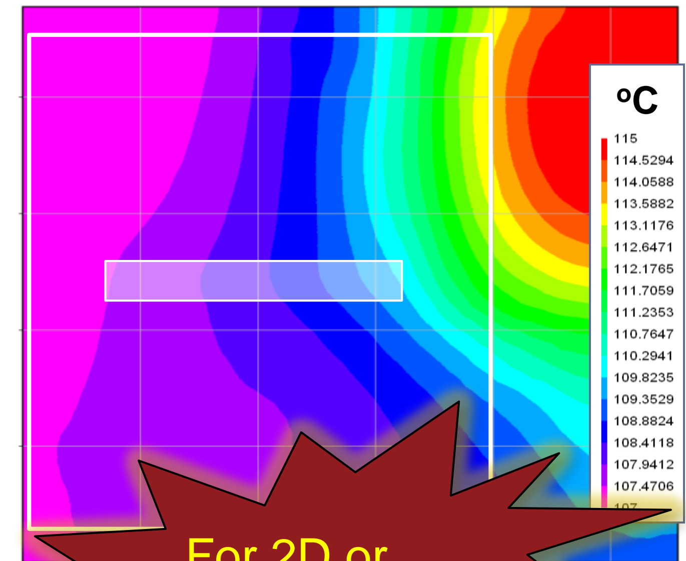
Thermal : Everything Changes …

- If We Did Not Have a Thermal Problem Now, Will We Have One in the Future … The World has Changed
- Mobile power densities approaching CPU
- Thermal Considerations Constraining System Design



	2002	2006	2008	2010	2012
MIPS	250	480	2200	5300	22000
BW (GB/s)	1		2	3	8
Technology	130 nm	90 nm	65 nm	45 nm	28 nm / 22 nm

	Past	Future
Reality	• Excess Margin	• Negative Margin
Diagnostics	• Fixed Arbitrary	• Reference System
	• Steady State (dc)	• Transient (ac)
Design	• WC Spec	• Realistic Spec
	• System Lvl Sensing	• On Chip Sensing
	• Performance / Power	• + Design for Thermal

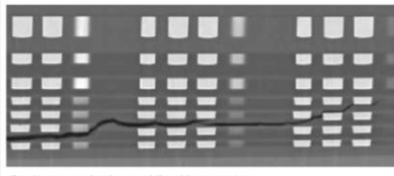


For 2D or 3D designs

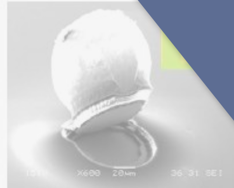
- Must Manage Hot Spots
- Must Manage Overall System Thermal Limit

Mechanical Stress: a "Perfect Storm"

- Chip-Package Interactions (CPI)
  - Package-Si CTE Mismatch
  - Soft ELK + Hard Cu
  - Hard Pb-Free Balls
  - Harder Cu-Pillars

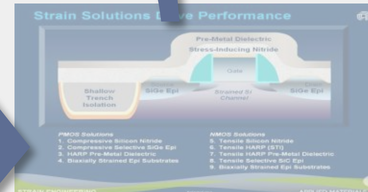


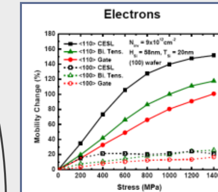
Crack propagation in a multilevel interconnect.

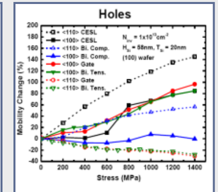


- Material Integrity Issues

- On Chip Strain Sources
  - BEOL-FEOL CTE Mismatch
  - Liners (CESL / memorization)
  - SEG Strained Si (eSiGe, eSiC)
  - Metal Gates & Contacts / STI …







- Device Electrical Integrity Issues

Σ

- 3D TSS Technology Interactions
  - TSV : interaction of (big) Cu … neighboring devices ?
  - µ-Bump : new issues with both, Tier 1 and Tier 2 die ?
  - Thin Si : Enhanced BEOL-FEOL + Si-Pckg CTE Mismatch
  - BRDL : new CTE Mismatch challenges
  - Die to Die : stress re-distribution among the stacked die
  - Die Alignment : stress concentration among stacked die

Thermal/Stress Simulation Requirements = TechTuning

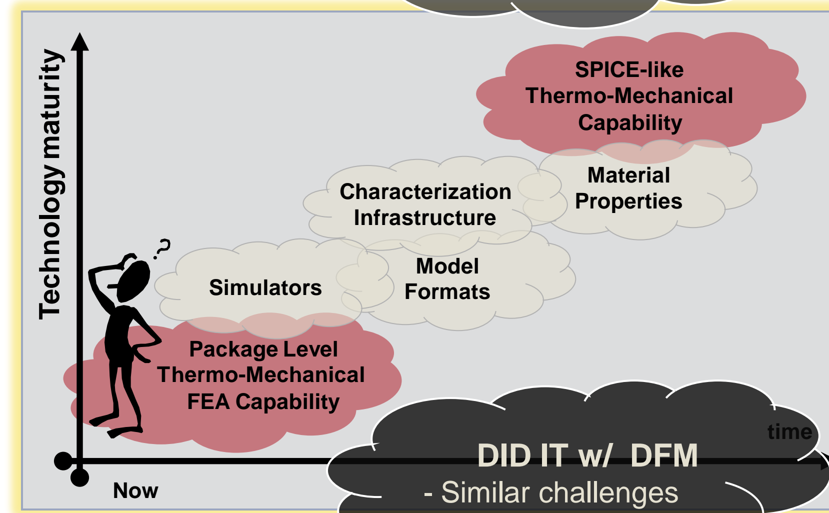
- Simulators
  - Software tool(s) and Simulation Methodologies
- Models
  - FEA and/or Compact Behavioral models
  - Absolute vs. values relative to some reference point ?
  - Modeling of individual layers vs. smear a stack of layers ?
- Data
  - Material Properties
    - FEOL, BEOL, RDL, uBump, FC Bump, Underfil, Substrate..
    - Young's Modulus, Poisson's ratio, TCE, Stress Free T..
    - Thermal Conductivity
  - Geometric Properties
- Standards
  - Model Formats
  - Exchange Formats (Handoff among Tools)
  - Metrology Systems & Definitions
    - Calibration QA Methodology
    - Validation QA Methodology
- Use Flow
  - Use Environment QA Methodology

THIS IS A LOT OF WORK + NEW STUFF

BUT necessary if TSS technology is to go mainstream

SO LET US BEGIN
-If not us or now - then who and when ?

SPICE TEMPLATE
-Established model based eco-system



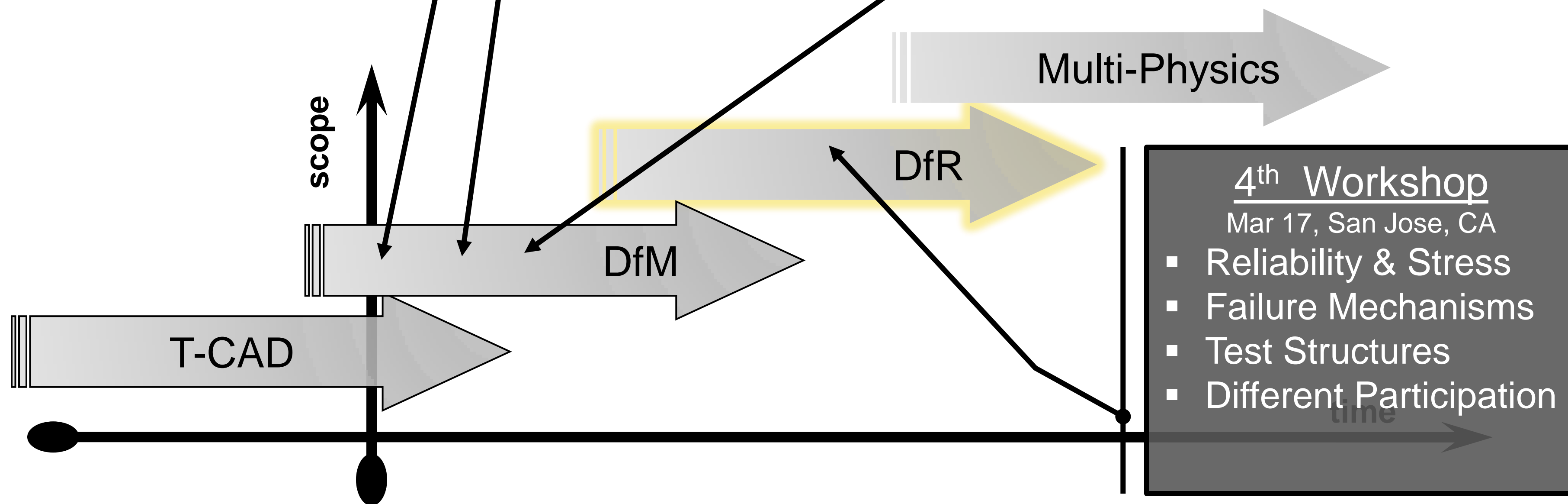
Status : Stress Simulation Methodology

- T-CAD
  - ✓ Have ability to simulate within a domain and within a process flow
1. Manufacturability and DFM
   - Integrate into a flow & add ability to simulate at End-of-Line effects
   - Develop Fundamental Infrastructure
2. Reliability and DfR
   - Add ability to simulate operational time
3. MultiPhysics
   - Add ability to simulate inter-dependence during operational time

1st Workshop
March 2010 Albany, NY
- ✓ Agreement on the feasibility of the DFM methodology
- ✓ Formulation of the Problem

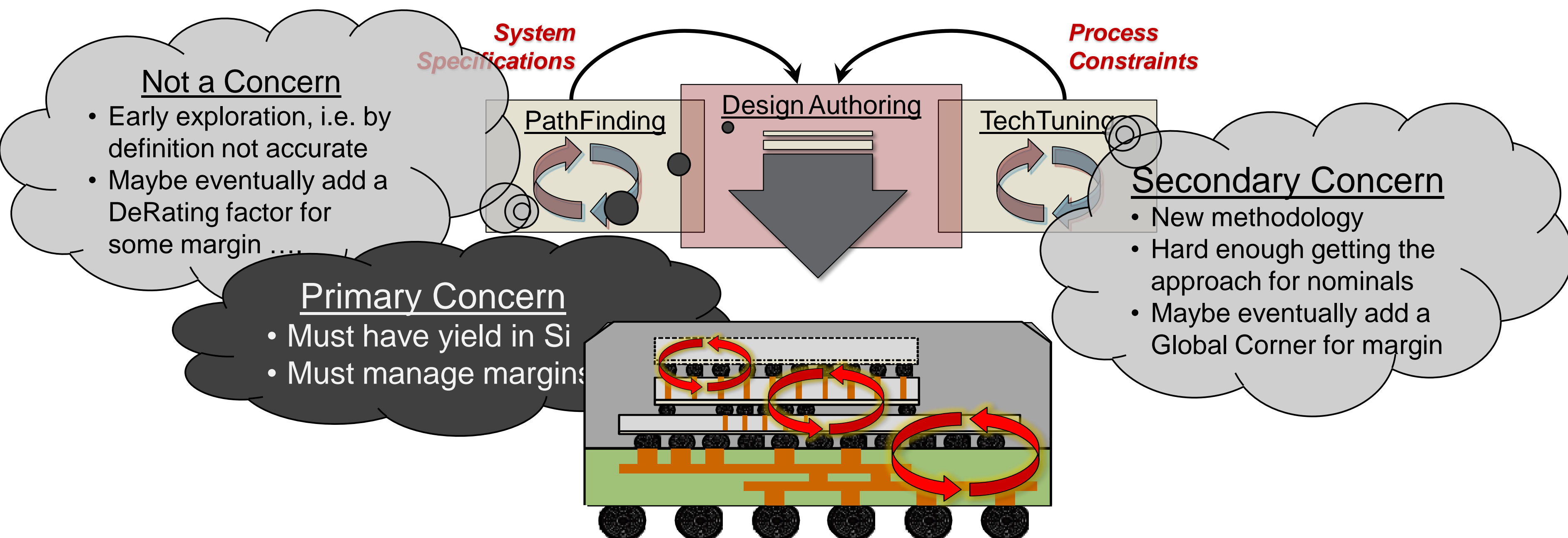
2nd Workshop
July 2010 San Francisco, CA
- Review proposed Std Tables of Material Properties & Char. Methods
- Broader Participation

3rd Workshop
Oct 2010 Dresden, Germany
- 'Blessing' of the Methodology & Characterization Techniques
- Broader Participation



QUALCOMM CDMA Technologies

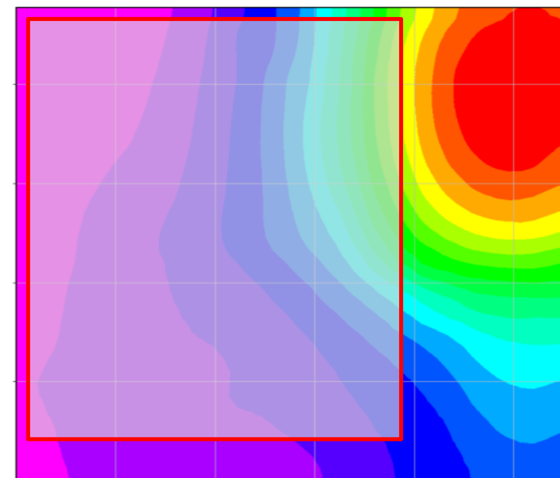
Concern w/ Managing Interactions & Variability

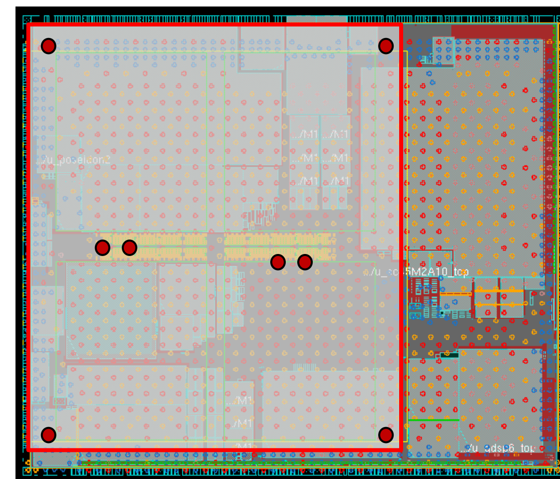


- Old Sources of Variability & Variability Concerns
  - '2D Variability" i.e. all the usual P-V-T Variability
- New Sources of Variability : 3D Tier to Tier Interactions
  - Variability induced by Electrical Interactions
  - Variability induced by Thermal Gradients
  - Variability induced by Mechanical Stress
- Design Authoring: Do One Die at a Time *But Analyze the Whole Stack*
  - e.g. For Power and Signal Integrity and/or Thermal & Stress Interactions

Variability Caused by Interactions : the Problem

- **Concerns** :
  - Thermal Hot Spots and Thermal *Gradient*
  - Stress “Hot Spot” and Stress *Gradient*
  - Power & Signal Integrity issues
  - May induce unique & incremental failure modes
    - e.g. mismatch (in analog, memories, differential circuits..)
    - e.g. race conditions (in set up and hold circuits ..)
  - Not addressed by any of the current design flows
  - Also a Source of *Excess Margin* in 2D SoC Designs

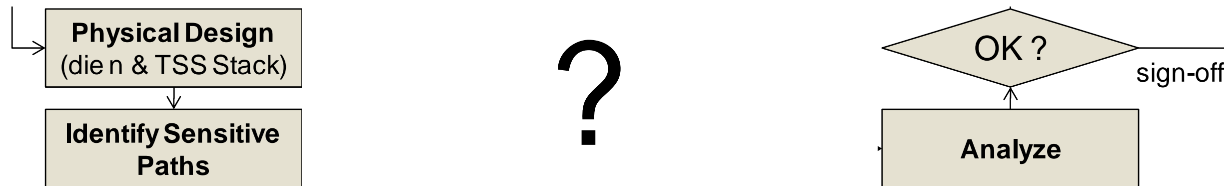




- Especially for Advanced 3D Stacked SoC Designs
  - Performance & Functionality Pushing Electrical Limits
  - Form Factor Pushing Physical & Material Limits
  - Temperature Range across a die > 10°C quite possible,
  - Local Stress Mobility Variations > 10% quite possible
  - Si/PI issues above the norm for 2D die quite possible
- Especially When Induced by an External Source
  - e.g. when caused by interaction with another die in a stack
  - cannot be identified during die characterization and sort test,
  - *Failure mode very difficult to de-bug => low risk / hi liability*
- Clearly Key and Fundamental Consideration for 3D Stack Design

Thermal Variability : Design & Validation Solution ?

- **Design Requirements** : Address Thermal & Stress Gradients in Design
  - Methodology, Tools, Flows, Standards, Models, Practices…
- Need it to be Minimally Invasive to Today's Flows
  - Best Addressed as a New Source of Variability in Existing Flow ?



- Simulate Temperature / Stress Profile on Each Die in a Stack
- Import Temp / Stress Profile of All Die in a Stack
- Superimpose Temp / Stress Gradient on Timing Flow
- **Validation Requirements** : Thermal/Stress Calibration + Timing Validation
  - Validate Thermal Simulator vs Test Chip Si ? and/or
  - Characterize Sensitivity of Each Die and Define Safe Op. Area ? and/or
  - Characterize Thermal Interactions post-Stack ?
    - DFT Challenge and/or Induce Thermal Gradients Some Other Way ?

Incremental Short Term Opportunities ?

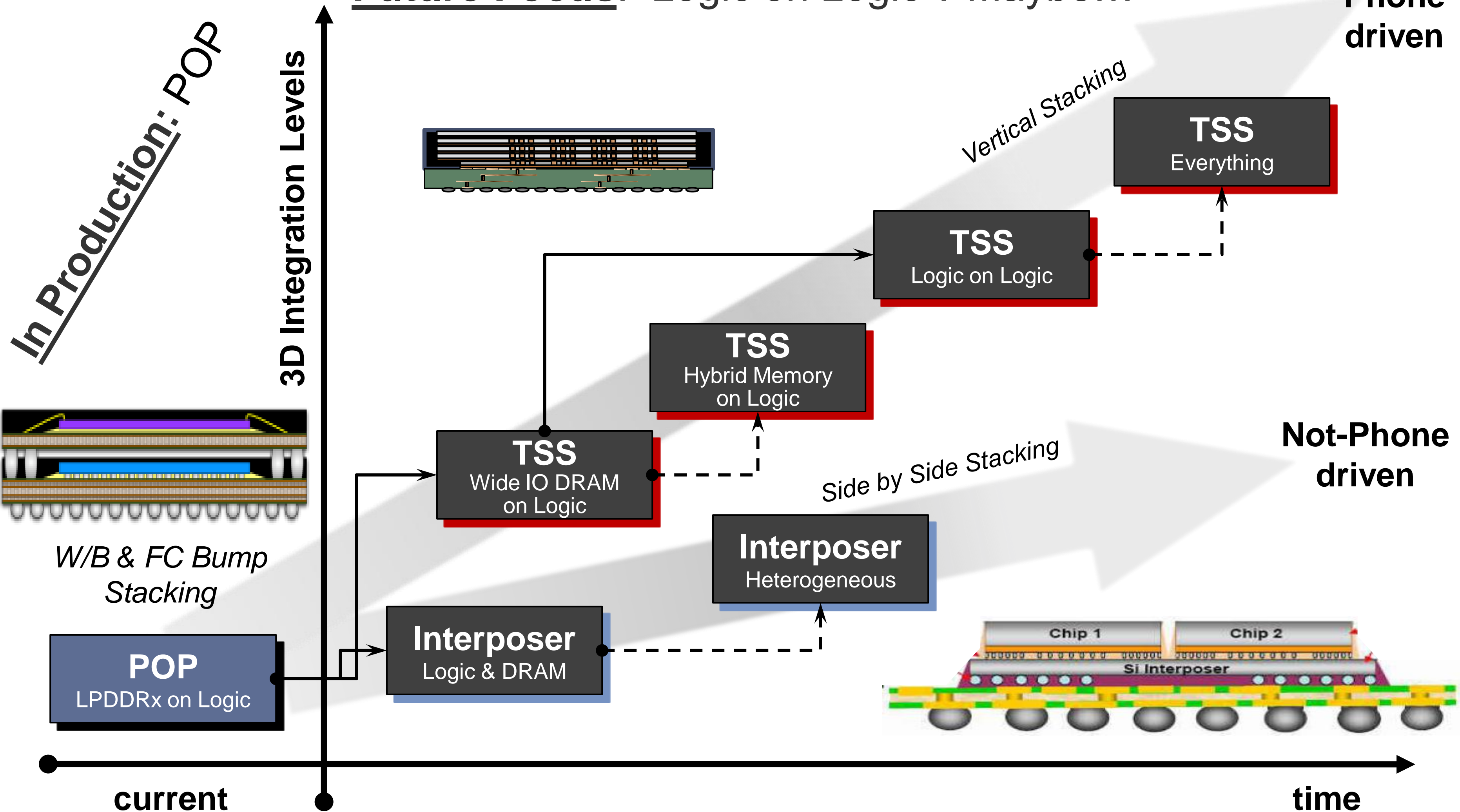
- 3D Reliability
  - Taxonomy of the Incremental 3D Failure Mechanisms
    - Especially in addition to the stress issues (Stress Workshop – in flight)
  - Failure Modes, Mechanisms, Models, Test Structures, Test Environments ...
  - 3D Product Qualification Requirements
  - SRC RFP - in flight
- ESD – die to die discharge during stacking processes
  - i.e. how much protection is required for pins that only face other tiers ?
  - Why is it not 0V & How can it be Driven
    - Discharge modes and charge sources
    - Measurements and process controls
  - Feels a bit like an orphan problem

QUALCOMM CDMA Technologies

Qualcomm Advanced Technology 3D Stacking Roadmap

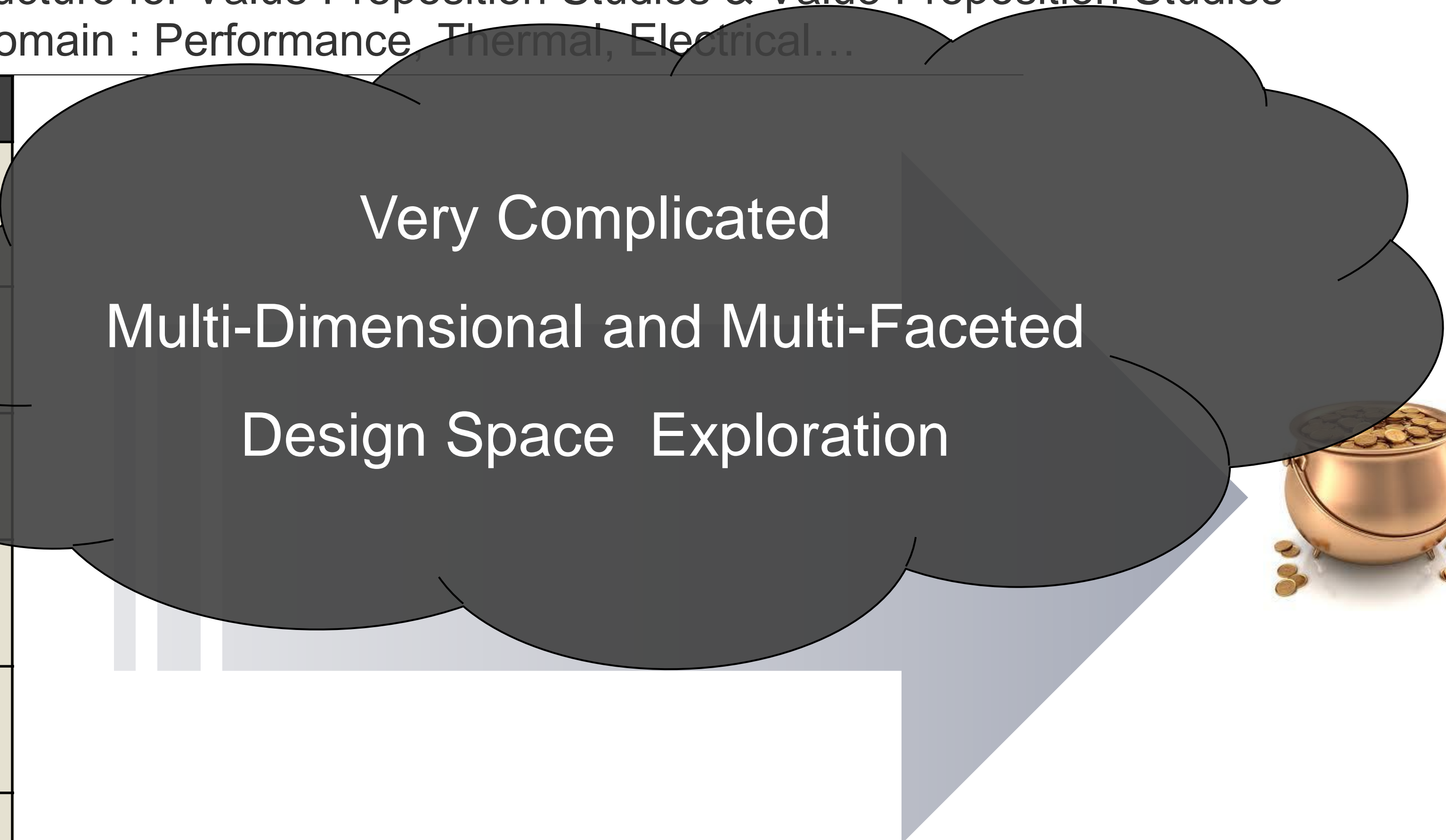
Current ATI Focus: Wide IO DRAM on Logic + TSS

Future Focus: Logic on Logic ? Maybe…



Need a Killer App : the Driver

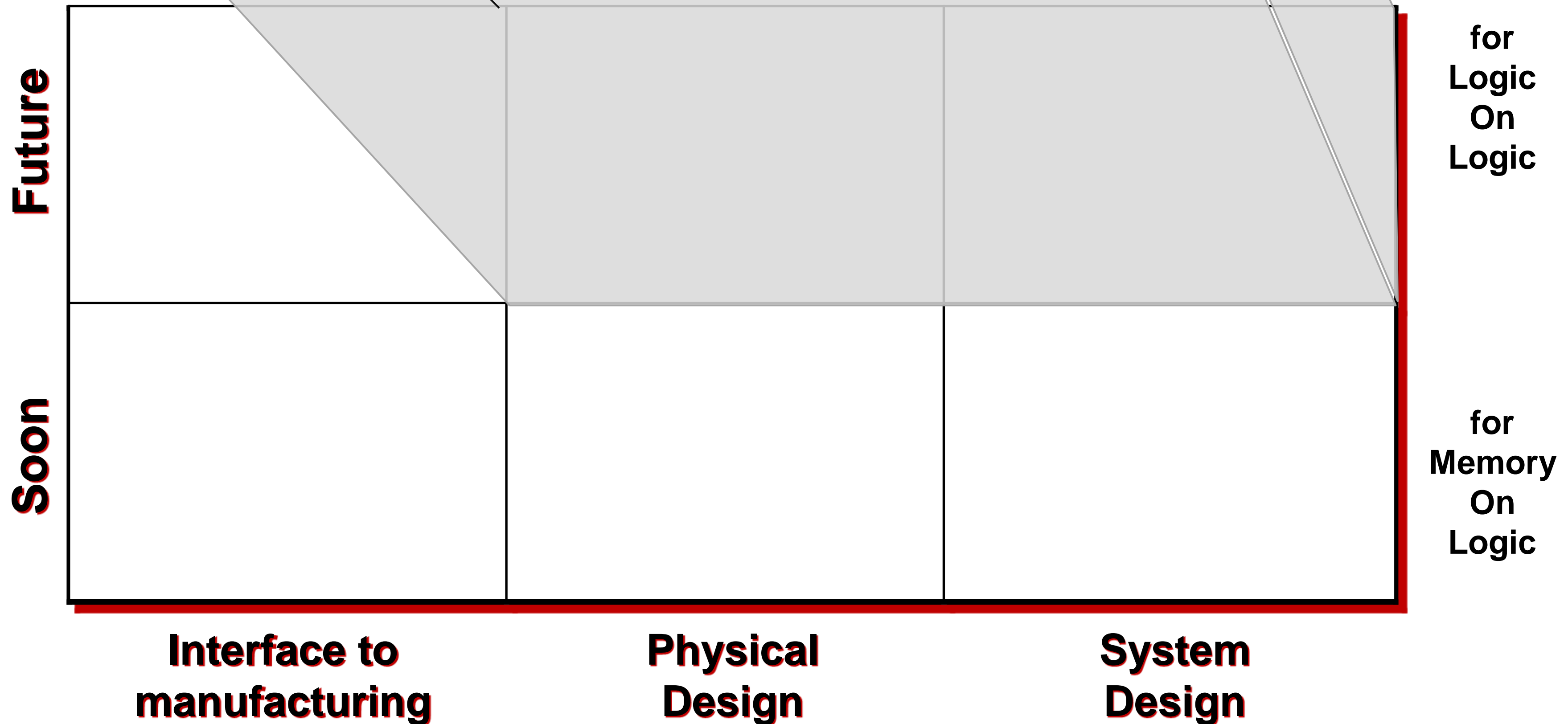
- Beyond Wide IO Memory-on-Logic
- Key Research Opportunities
  - Ideas for Candidate Solutions
  - infrastructure for Value Proposition Studies & Value Proposition Studies
  - Multi Domain : Performance, Thermal, Electrical…



QUALCOMM CDMA Technologies

Design Domain Challenges

- Increment
  - Top dow
- Key Rese
  - Chip De
  - System Design : Spatially Aware Path-finding



Design Domain Challenges

- Incremental 3D Process Features and Challenges
  - Top dow
- Key Resea
  - Integratio
  - Package

Research and Start Up Opportunities ?

ture

- **Ready-Made CMOS with Integrated TSV**
  - On all future nodes
- **Standard Metallurgy w/ Min. Restrictions**
- **New Package Designs & Materials**
  - For Thermal Management
  - For modularity

for Logic On Logic

Manufacturing Ramp Opportunities

Soo

- Thinning/uBump Process
- Uniform TSV Distribution
- Yield & Reliability
- Extended Design Kit

- Uniform fixed array config
- Yield & Reliability
- Multi Sourcing
- Select Metallurgies

- **Multi-Sourcing**
  - For memory die
- ✓ **Standards**
  - Thin Wafer handling
  - Carriers
  - …

for Memory On Logic

Integration w/ Si Process | **Integration w/ Other Die** | **Integration w/ Packaging**

QUALCOMM CONFIDENTIAL AND PROPRIETARY

REDEFINING MOBILITY

THANK YOU

RikoR

1Q11