Prospects for Nanoelectronics CMOS Scaling and Functional Diversification

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SRC/SFI/NSF Forum on Integrated Sensors for Cybersystems (FISC-2030)

Outline

- **Introduction**
- **Nanoelectronics scaling with thin films devices, new materials and new devices architectures.**

  Exploitation of 3rd dimension. Low Power/ High Perfomance
- **Heterogeneous Co-integration of More Moore and More than Moore.**

  3D as a strong asset. New applications .New progress laws.
- **Conclusion**

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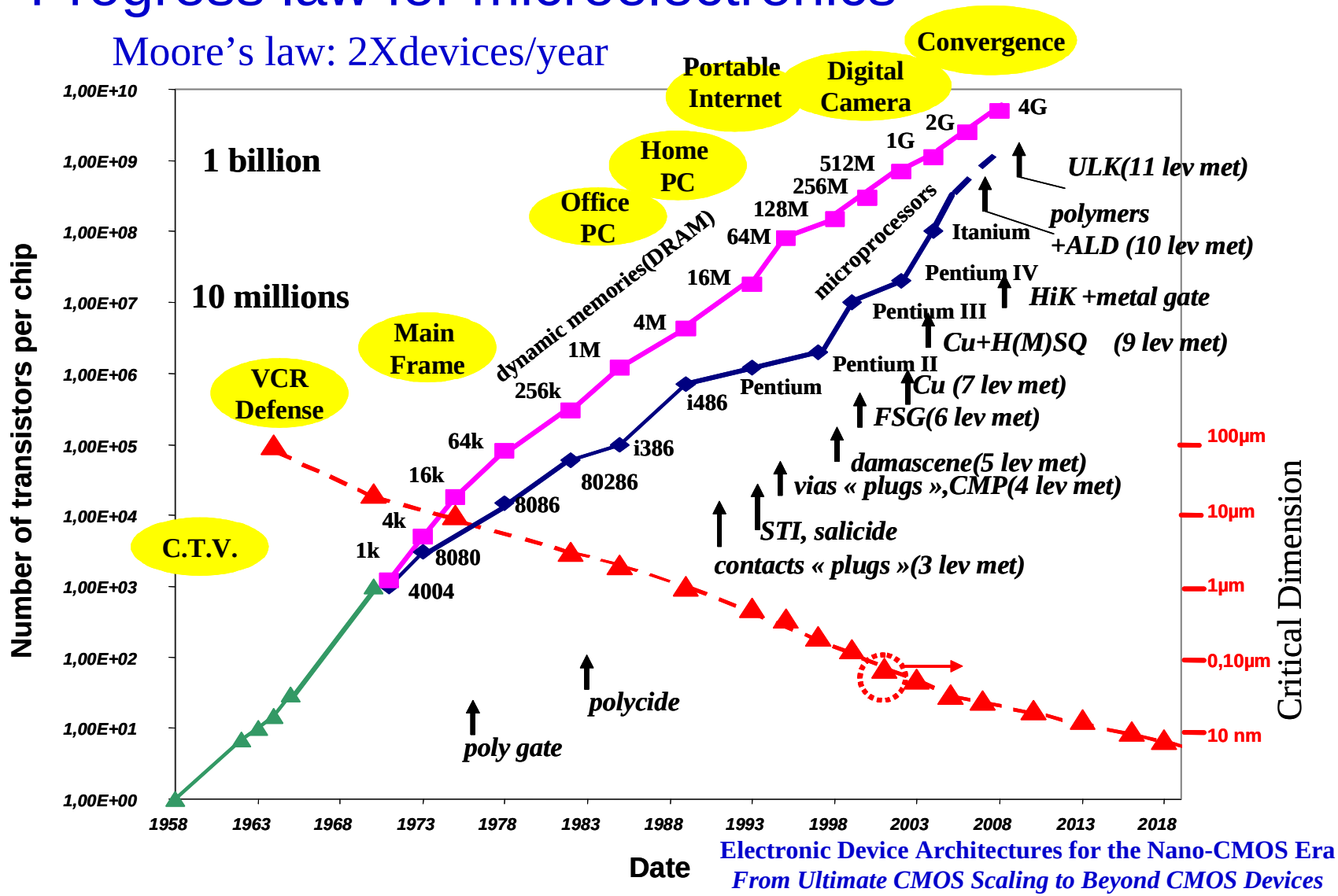
Scaling: a success story...thanks to innovation
Progress law for microelectronics



Electronic Device Architectures for the Nano-CMOS Era
From Ultimate CMOS Scaling to Beyond CMOS Devices
Editor: S.Deleonibus, Pan Stanford Publishing, Oct 2008

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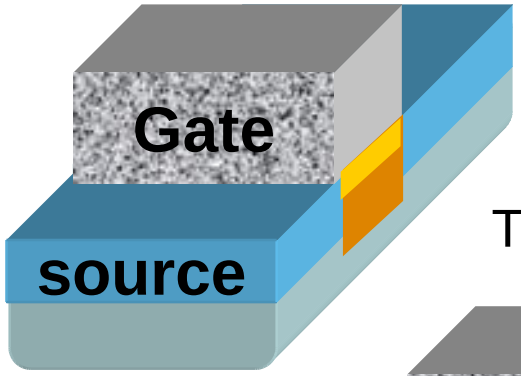
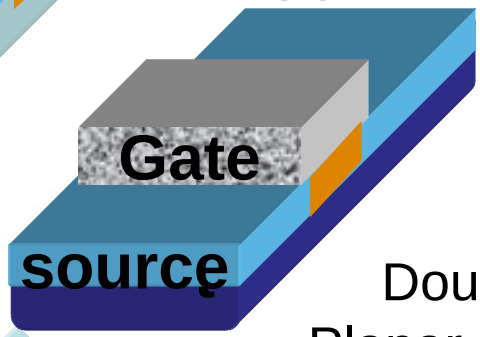
Bulk or thick SOI

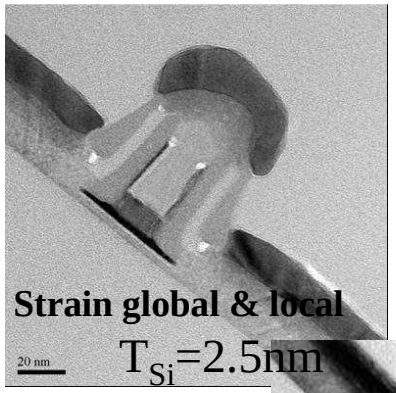


ThinSOI



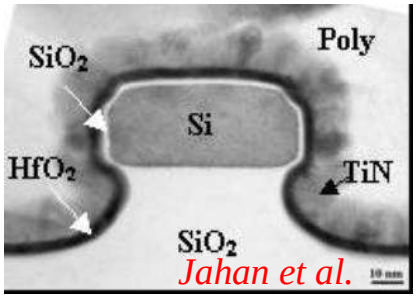
Planar

T_{Si}= ¼ Lg

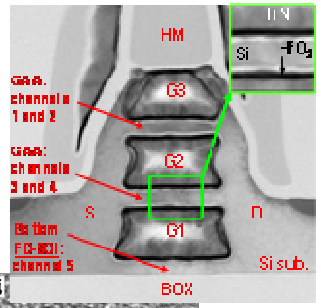


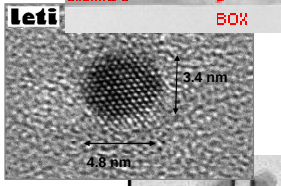
Barral et al. IEDM2007

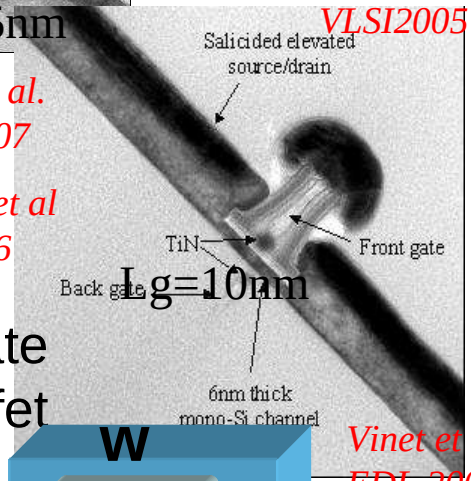
Andrieu et al VLSI2006



Jahan et al. VLSI2005

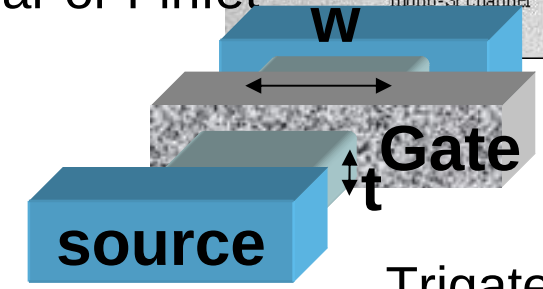




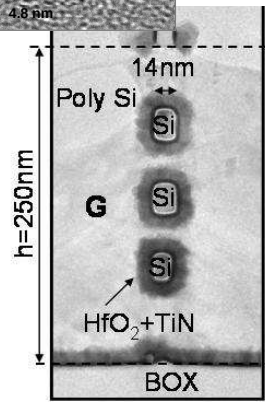


Vinet et al. EDL 2005

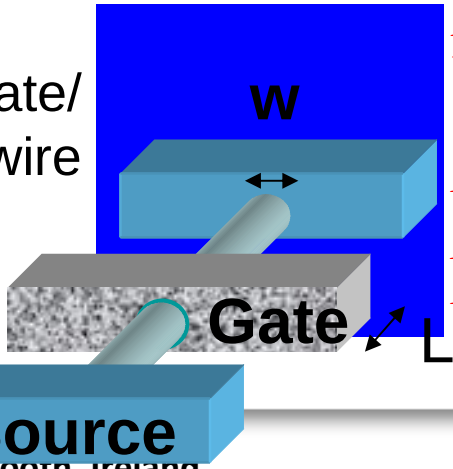
Double-gate Planar or Finfet



T_{Si}= ½ Lg



Trigate/ nanowire



Bernard et al VLSI 2008

Dupré et al. IEDM 2008

Ernst et al. IEDM 2008

T_{Si}= 1 to 2 Lg

Thin Films Devices *Relaxing optimization scaling rule by architecture*

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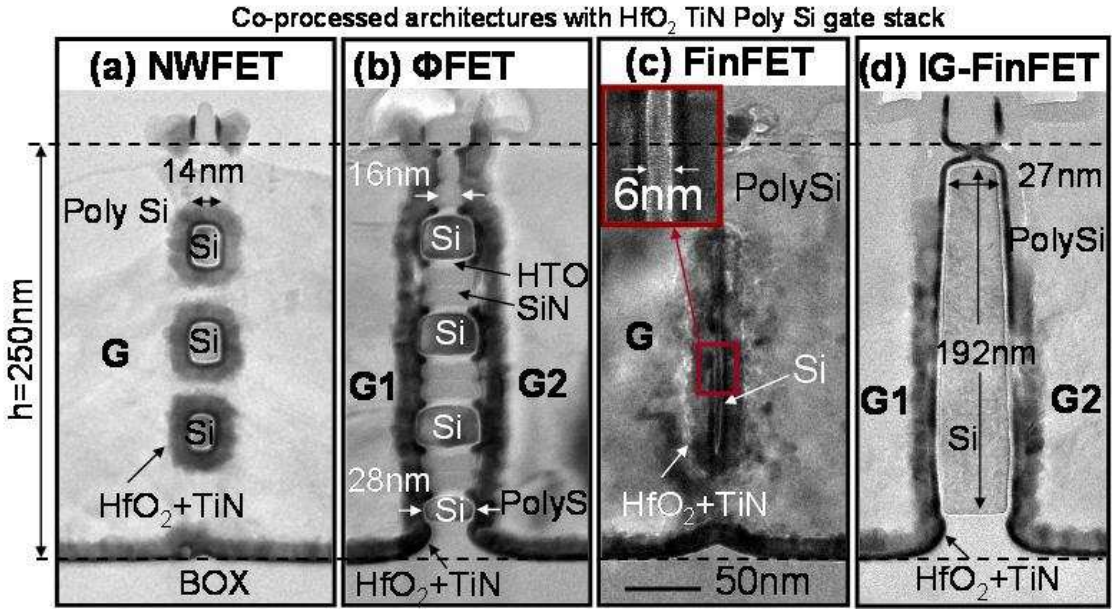
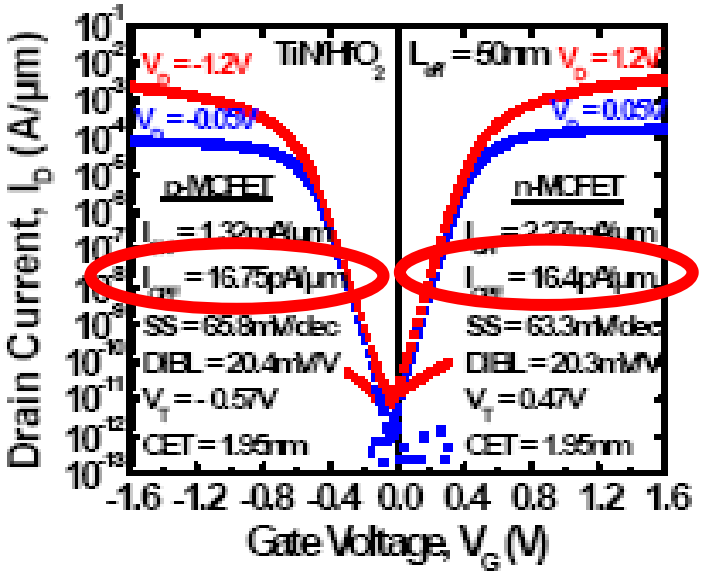
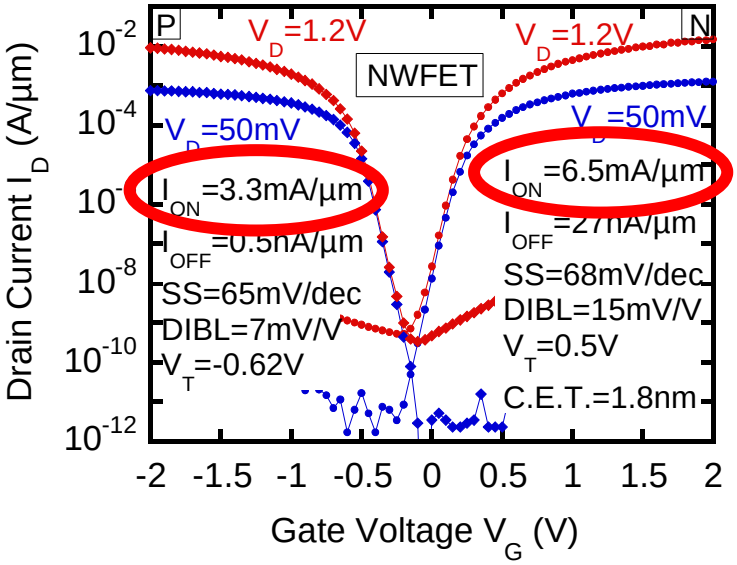
Stacked Multichannels and MultiNanowires « Top-Down » approach







LETI top down approach for
Low Power and High performance

-CV/I outperforms Planar in loaded environment
-Gate separation possible
-Transport properties in small nanowires
-Flexibility to tune channel conductance wrt FinFET
-Pervasion into microsystems (More than Moore)

LETI: Dupré et al. IEDM 2008, San Francisco(CA)
Ernst et al., Invited talk IEDM 2008, San Francisco(CA)
Bernard et al, VLSI Symposium 2008 Honolulu
K.Tachi et al., IEDM 2010, San Francisco

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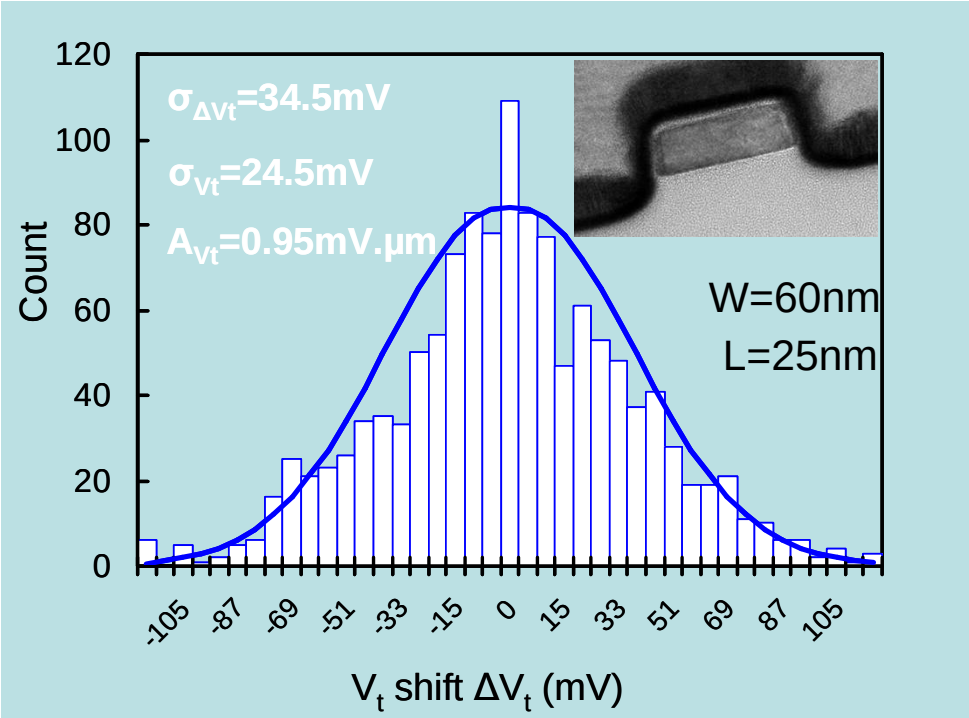
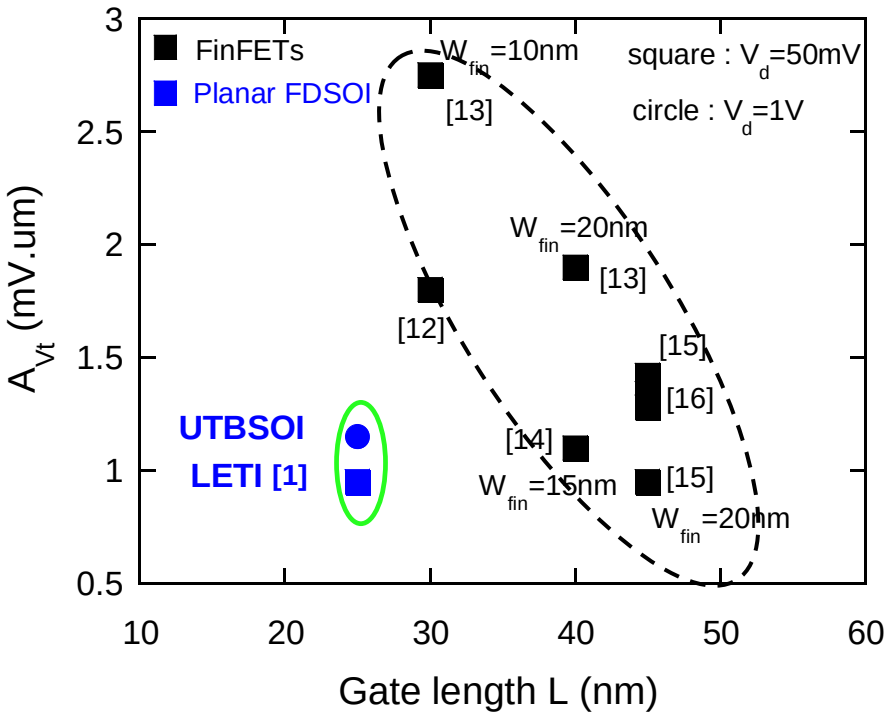
FDSOI Undoped channels vs.FinFET

Record-high V_T matching performance





LETI: O.Weber et al., IEDM 2008

$$\sigma_{Vt} = \frac{A_{Vt}}{\sqrt{WL}}$$

($\sigma_{Vt}=\sigma_{\Delta Vt}/\sqrt{2}$ to compare measurements on pairs and on arrays of transistors in the literature)

Best trade-off between V_T variations and gate length scaling compared to bulk MOSFETs and FinFETs

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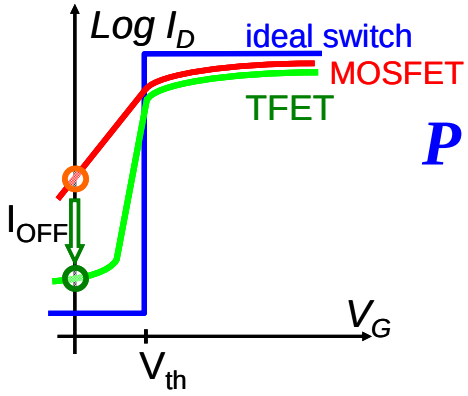
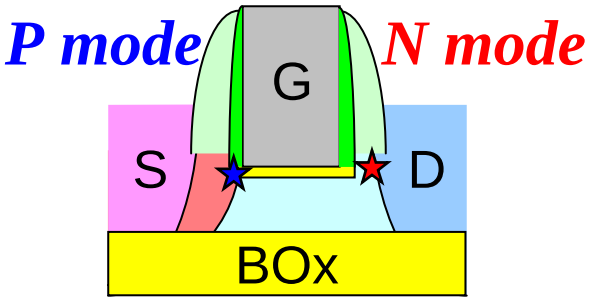
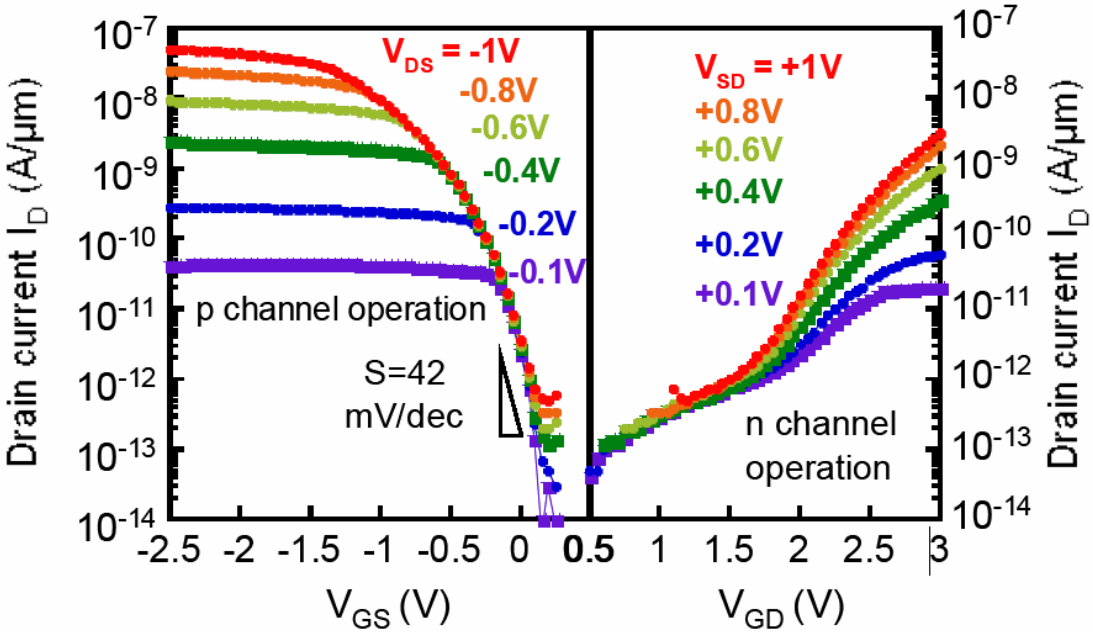
SOI TFETs co-integrated with CMOSFETs

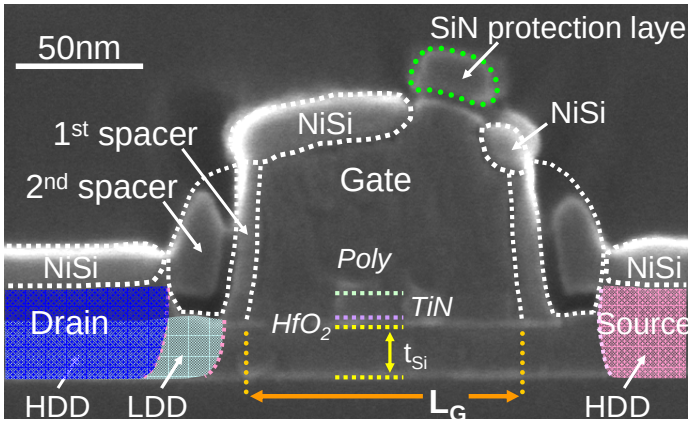




SOI TFET
w. LDDn

Experimental demonstration of Tunnel FET operations:





•P mode: V_{DS}<0 & V_{GS}<0 •N mode: V_{SD}>0 & V_{GD}>0

L=100nm; T=300K

F.Mayer et al., IEDM 2008,
C.LeRoyer et al., ULIS 2009

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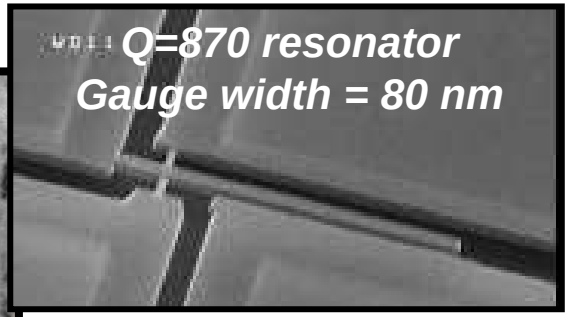
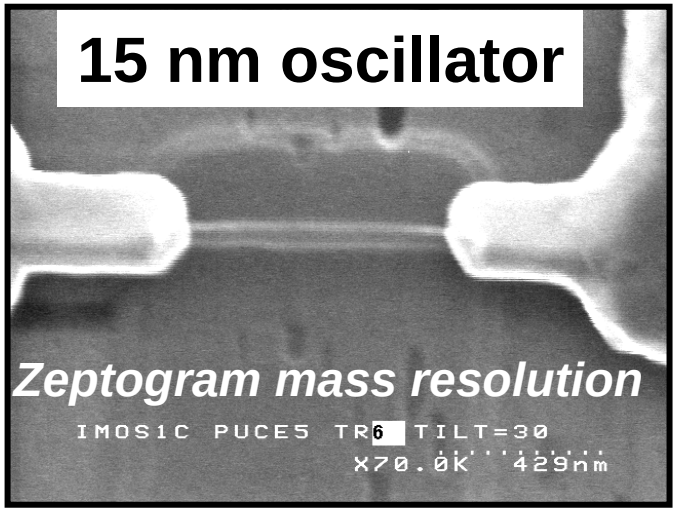
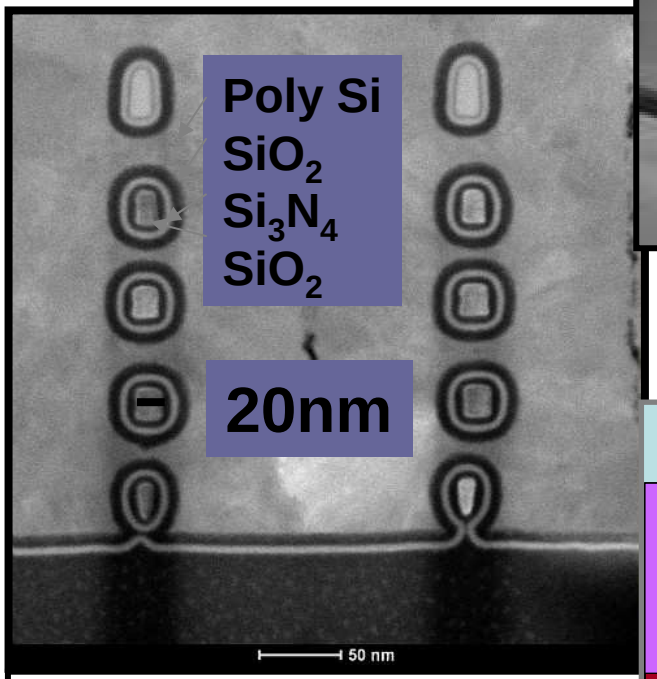
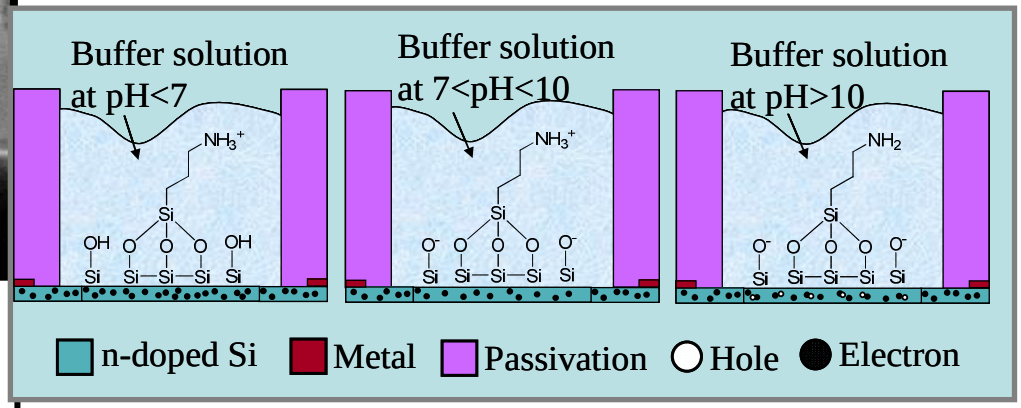
Pervasion of Nanowire technology: towards heterogenerous integration

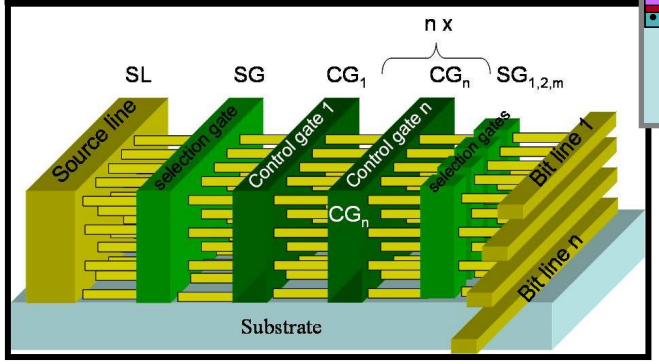
Mass detection







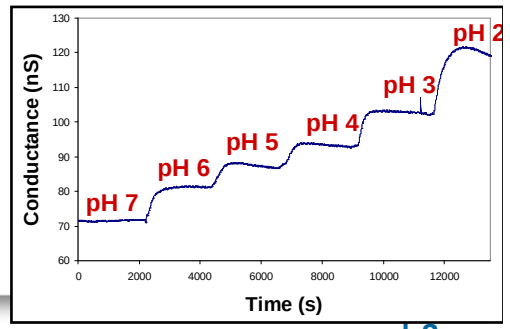




3D NAND Flash

Chemical sensing

T.Ernst et al., IEDM 2008
Hubert et al., IEDM 2009



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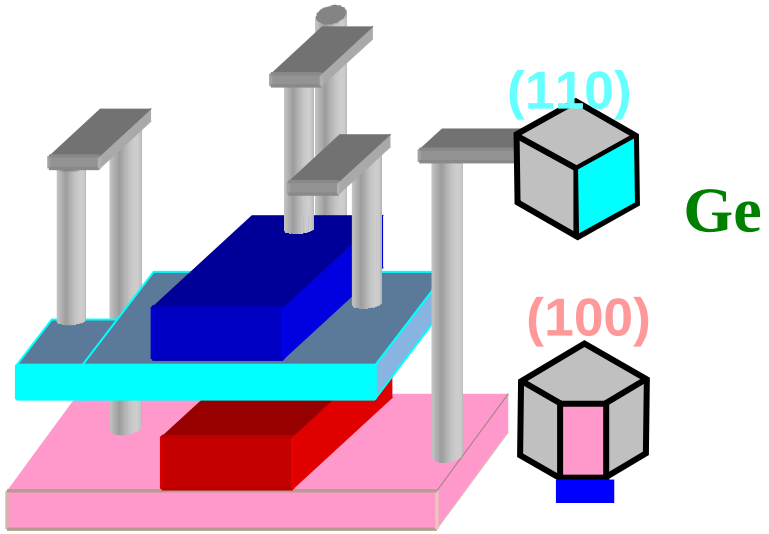
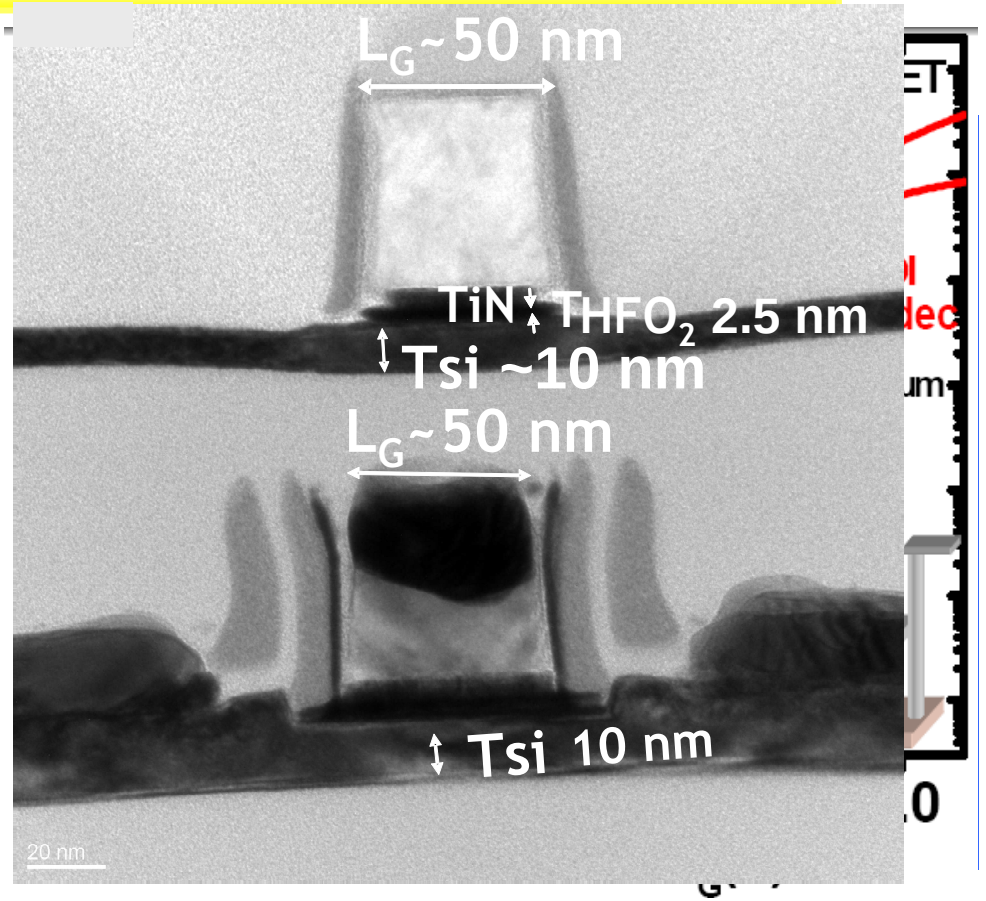
3D sequential process: one step ahead to

Co-Integrating Heterogeneous materials and devices





- cold end process(bonding) Improved Ig

Opportunities for other SC(Ge,III-V, C, ...)

- improved layout (40% area SRAM cell)
- 4T SRAM
- dynamically controlled VT:

improved RNM and SNM

P.Batude et al., Best student Paper Award, IEDM 2009

P.Batude et al, 2011 VLSI Tech Symp

First heterogeneous orientation in 3D Si sequential integration

Enabled by use of wafer bonding by keeping low thermal budget

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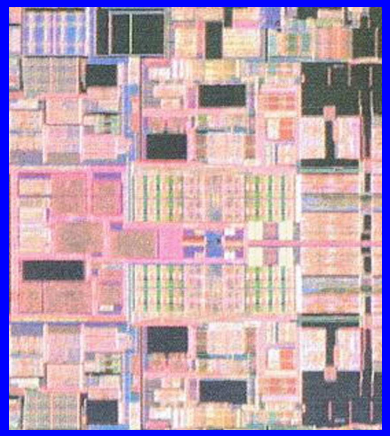
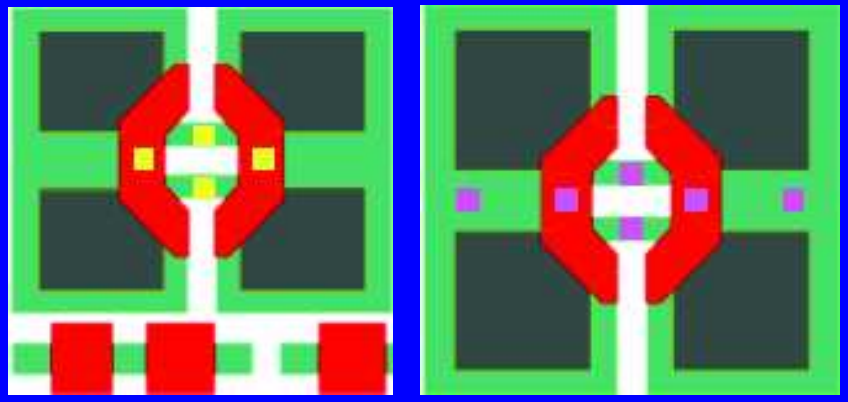
Sequential 3D: Potential and Demonstrated Applications

High density logic applications



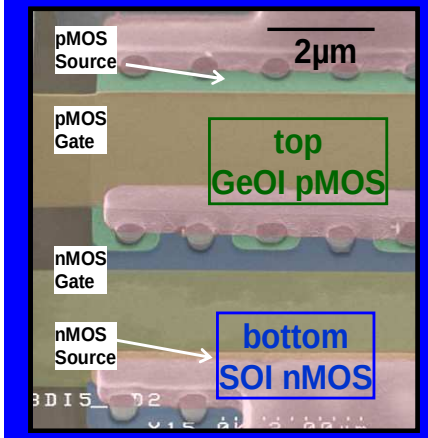
~ 1 node gain with same design rules for Front end levels

Highly miniaturized CMOS imagers pixels



P. Coudrain et al, IEDM 08,

Heterogeneous integration

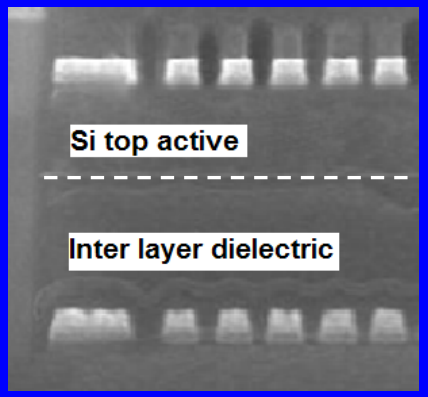


- Nanoelectronics & Photonics applications with Si-Ge Co-integration
- SRAM on top SOI logic, I/Os, analog on bottom bulk
- …

P. Batude et al,VLSI09

3D memories

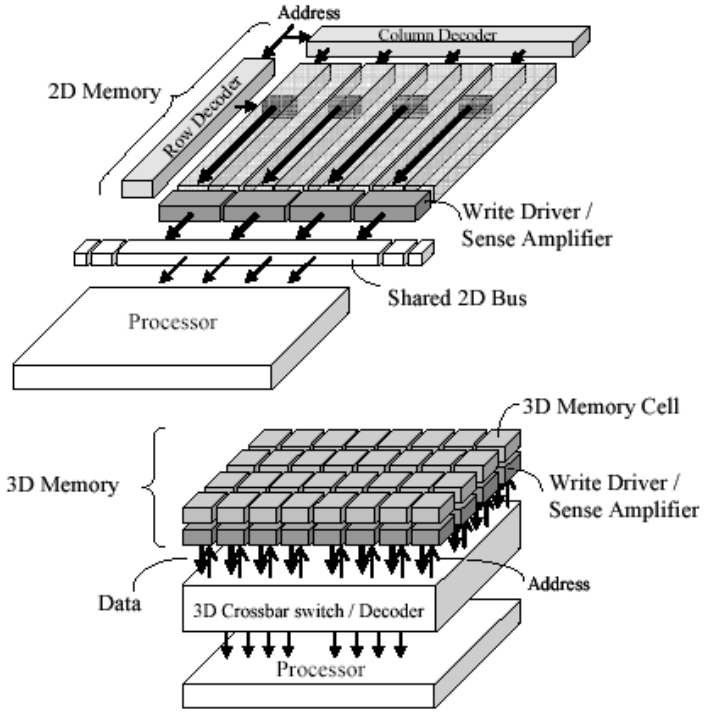
- SRAMs
- FLASH

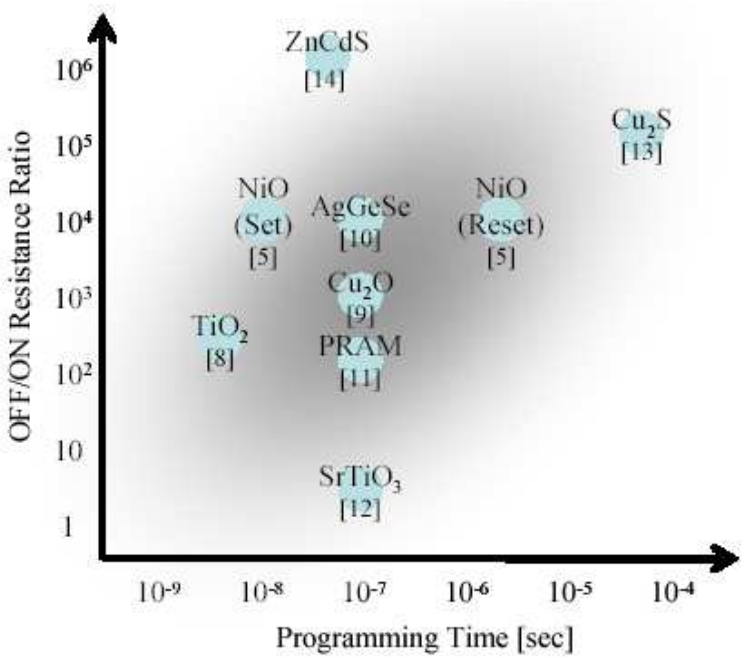


Y-H. Son et al, VLSI 07, Jung et al, IEDM 2006

P.Batude et al., IEDM 2009, Best Student Paper Award

3D-Xbar Memory stacked on Logic: towards NV Logic





Resistive switches

Toshiba, Stanford Univ.: K.Abe et al, ICICDT 2008; Suri et al. IEDM 2011

Logic + Stacked NVM: High bandwith, Reduced Power consumption,… Reconfigurable, Neuromimetic

ex: 32 nm node : > 1TB/s per $1mm^2$

proven in 2D with Magnetic Tunnel Junctions, FeRAM ***Tohoku Univ., Hitachi: S.Matsunaga et al., Appl.Phys. Express(2008); ROHM***

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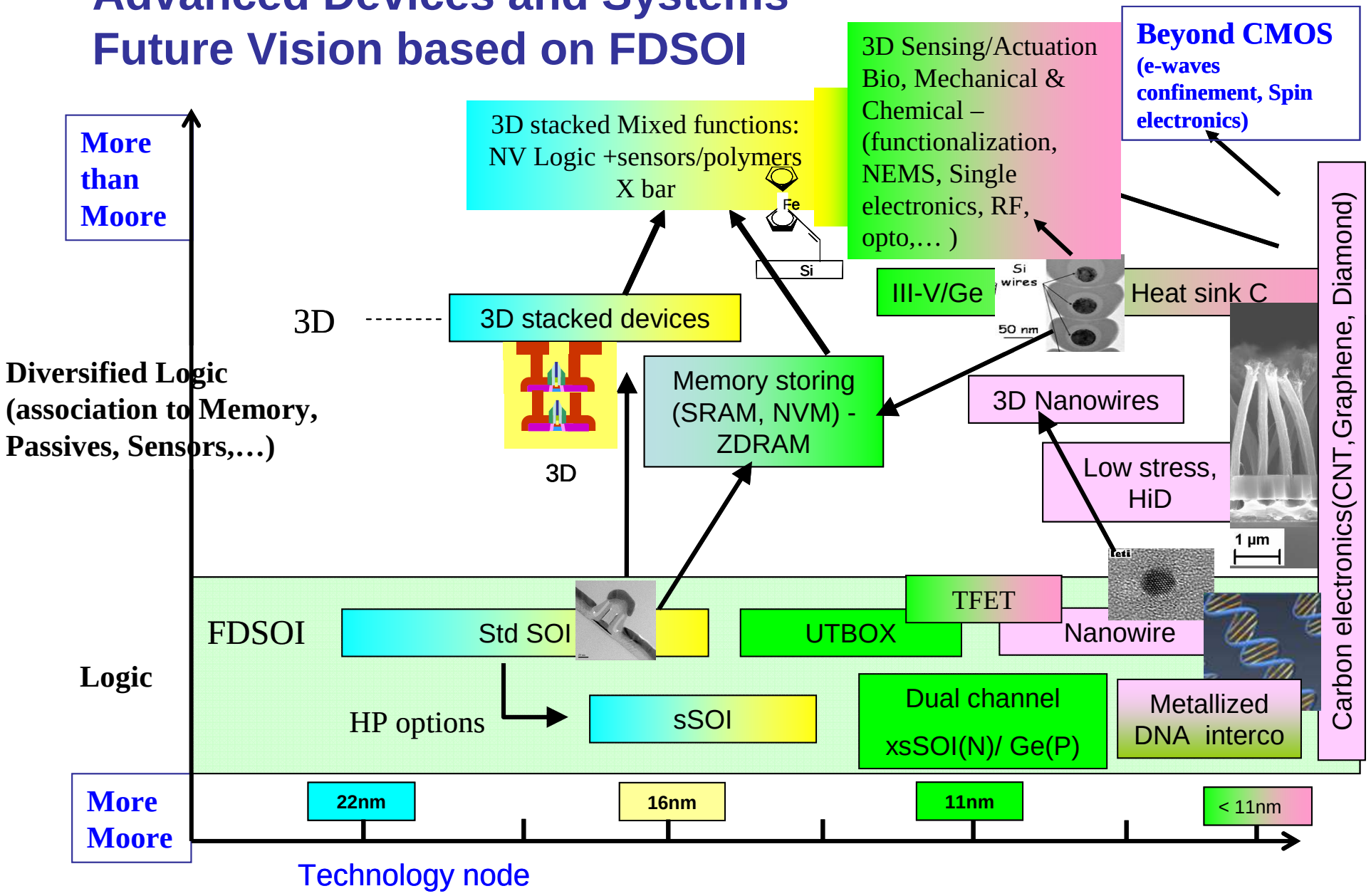
Advanced Devices and Systems Future Vision based on FDSOI



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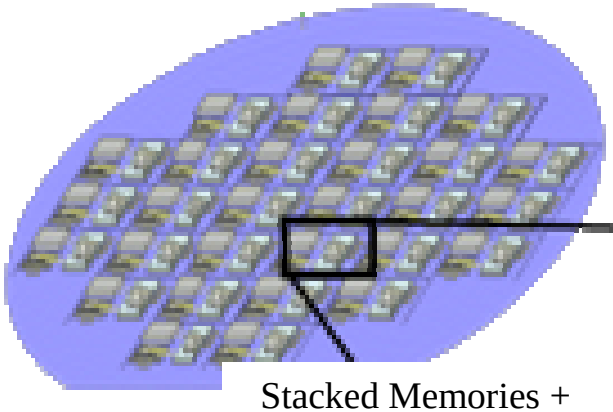
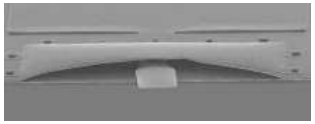
System On Wafer: Heterogeneous co-Integrated Systems

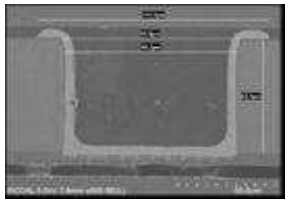
(Parallel 3D)



Stacked Memories +
Logic, Sensors,,…

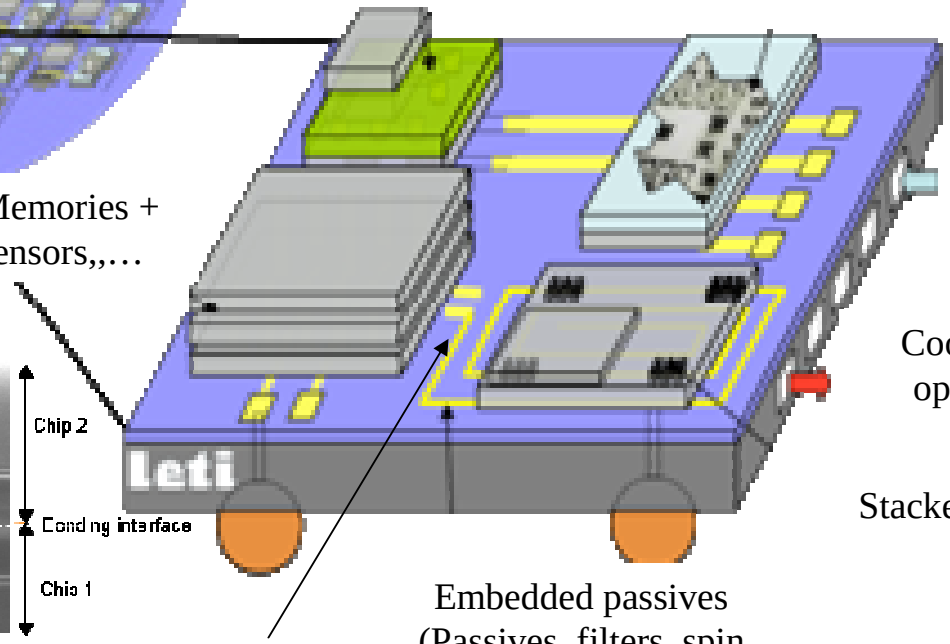


Wafer level packaged MEMS



Energy source
converter

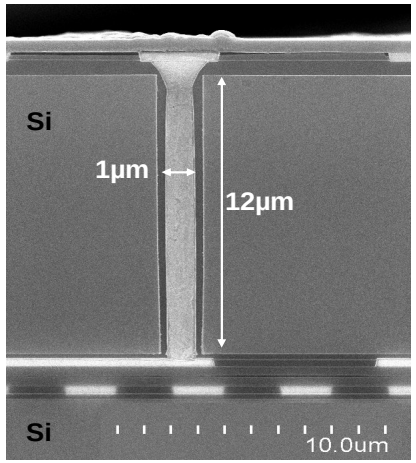
MEMS



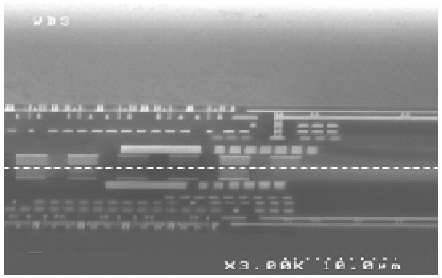
Cooling
option

Stacked ICs

80 µm diameter TSV imagers packaging



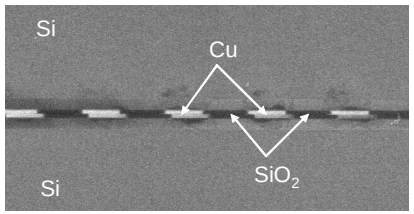
1 µm diameter
High AR TSV stacked ICs



Oxide/Oxide bonding

Optical Interconnects

Embedded passives
(Passives, filters, spin
torque osc,…)



Copper/Copper bonding

Heterogenous Integration On Silicon

Packaging is taken into account at the 3D wafer level

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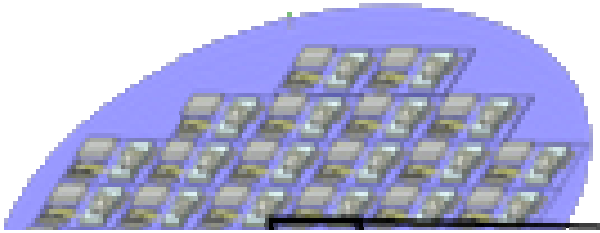
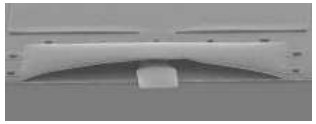
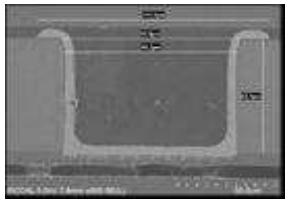
System On Wafer: Heterogeneous co-Integrated Systems

(Parallel 3D)



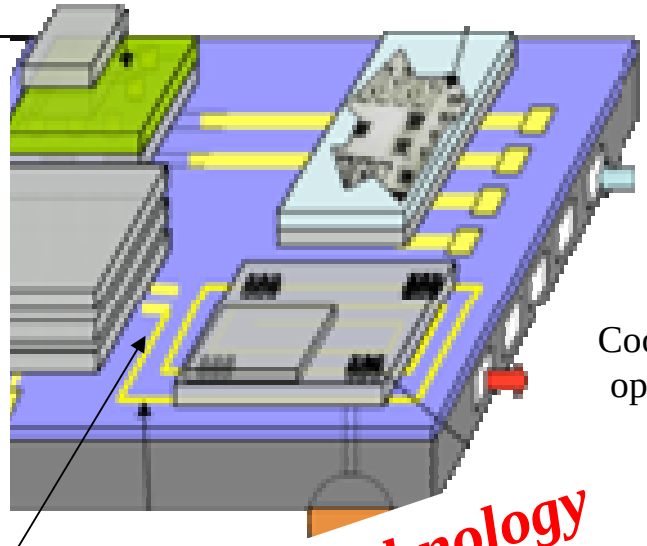




Energy source converter

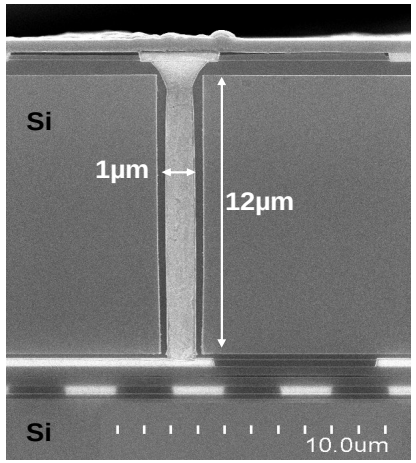
Wafer level packaged MEMS

MEMS



Cooling option

80 µm diameter TSV imagers packaging



1 µm diameter
High AR TSV stacked ICs

Commercial products

- image on board VGA camera,
- mixed nodes & modes,
- high density TSV

Cross talks:

-delay, matching,

-power dissipation
(global temp. increase,
hot spots, reliability, …)

Multiphysics

New Progress Laws

- application specific

Via belt technology
MEMS + IC stack
Ultra flat 3D
Chip stacking(TSV)
Active Silicon interposer

On Silicon

account

wafer level

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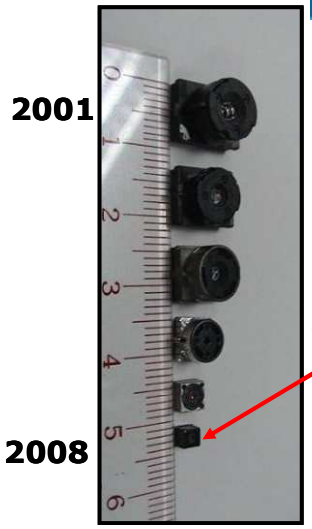
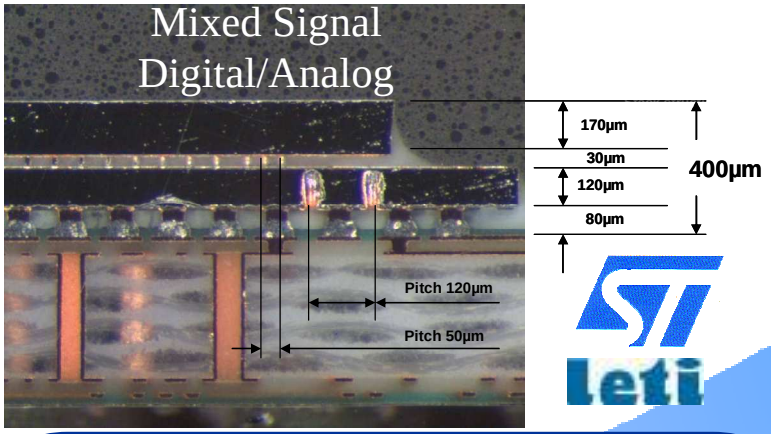
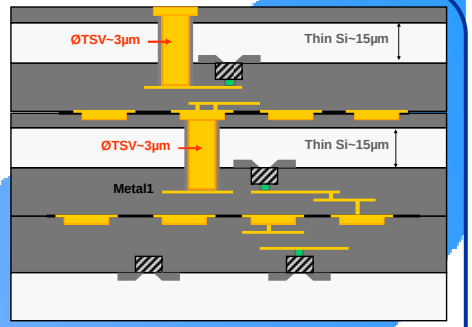
3D Integration: from imagers to advanced 3D ICs

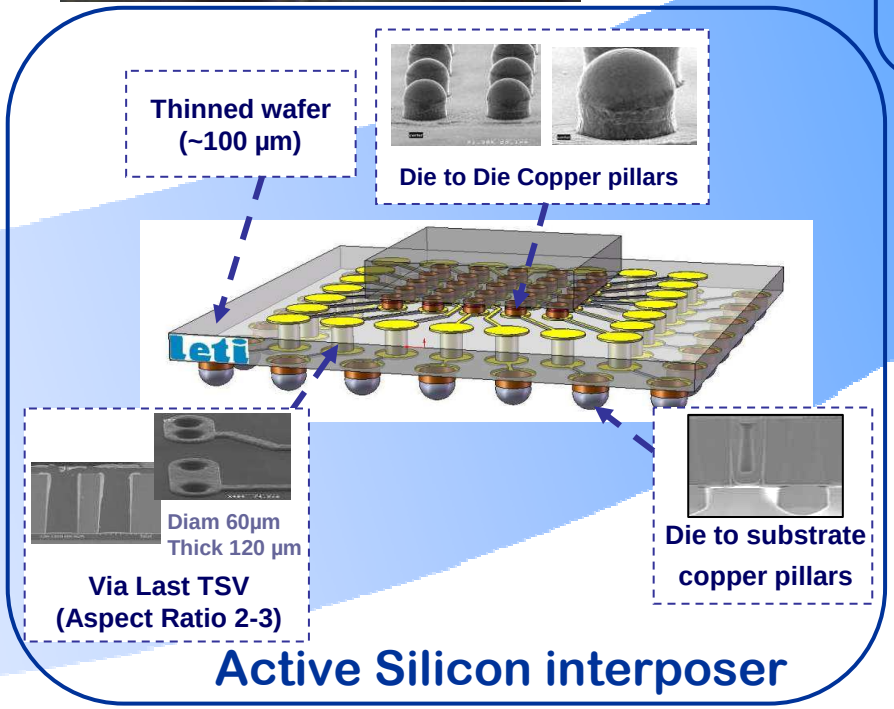


VGA cameras (300kpixels)





Memory, Processors, Imagers with high density TSV, NEMS…



3D high density

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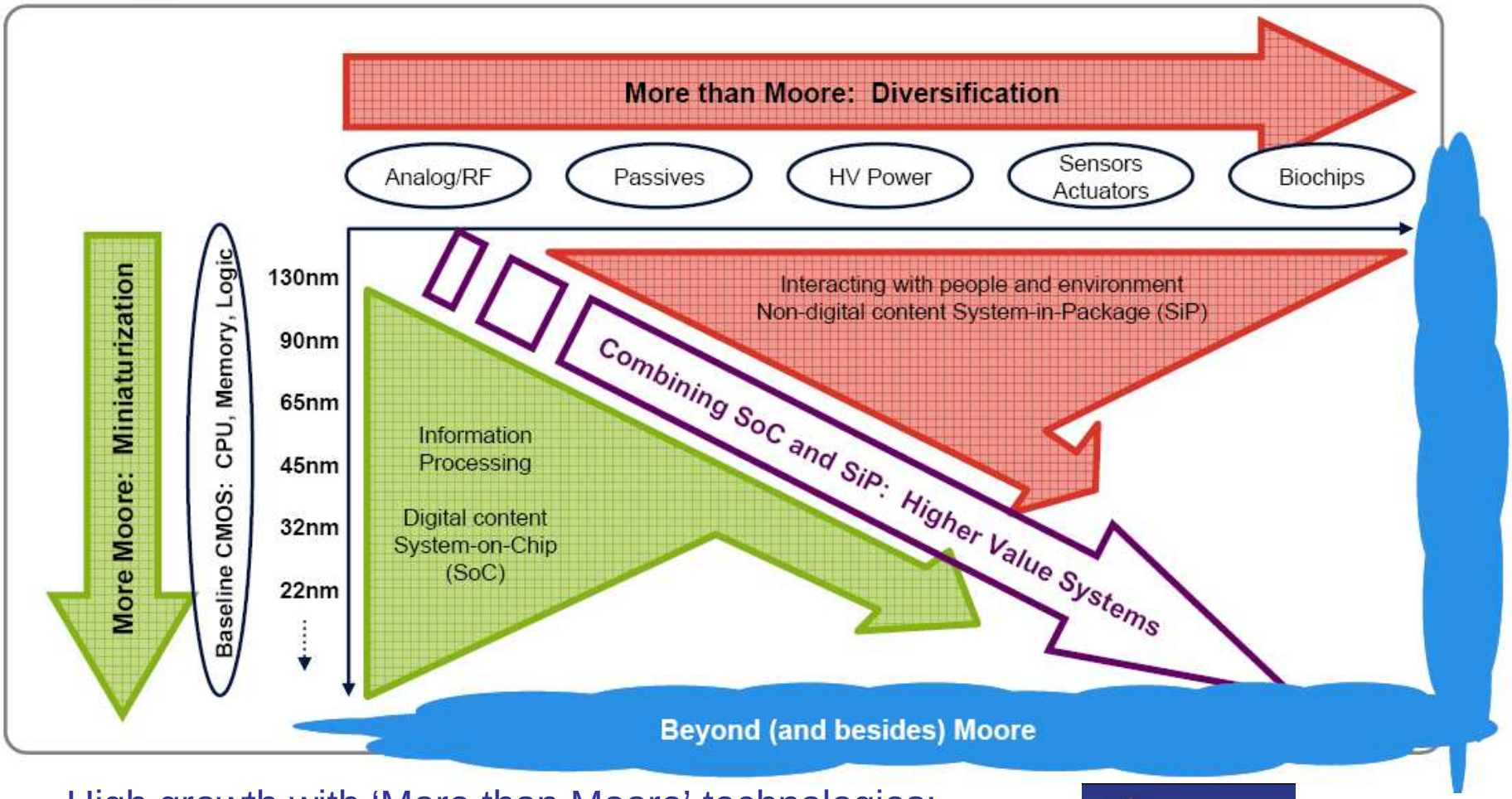
« More, More than, Beyond Moore »

Tomorrow's top added value markets



High growth with 'More than Moore' technologies:
they require expertise in all technical domains and in-depth knowledge of the targeted markets

ITRS 2009

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NEMS scaling laws: is it worth?

- potentially many applications : sensors, actuators(switches /RF, memory,…)
- resolution increases
- areal cross section decreases (SBR,SNR) => arrays, actuation,…
- figures of merit pressure and vacuum quality dependent

$$\delta m = \frac{M_{eff}}{Q} \cdot 10^{-(DR/20)}$$

$$DR \propto \sqrt{\frac{\sum S_{noise}}{P_{act}}} = \frac{1}{SNR}$$

ML Roukes et. al. APL (2005)

Parameter	Scaling rule
mass	k^3
stiffness	k
resonant frequency	k^{-1}
mass responsivity	k^{-4}
energy consumption	k^3 [rough estimate]

$$M_{eff} \propto l \cdot w \cdot t$$

$$\kappa_{eff} \propto w \cdot \frac{t^3}{l^3}$$

$$f_0 \propto \sqrt{\frac{\kappa_{eff}}{M_{eff}}} \propto \frac{t}{l^2}$$

$$\Re = \frac{\partial f_0}{\partial M_{eff}} = -\frac{f_0}{2M_{eff}}$$

$$E_P \approx \frac{1}{2}\kappa_{eff} \cdot x_{Max}^2$$

and $x_{Max} \propto t$

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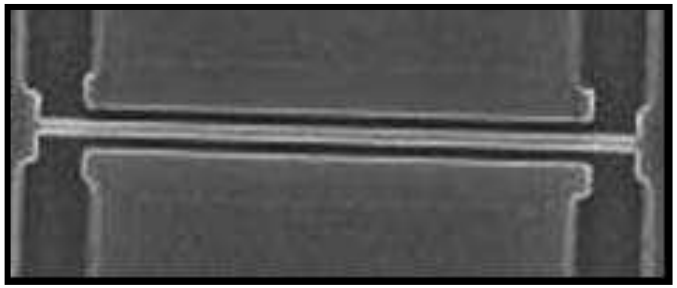
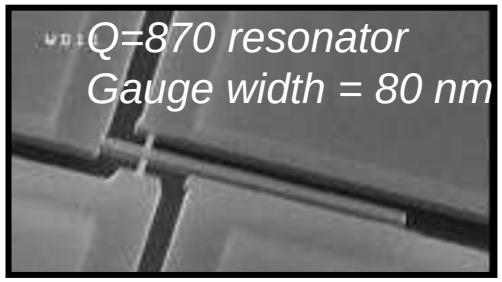
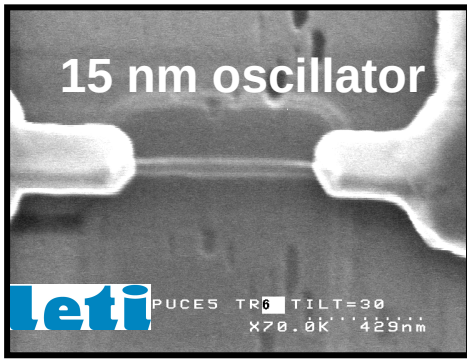
Nanowires & Arrays used for mass detection

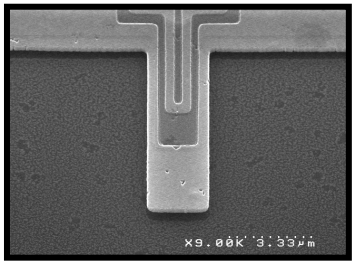




$$\delta m \approx 0.5\ zg/\sqrt{Hz}$$

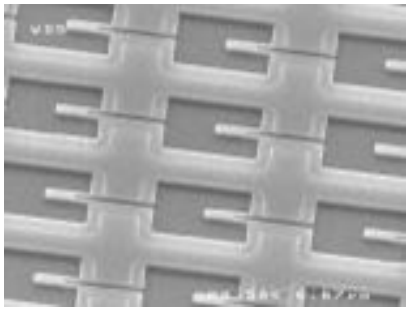


Capacitive actuation & detection

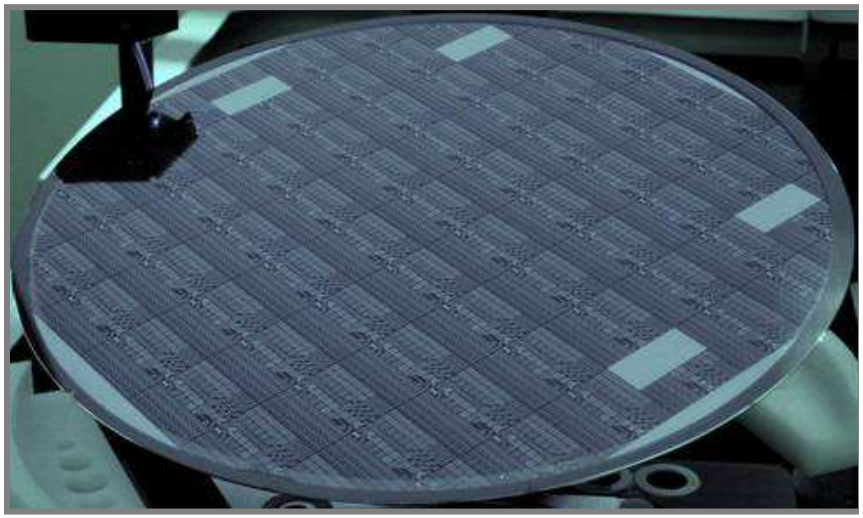


Thermo-elastic actuation & piezo-resistive detection.

Capacitive actuation & piezo-resistive detection with nanowires



NEMS array



leti

- *First 200 mm wafers with 3.5 millions NEMS*
- *Association Nanowire/Resonator ; Cantilever arrays CMOS compatible*

LETI: T.Ernst et al., IEDM 2008, Invited talk
L. Duraffourg et. al, APL 92, 174106 (2008)
E Mille et al, Nanotechnology, 165504, (2010)
J.Arcamone et al. , IEDM 2011

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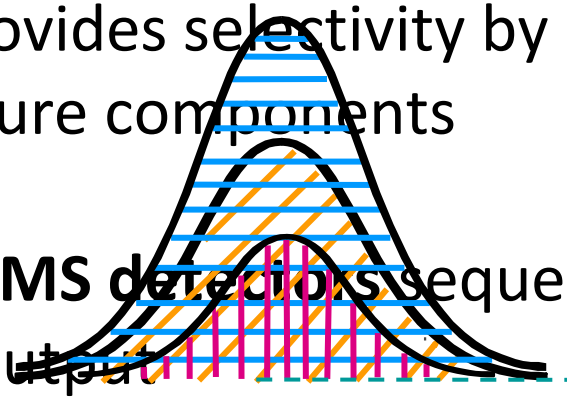
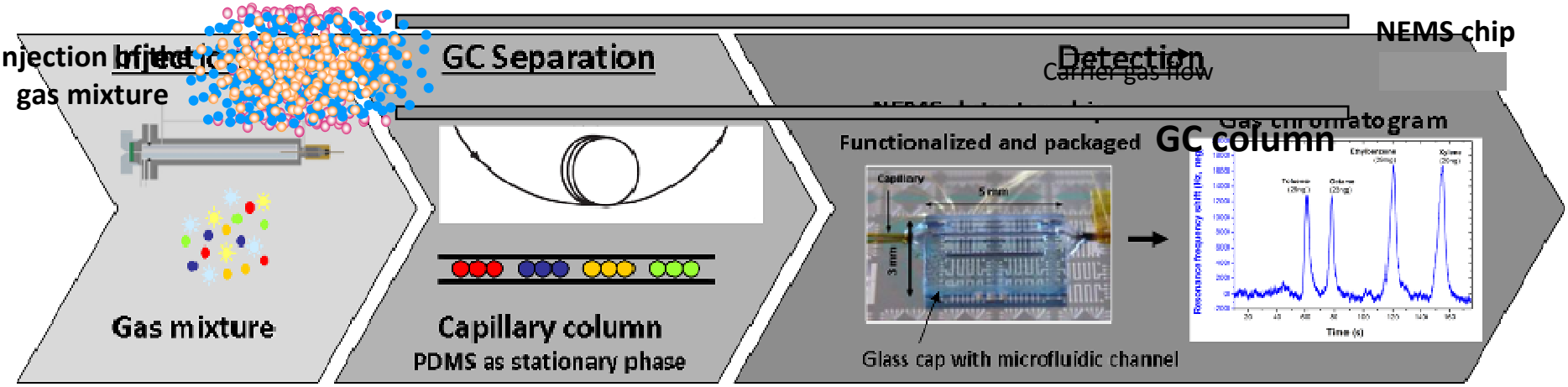
A possible solution: coupling GC and NEMS

- **Gas Chromatography (GC)** is a well-known separation method
It provides selectivity by separating in time and space the gas mixture components



J.Arcamone et al. , IEDM 2011

- **NEMS detectors** sequentially detect the elution peaks at the GC output



- **Both GC column and NEMS detectors can be fabricated** with VLSI silicon micro / nanofabrication techniques

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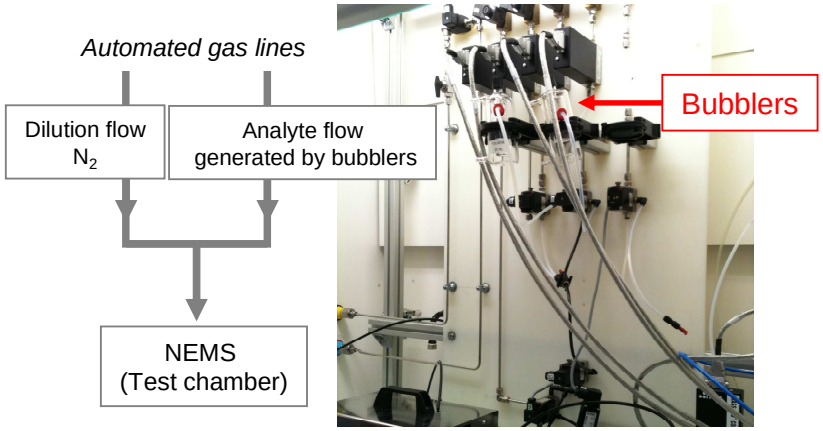
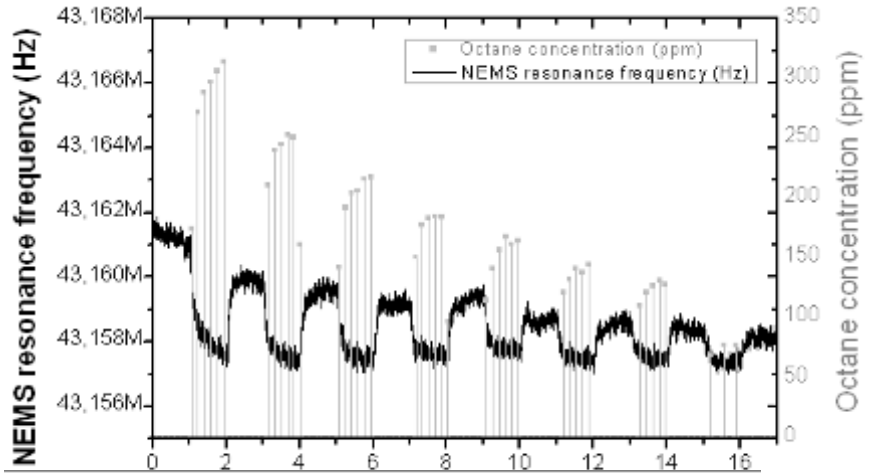
Specific constraints related to gas sensing: NEMS functionalization

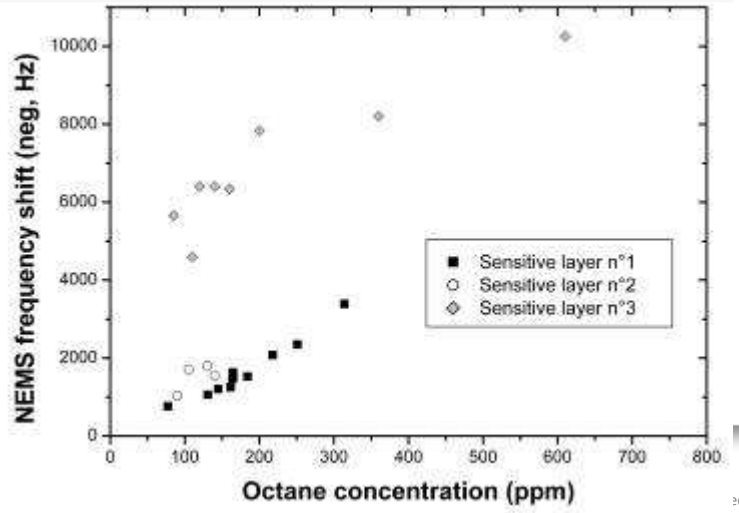
- **deposition of sensitive layers** (they have to absorb everything)
- targeted gases: **alkanes** (for instance, octane) and **volatile organic compounds** (toluene, xylene, etc…)
- every coating layer is characterized (at equilibrium) in a gas test bench



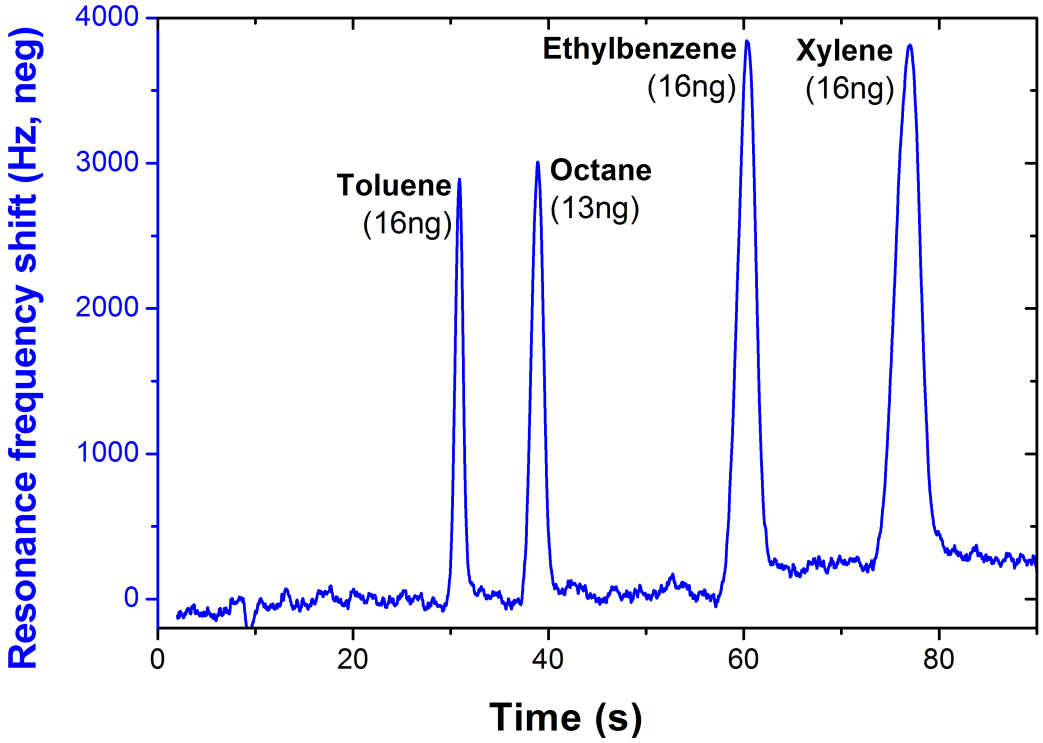


Resonators exposed to sequences of
[carrier gas / carrier gas + analyte]
→ determination of *K* coefficients

J.Arcamone et al. , IEDM 2011



Gas recognition: multigas analysis



J.Arcamone et al. , IEDM 2011

Partnership:

spin off from
LETI and Caltech

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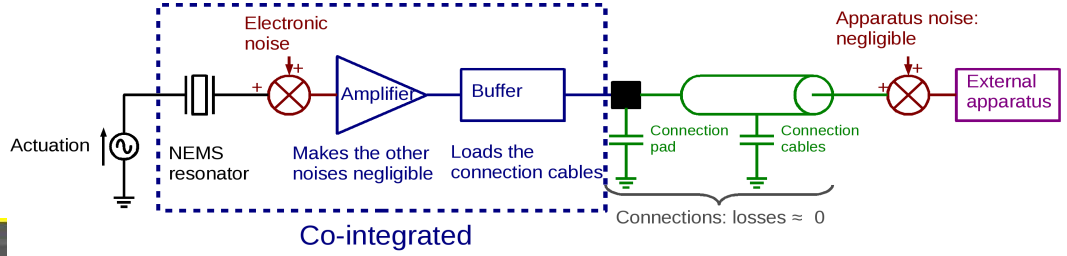
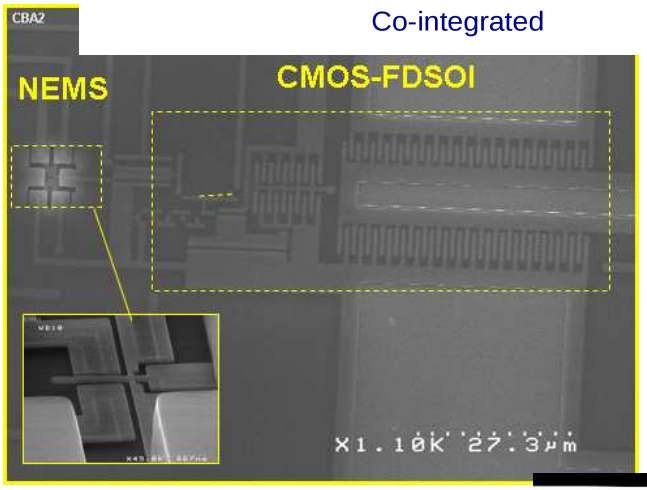
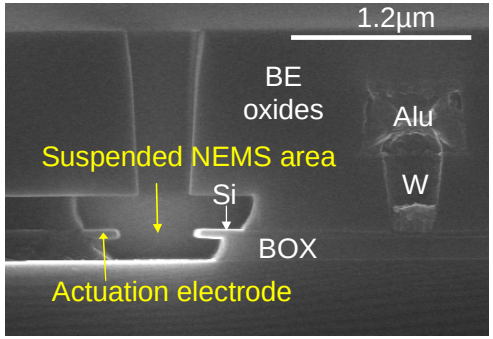
Front-end co-integration of ultra-scaled Si NEMS with FDSOI CMOS

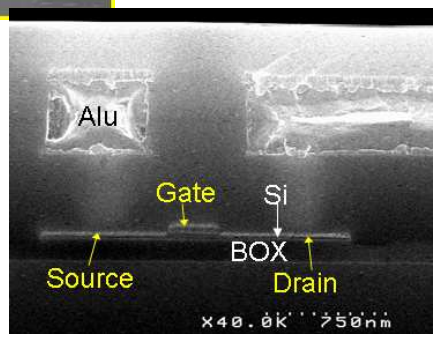
Integration of first amplification stage enables direct measurement of small electrical signals provided by the NEMS resonators (40nmx40nm cross section)



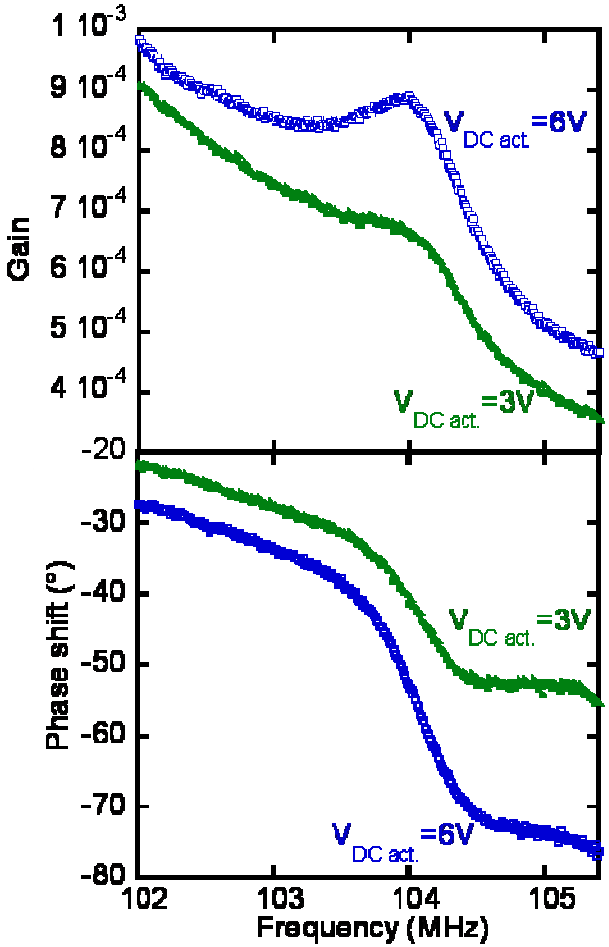




NEMS part



CMOS part



LETI: E.Ollier, C.Dupré, IEEE MEMS 2012

EU NEMSIC project

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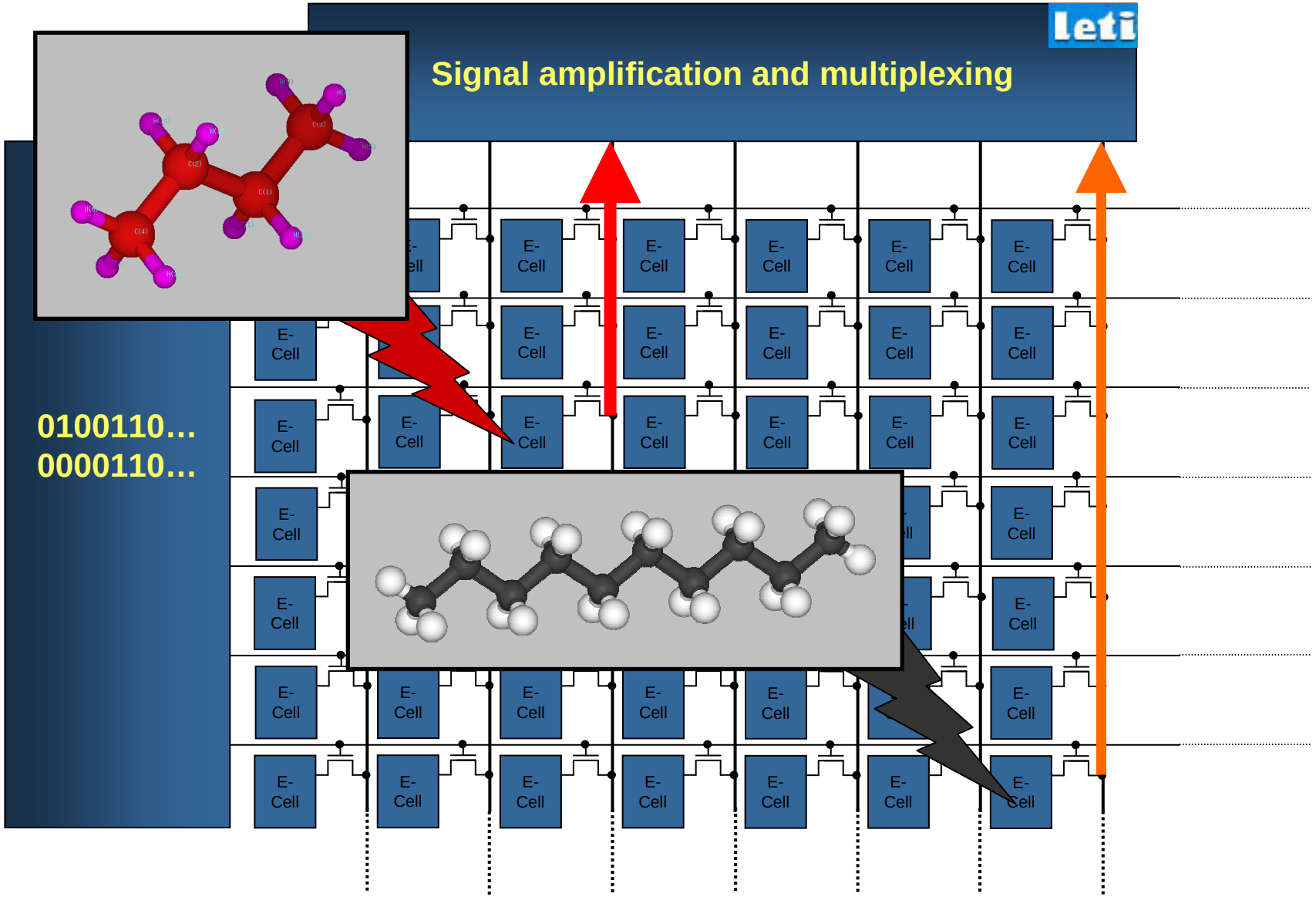
A multi-physics system vision

EUROPEAN COMMISSION
7th Framework Programme on
Research, Technological
Development and Demonstration



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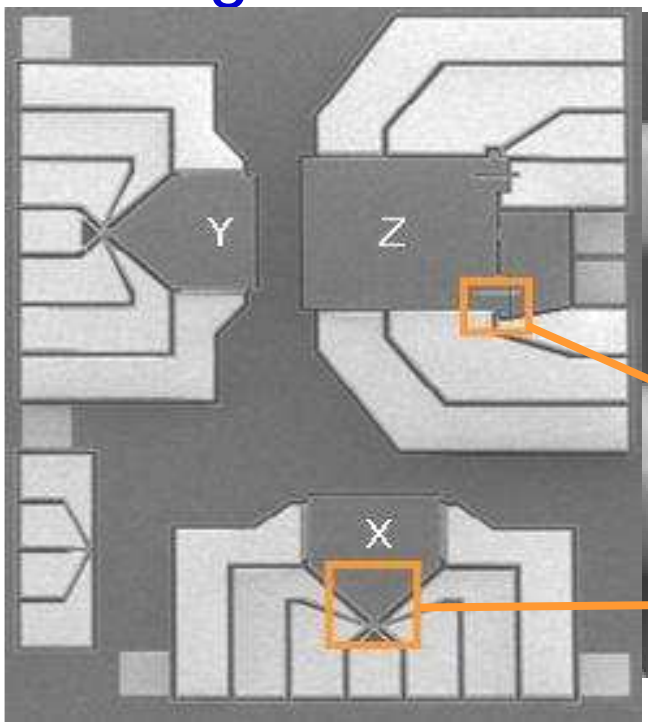
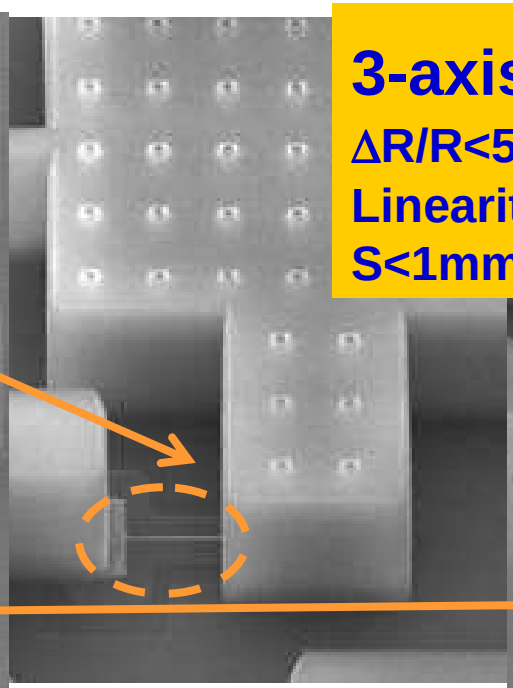
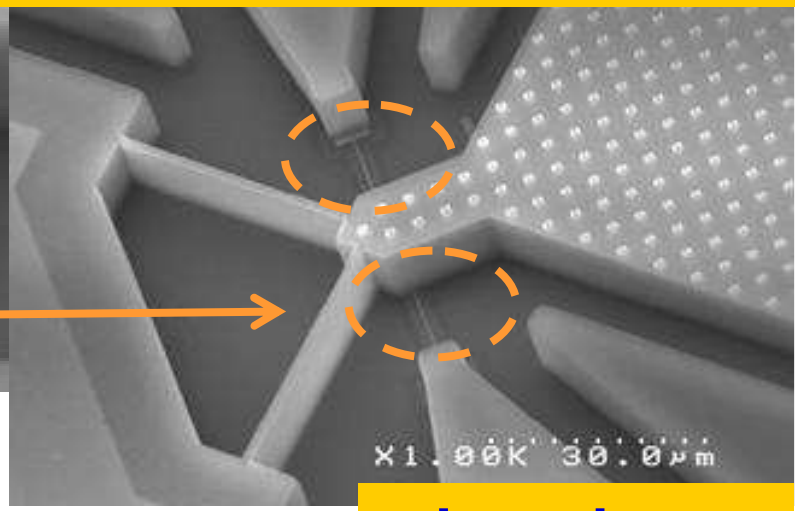
M&NEMS co integrated devices platform for 3D sensing







3-axis accelerometer

$\Delta R/R<5x10^{-4}$ (±1g)
Linearity <0.3% (0 and 200MPa)
S<1mm2 (3 axis)

Area ÷4 vs SoA

Nanobeams

3-axis gyroscope

$F_0 \approx 20.3$ kHz
Q > 100.000 S=0.8mm² / axis

P.Robert et al, 2009 IEEE Sensors
D.Ettelt et al, 2011 Transducers

3D magnetometer

Resol 20-80 nT/√Hz
Lin 4.5 mT
S=0.25 mm²/axis

microphone

pressure sensor

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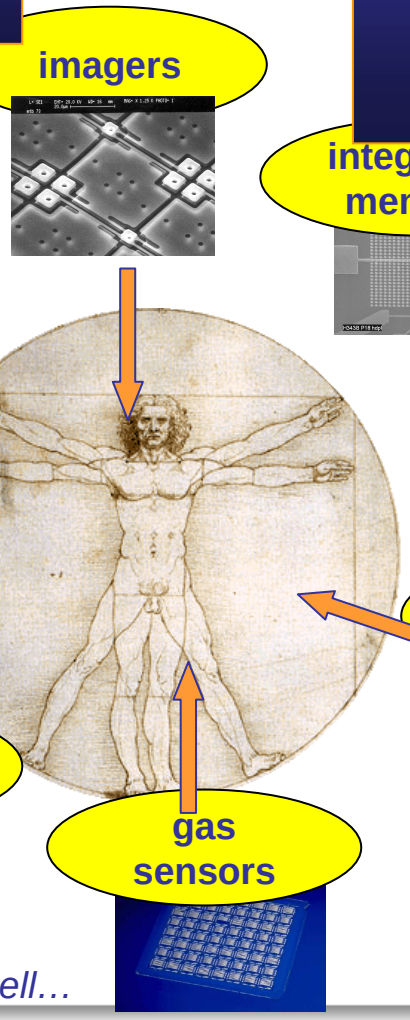
Closer to « human processing »…

Nowadays : independent replications of senses in different domains

objective

- ***Sense in various domains***
- ***Communicate***
- ***Fusion***
- ***Interpret***

→ Improve quality of life



…and more/"augmented"
… with ethics!

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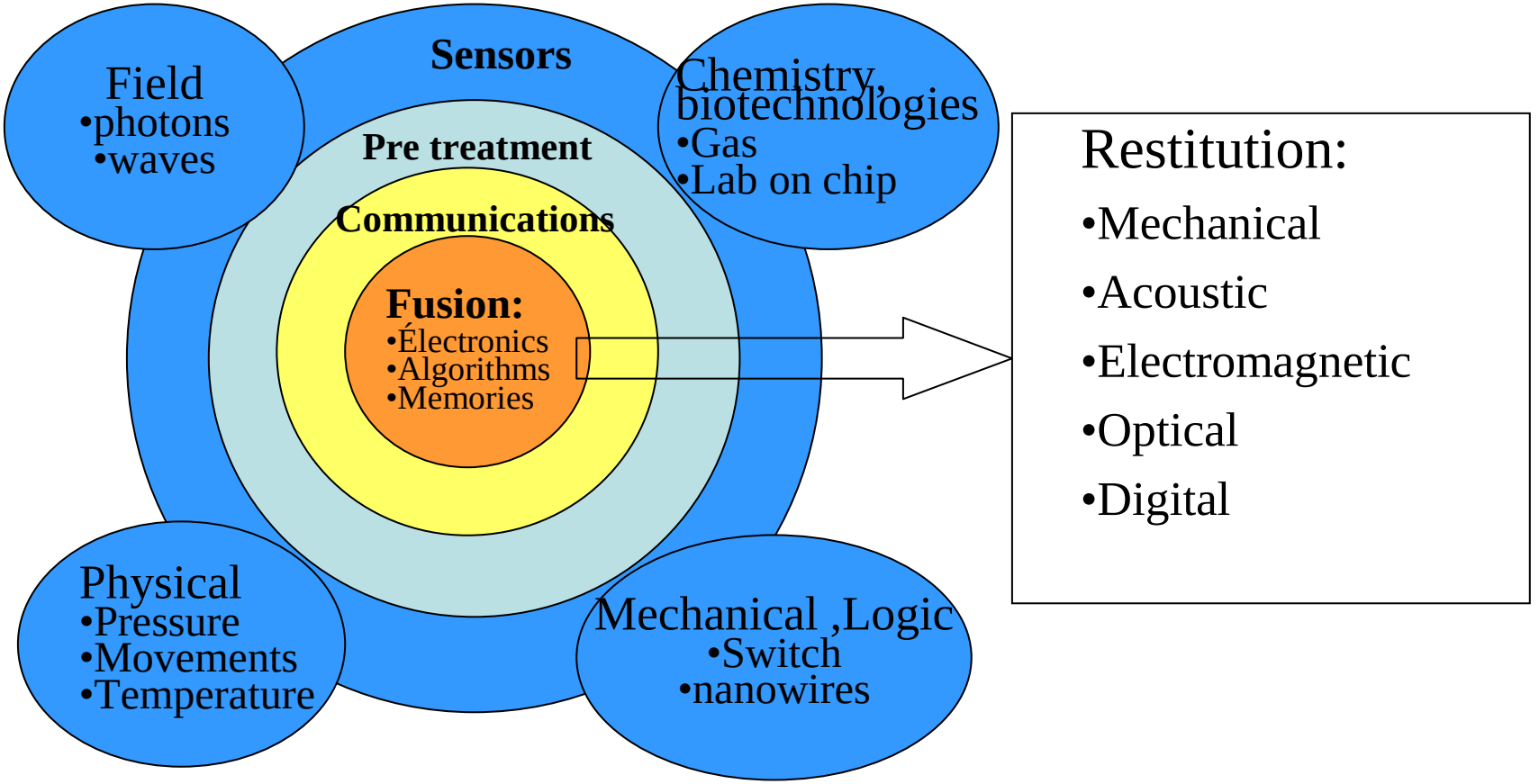
Multi Sensorial Extended System /Fusion,Intelligent communication



Applications: assistance , security (home, industrial, medical), surveillance, diagnostic, medical care, environment ,food, agriculture

To be published

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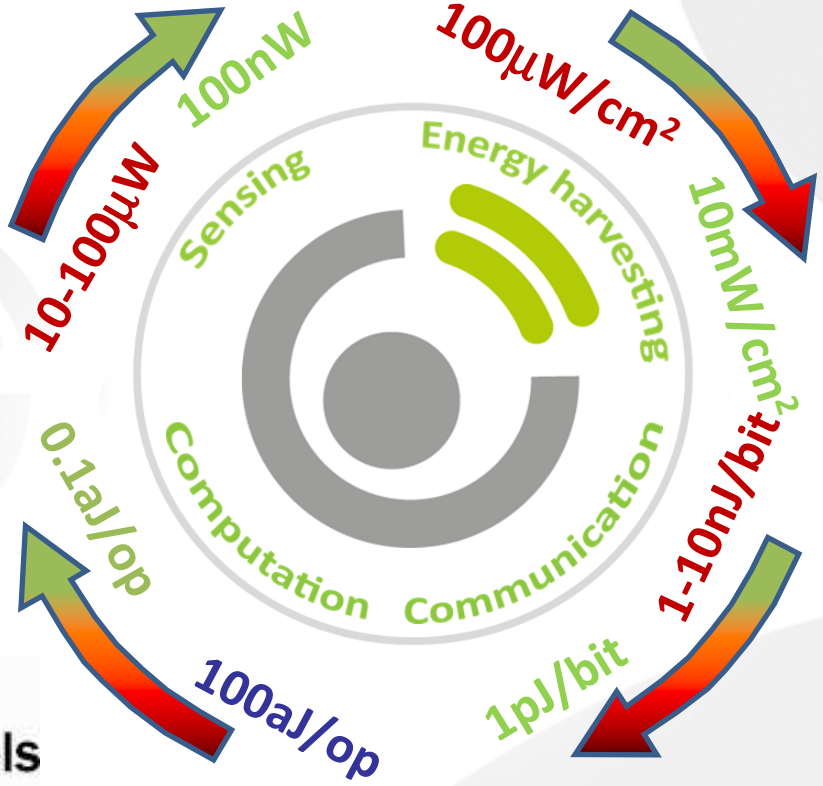
Zero power and science drive

- **Zero-power is the system ability to harvest energy** existing in dynamic environments (solar, thermal, vibrations, electromagnetic) and power-up the smart GA systems.
- **Science drive**: energy efficiency limits and disruptive harvesters.



Guardian Angels
for a smarter life

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Conclusion : Nano–« electronics and systems » from Devices to Systems Perspectives

- **Innovation from strong association of**
  System/Device/Materials Science and Engineering
- **Si CMOS: Nanoelectronics Base platform beyond ITRS**
- **Low Power consumption: major challenge to Zero Power.**
  Device/ system architecture optimization
  (GAA nanowires, low slopes,design, 3D)
  Opportunities for new materials(revised low BG III-V, Carbon based ,…)
- **Heterogeneous 3D co-Integration on Si, Low Power:**
  Co integration : Add Functionalities for diversification, Sensors, actuators,
  NonCMOS & CMOS, Monolithic, 3rd dimension in device,
  Stacked mixed functions, System On Wafer
- **System Design towards Fusion:**
  New Design Models, Multiphysics, Intelligent communication ,
  Health, environment, quality of life, IST,food/agriculture, industrial control,…

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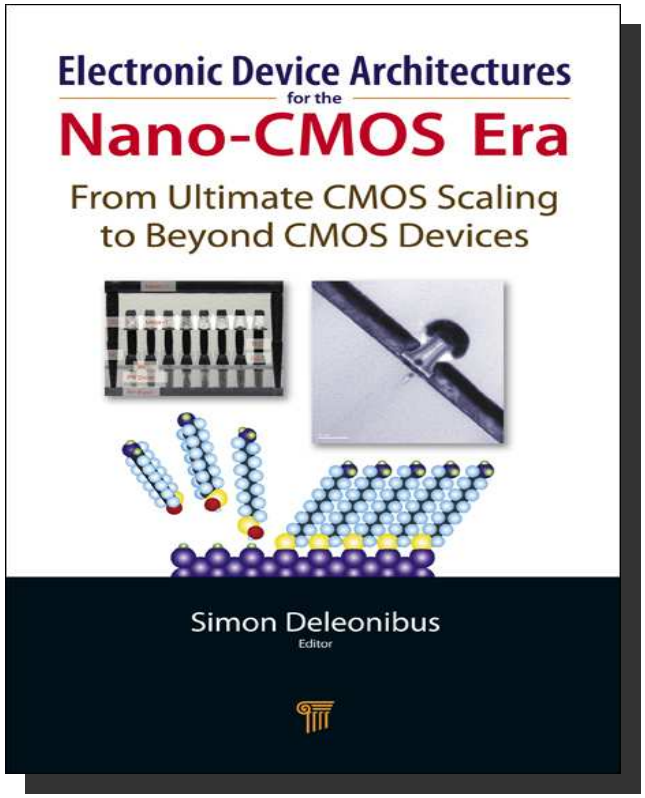
Thank you for your attention

Merci de votre attention



Electronic Device Architectures for the Nano-CMOS Era

From Ultimate CMOS Scaling to Beyond CMOS Devices

edited by Simon Deleonibus (*CEA-LETI, France*)

Cloth July 2008 978-981-4241-28-1

★ Discusses the scaling limits of CMOS, the leverage brought by new materials, processes and device architectures (HiK and metal gate, SOI, GeOI, Multigate transistors, and others), the fundamental physical limits of switching based on electronic devices and new applications based on few electrons operation

★ Weighs the limits of copper interconnects against the challenges of implementation of optical interconnects

★ Reviews different memory architecture opportunities through the strong low-power requirement of mobile nomadic systems, due to the increasing role of these devices in future circuits

★ Discusses new paths added to CMOS architectures based on single-electron transistors, molecular devices, carbon nanotubes, and spin electronic FETs

Available at Amazon.com or any good bookstores.

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Sensor Type	Advantages	Disadvantages
Calorimetric or catalytic bead (CB)	Fast response and recovery time, high specificity for oxidized compounds	High temperature operation, only sensitive to oxygen-containing compounds
Catalytic field-effect sensors (MOSFET)	Small sensor size, inexpensive operating costs	Requires environmental control, baseline drift, low sensitivity to ammonia and carbon dioxide
Conducting polymer sensors	Ambient temperature operation, sensitive to many VOCs, short response time, diverse sensor coatings, inexpensive, resistance to sensor poisoning	Drift & lifetime limit due to oxidation, sensitivity to humidity & temperature, saturation of response, bulky size, sensitivity limited
Electrochemical sensors (EC)	Ambient temperature operation, low power consumption, very sensitive to diverse VOCs	Bulky size, limited sensitivity to simple or low molecular weight gases
Metal oxides semiconducting (MOS)	Very high sensitivity, limited sensing range, rapid response and recovery times	High temperature operation, high power consumption, limited sensor coatings, sensitive to humidity, poor precision
Optical sensors	Very high sensitivity, capable of identifications of individual compounds in mixtures, multi-parameter detection capabilities	Complex sensor-array systems, more expensive to operate, low portability due to delicate optics and electrical components
Quartz crystal Microbalance (QMB)	Good precision, diverse range of sensor coatings, high sensitivity	Poor signal-to noise ratio, difficult arrayability (discrete), limited sensitivity to low molecular weight analytes, bulky
Surface acoustic wave (SAW)	High sensitivity, good response time, diverse sensor coatings, small, inexpensive, sensitive to virtually all gases	Complex circuitry, power consumption
Organic thin film transistors (OTFT)	Multi-parameter detection capabilities, cost	Sensitivity, limited material-analyte compatibility, sensor life, sensing mechanism not yet well-understood, complex circuitry for multiparameter

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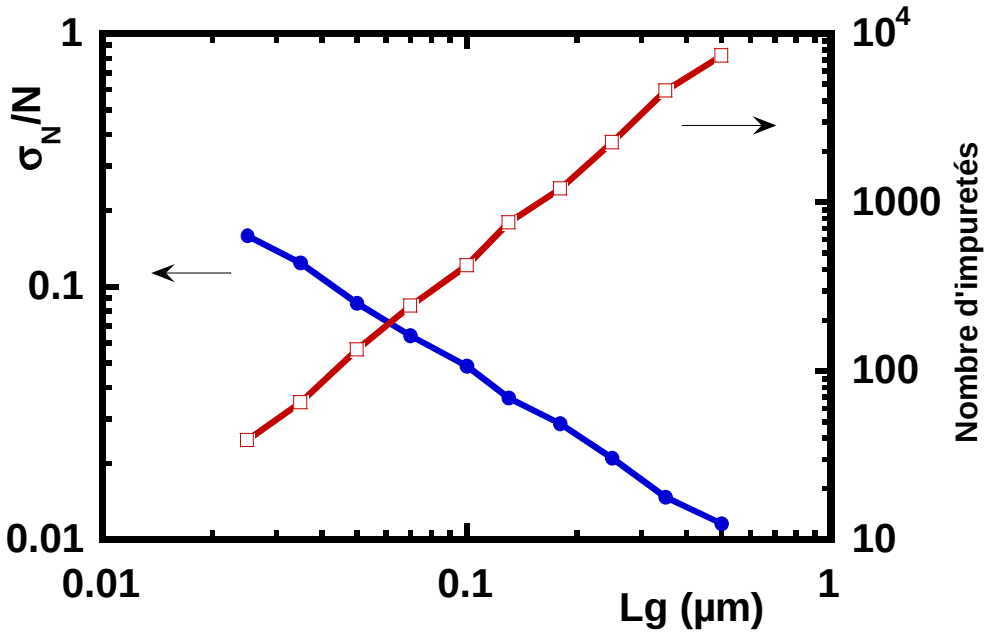
Hot Topics: parasitic effects in MOSFET technology

- Introduction of HiK and metal gate allows continued scaling and relaxes SiO2 gate leakage current related issues **- Ig added to SCE, DIBL, subthreshold leakage(LETI IEDM 2002, Intel IEDM 2005)**
- Statistical dopant variability

  - number of dopants in the active area decreases with scaling

  - random distribution of channel dopants

  Poisson's law. Standard deviation:



$$\sigma_{doping} = \left(\frac{N}{Volume} \right)^{1/2}$$

Statistical fluctuations of threshold voltage: 150 mV decay for VT=200mV(Lg=25nm) !!

Major interest for Low Doped channels

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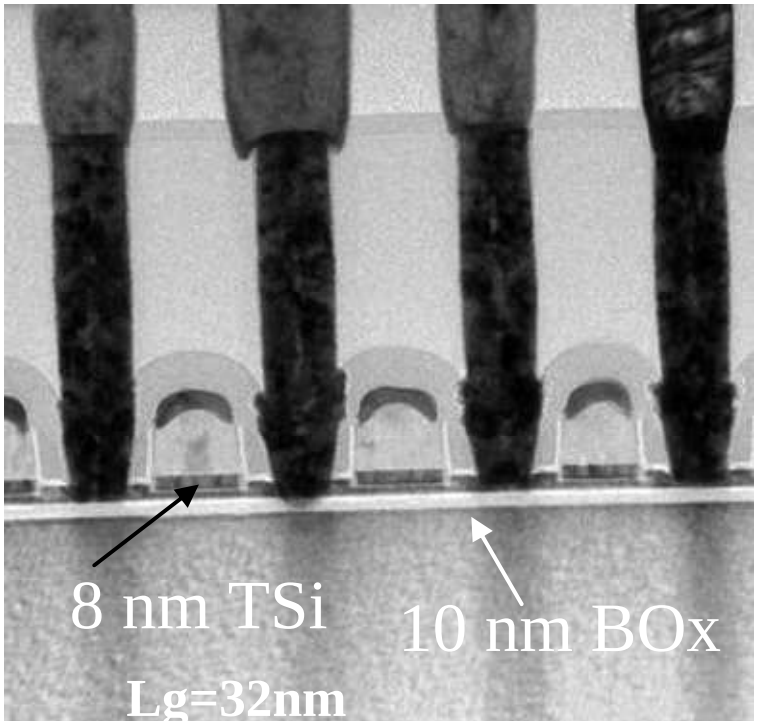
Low Power FDSOI Thin Films Undoped channels

300mm wafers

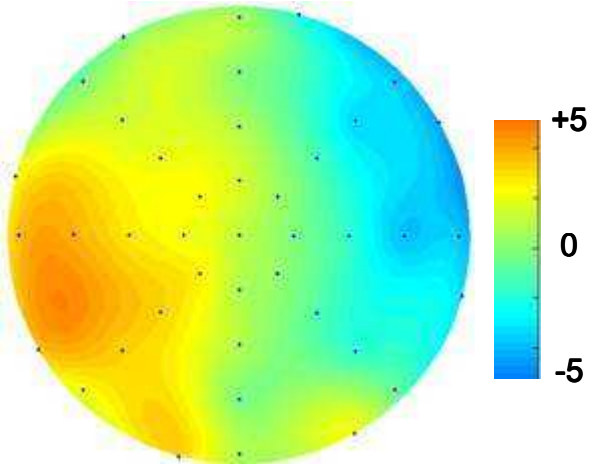
6T SRAM



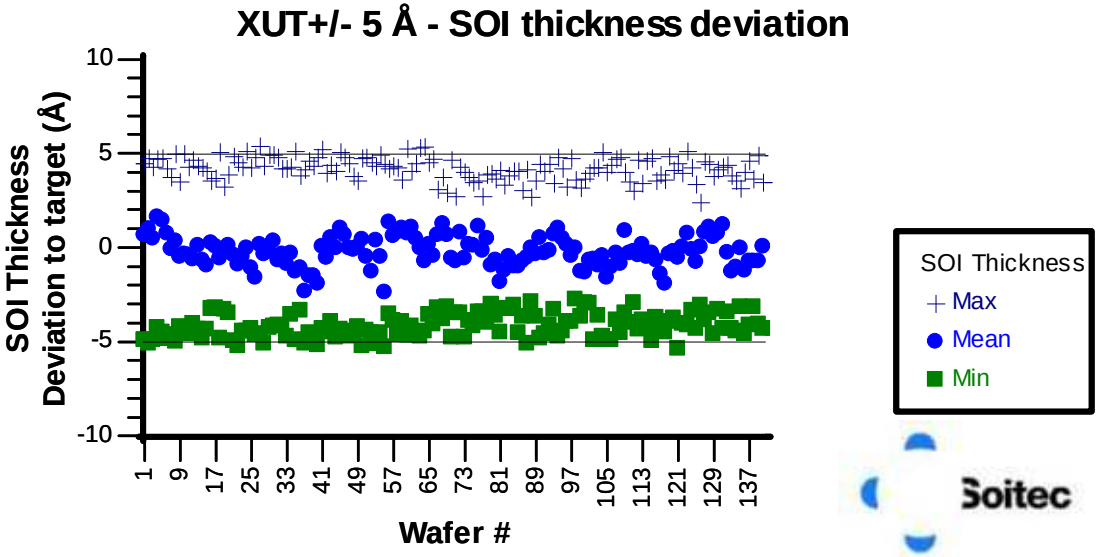
0.248µm² SNM (1.2V)=140mV

0.179µm² SNM (1.2V)=230mV

VDD=1V Ioff=6pA/µm



Range = ±4 Å!



LETI, ST Micro: C.Fenouillet Beranger et al., IEDM 2007, VLSI Symp 2010
V.Barral et al., IEDM2007

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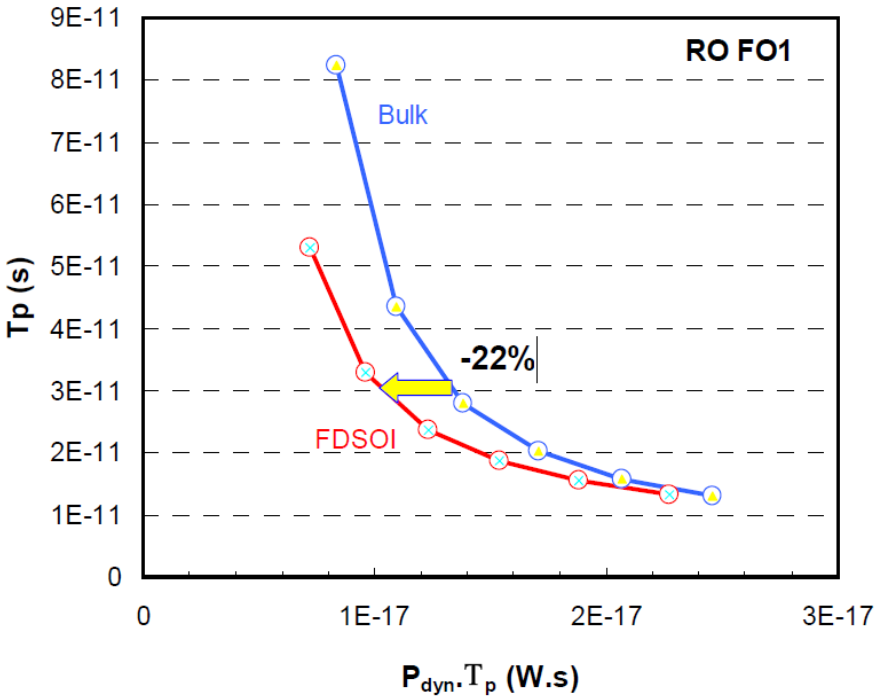
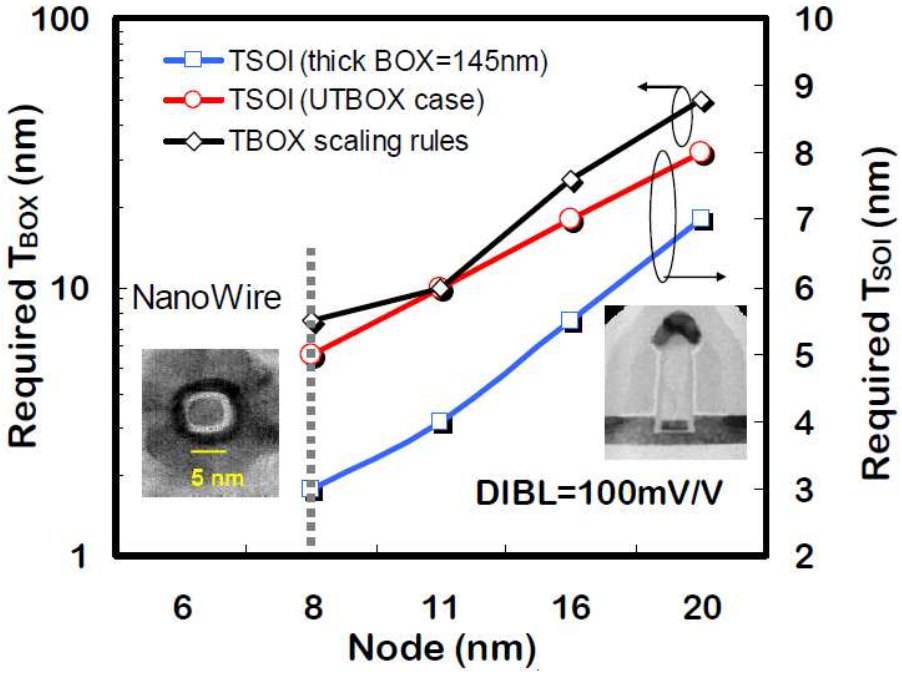
Merits of FDSOI

Delay vs. Power x Delay
22% improvement/bulk (20nm)



Reachable Scaling rules
(TSi, TBOx)



O.Faynot et al, IEDM 2010, invited talk

L.Clavelier et al, IEDM 2010, invited talk

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Expected impact

Society and life

- as personal companions, GA's will preserve human health and improve the quality of life for all categories of ages, in an affordable way
- GA's will make our environment more interconnected and smart, more energy efficient and safe
- Disruptive technology focused on prevention based on augmented information for personal level decision

Leadership in science and technology

- leading role of Europe in zero-power novel technologies
- enabling a stronger role of manufacturing in Europe
- improving the competitiveness for leading communication and medical companies

Employment

- creation of new employment in Europe in ICT domain
- new business opportunities

Guardian Angels
for a smarter life

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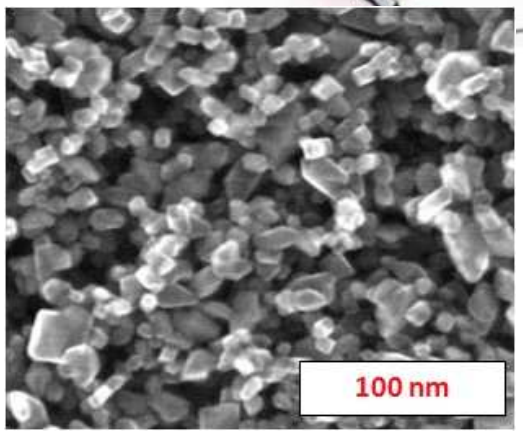
Towards a zero-power technology platform

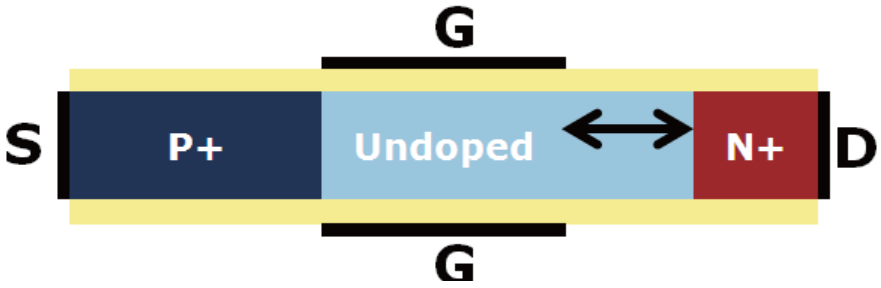
Bio-inspired energy scavenging: **artificial photosynthesis**



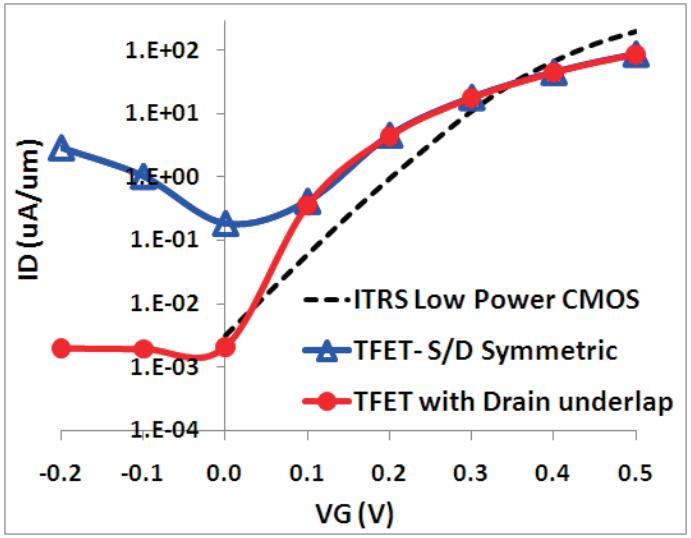
- Environmentally friendly materials
- High efficiency in-door & out-door

Guardian Angels
for a smarter life

TFET for Ultra Low Power outperforms CMOS
Offset/drain reduces Ioff(ambipolar current)

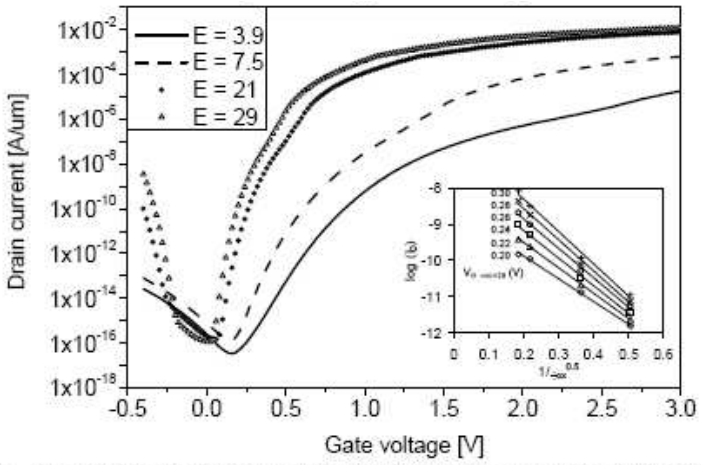


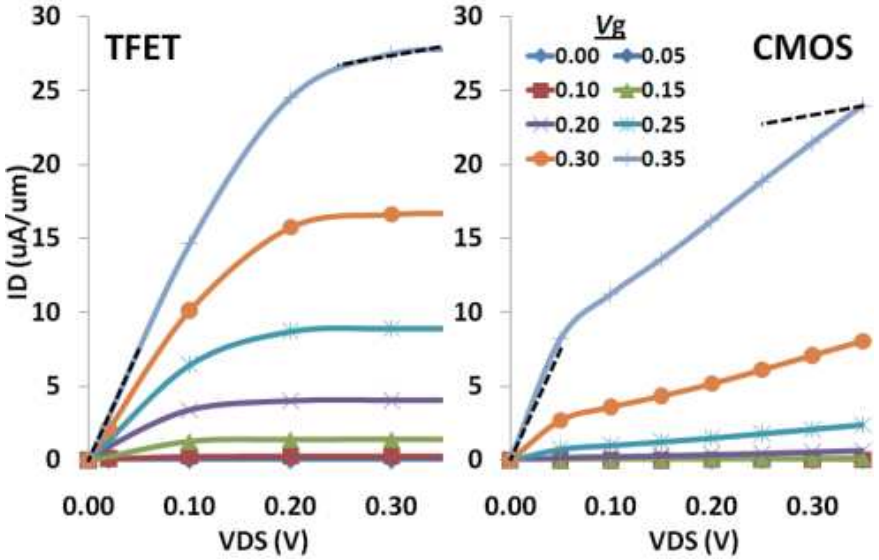
LETI: Mayer et al, IEDM 2008
Intel: U.E. Avci et al, VLSI Tech Symp 2011



Multigate improves Ion

EPFL: K. Boucart & A. M. Ionescu, ESSDERC 2006
TUM: M. Schlosser et al. IEEE TED, Jan. 2009





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