Nanoelectronics • Architectures
MIND
MIDWEST INSTITUTE FOR NANOELECTRONICS DISCOVERY

Nanoelectronics Research Initiative (NRI) Architecture & Device Benchmarking Workshop

Tuesday, August 14, 2012 • University of Notre Dame, McKenna Hall

7:45a	Check-in and continental breakfast	
8:30	Welcome and logistics	Wolfgang Porod, ND
8:35	NRI perspective	Tom Theis, NRI Kerry Bernstein, IBM
8:55	Intel Methodology for Beyond CMOS Benchmarking	Dmitri Nikonov, Intel
9:55	Break	
STATE VARIABLE - RESISTANCE. *Chair: Wolfgang Porod*		
10:25	Tunnel FETs – MIND	Alan Seabaugh, ND and Suman Datta, Penn State
11:10	Graphene PN Junction – INDEX	Azad Naeemi, Georgia Tech.
STATE VARIABLE – BOSE-EINSTEIN CONDENSATE. *Chair: Wolfgang Porod*		
11:40	BiSFET – SWAN	Frank Register, UT Austin
12:10p	Group Photo & Lunch	Irish Courtyard, Morris Inn
STATE VARIABLE – MAGNETIZATION I. *Chair: Sharon Hu, Notre Dame*		
1:15	SpinFET and Spin Wave Logic – WIN	Alexander Khitun, UC Riverside
1:45	Spin Torque Oscillators – WIN	Ilya Krivorotov, UC Irvine
2:15	Spin Torque Majority Gate – WIN	Dmitri Nikonov, Intel
2:45	Break	
STATE VARIABLE – MAGNETIZATION II. *Chair: Joe Nahas, Notre Dame*		
3:15	Spin Torque Domain Wall – INDEX	Jean Anne Currivan, Harvard / MIT
3:45	All Spin Logic – INDEX	Supriyo Datta and Joerg Appenzeller, Purdue
4:15	Nanomagnet Logic – MIND / WIN	Michael Niemier, ND
4:45	Future Directions Discussion	Kerry Bernstein/All
5:05	Adjourn	
5:45	Reception	Notre Dame Stadium Press Box
6:30	Dinner	Notre Dame Stadium Press Box
7:15	Remarks	Tom Theis