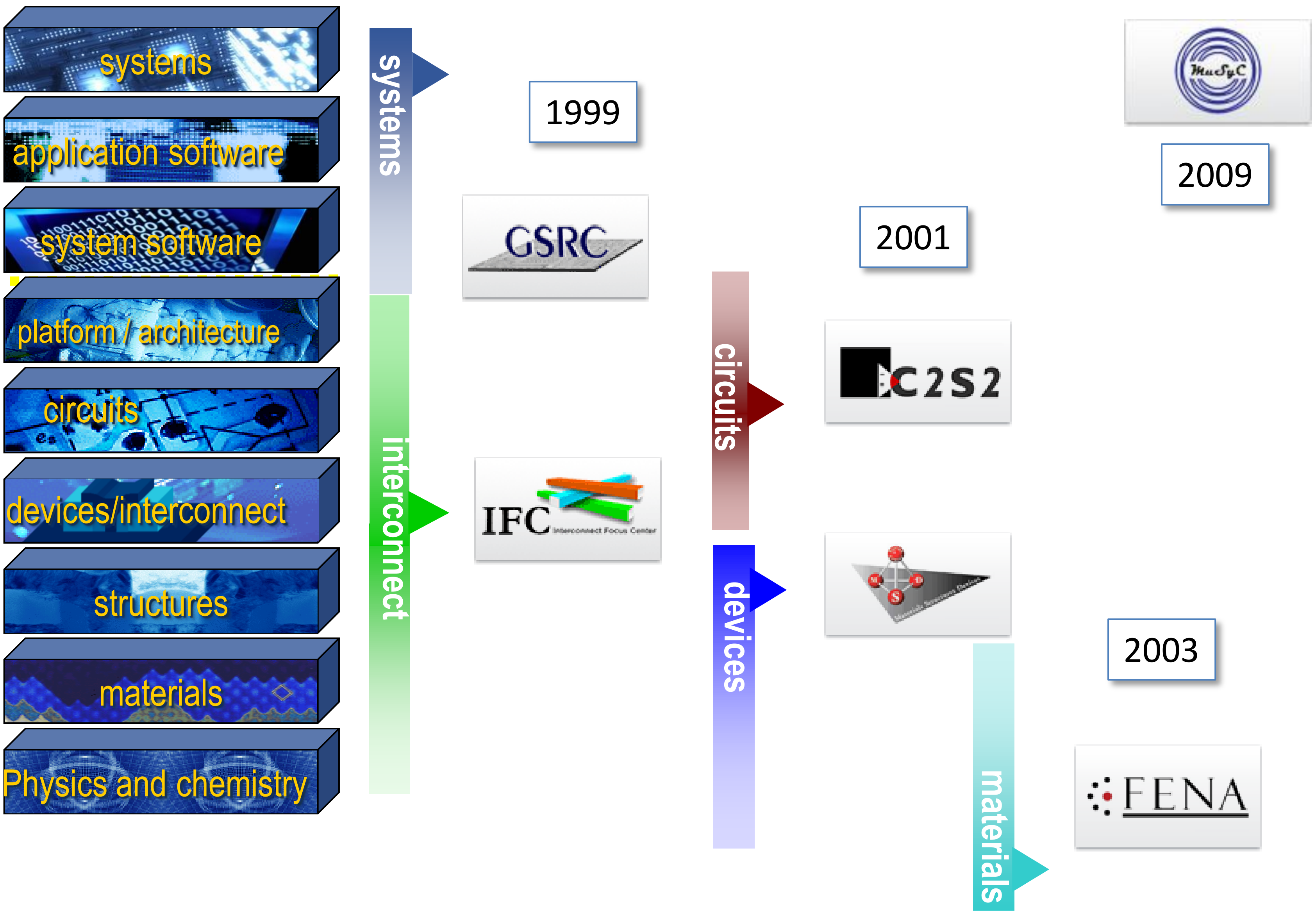
PAST

Mission: Carrying CMOS to its ultimate limits and beyond, keeping the United States and its industries at the forefront of technology, *i.e.*, "scaling"

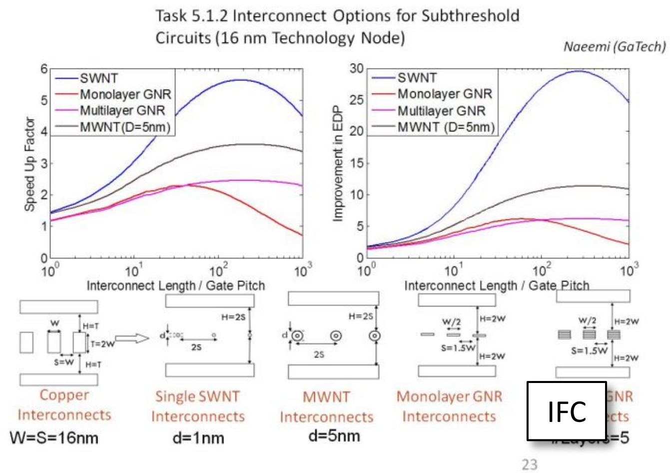
Source: SRC website, Feb 2011

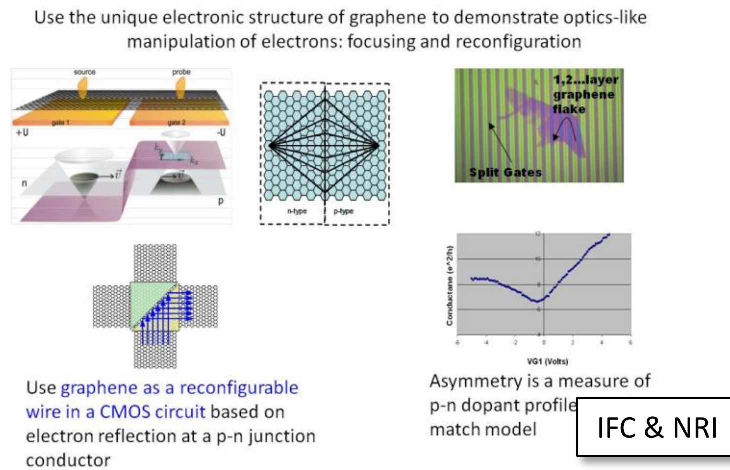
FCRP Center Evolution

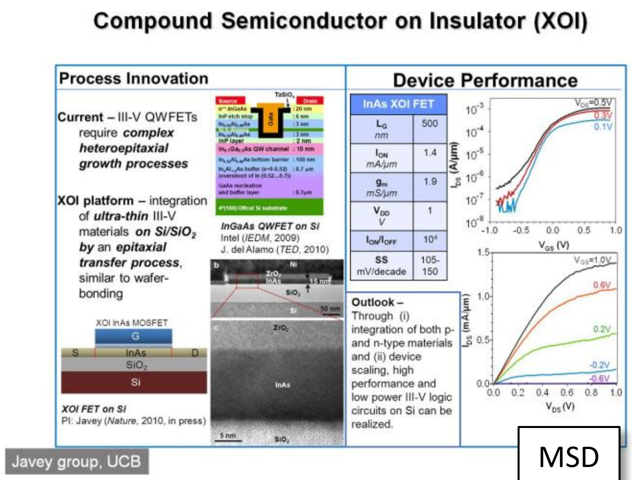


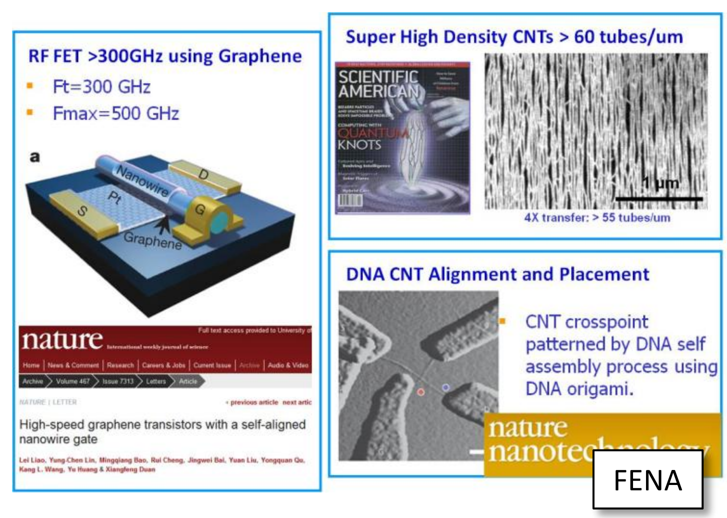
PRESENT

Example Projects



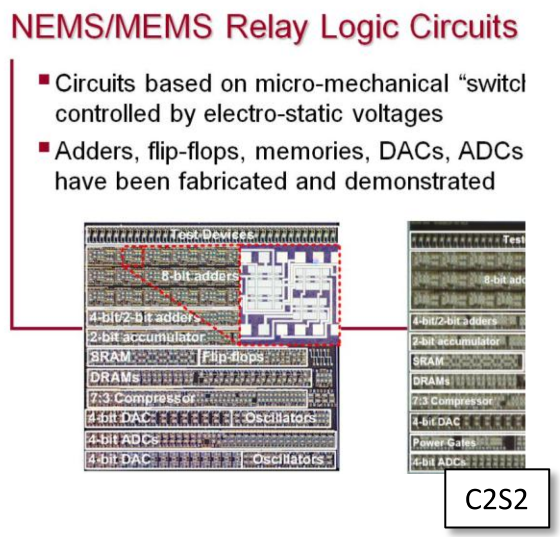


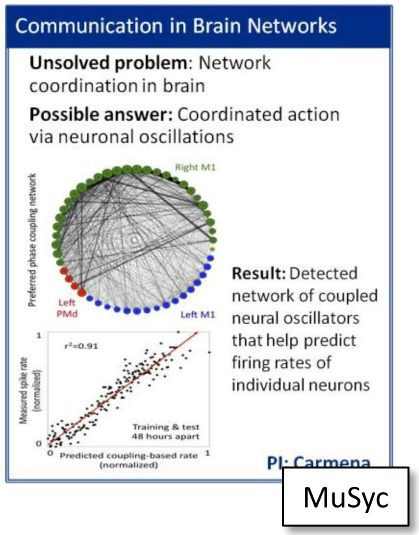


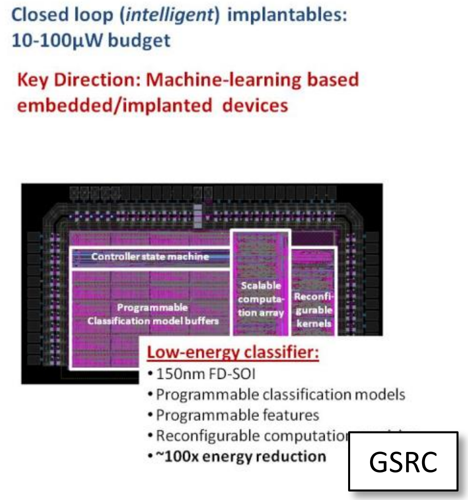


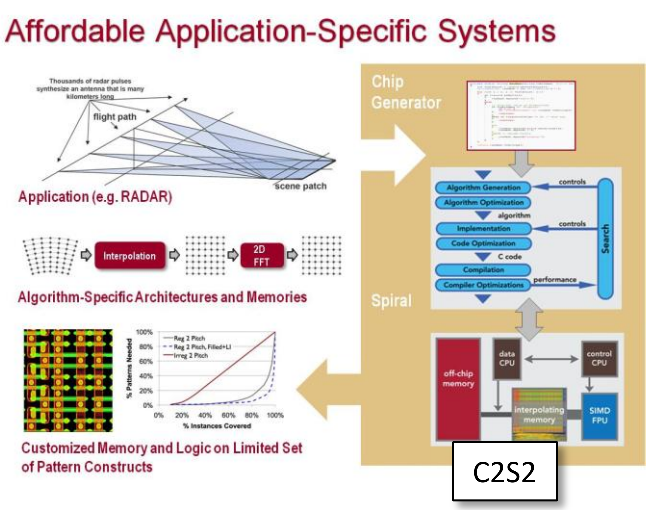
Source: FCRP Highlights, Nov 2010

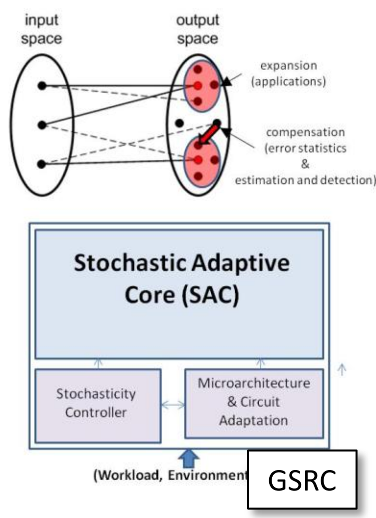
Example Projects

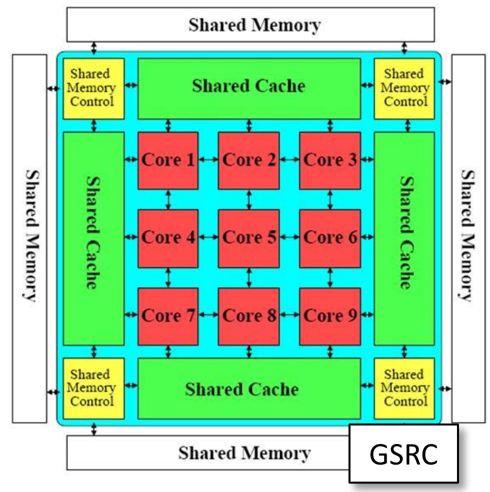








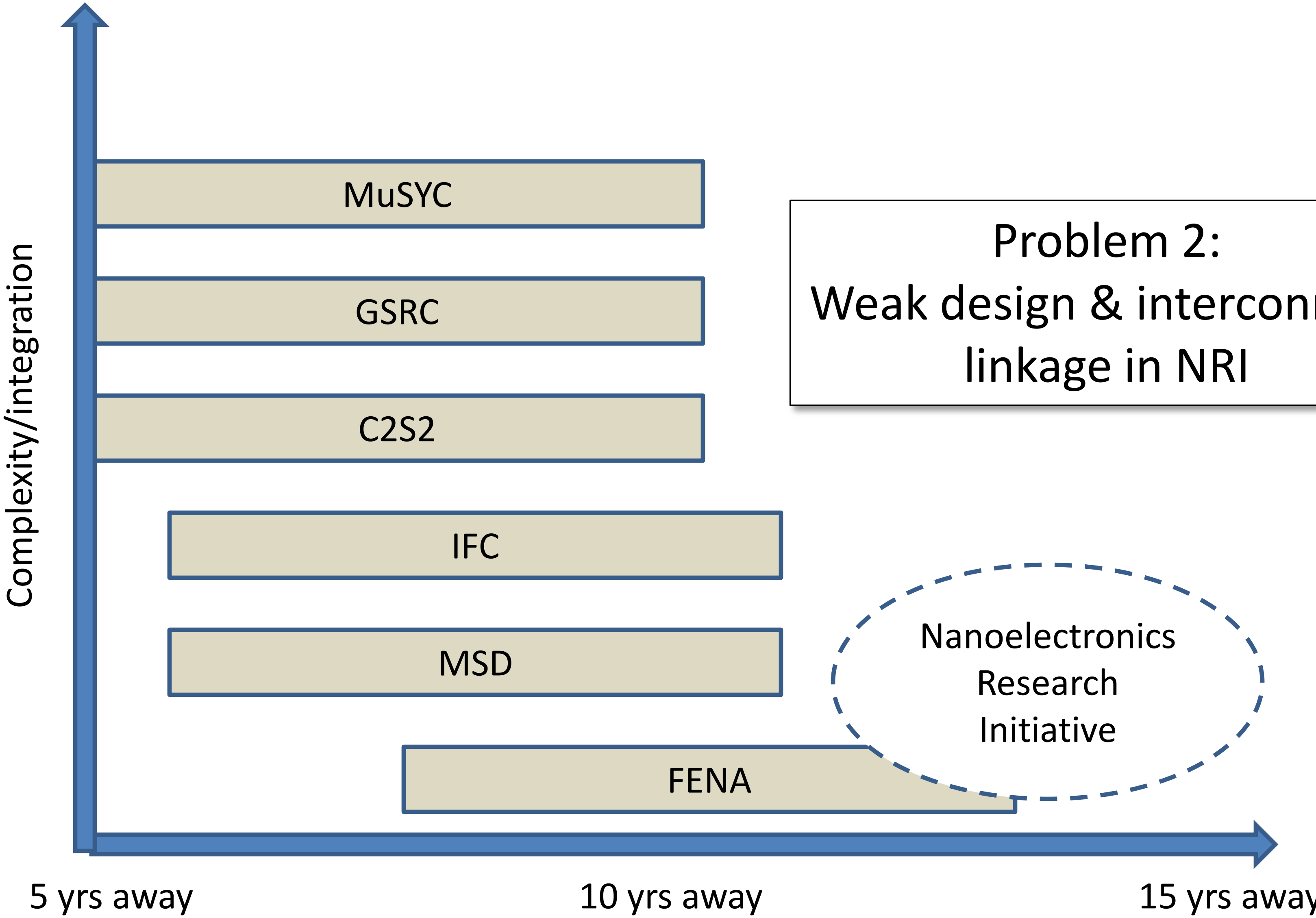




Source: FCRP Highlights, Nov 2010

WE GAVE YOU WANT YOU ASKED FOR, WHAT'S THE ISSUE?

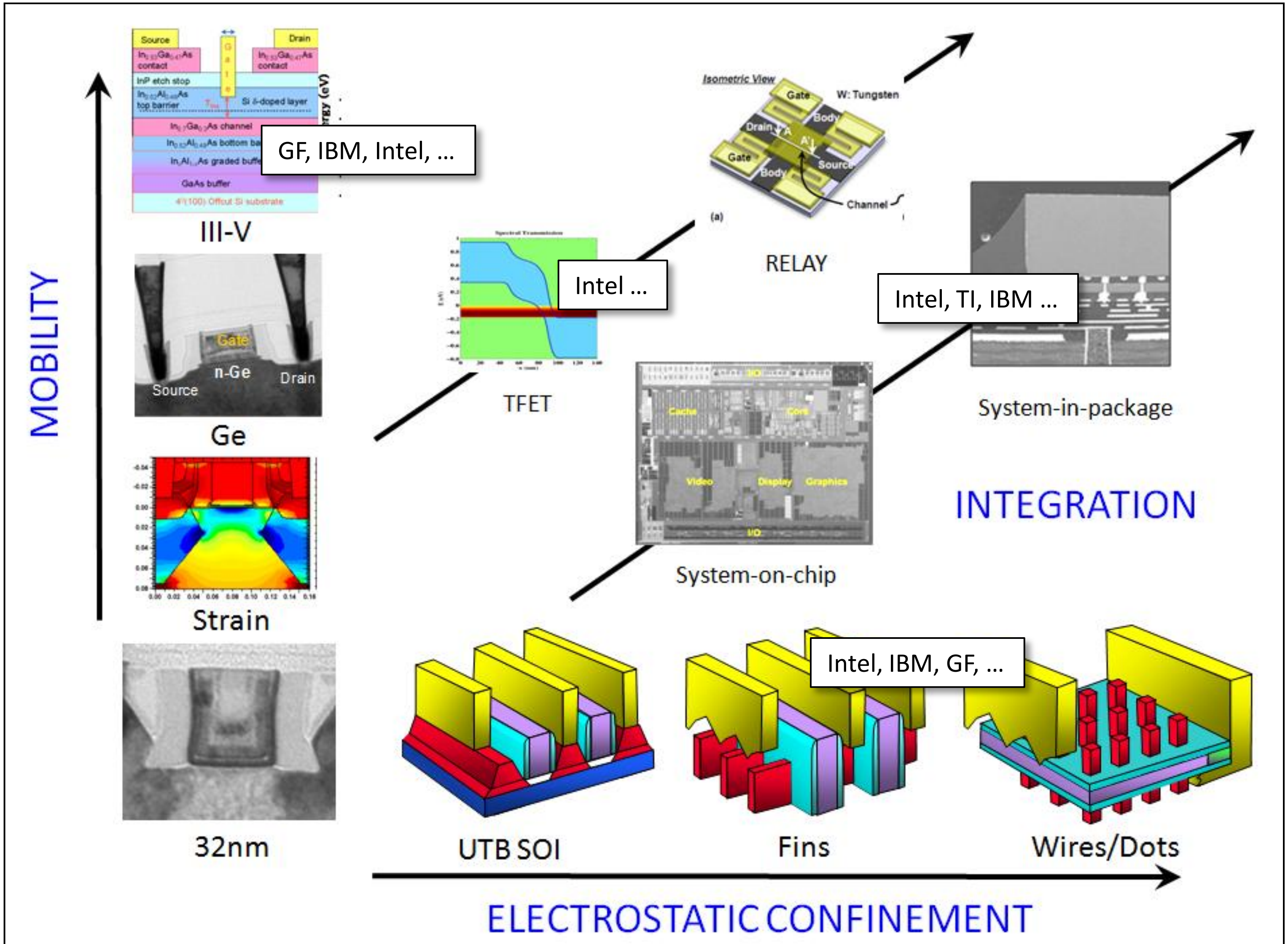
YOU WILL MISS OPPORTUNITIES IF YOU ONLY LOOK FOR BETTER VERSIONS OF TODAY'S TECHNOLOGY AND PRODUCTS



Problem 2:
Weak design & interconnect linkage in NRI

Problem 1:
Industry research catching up to current FCRP research

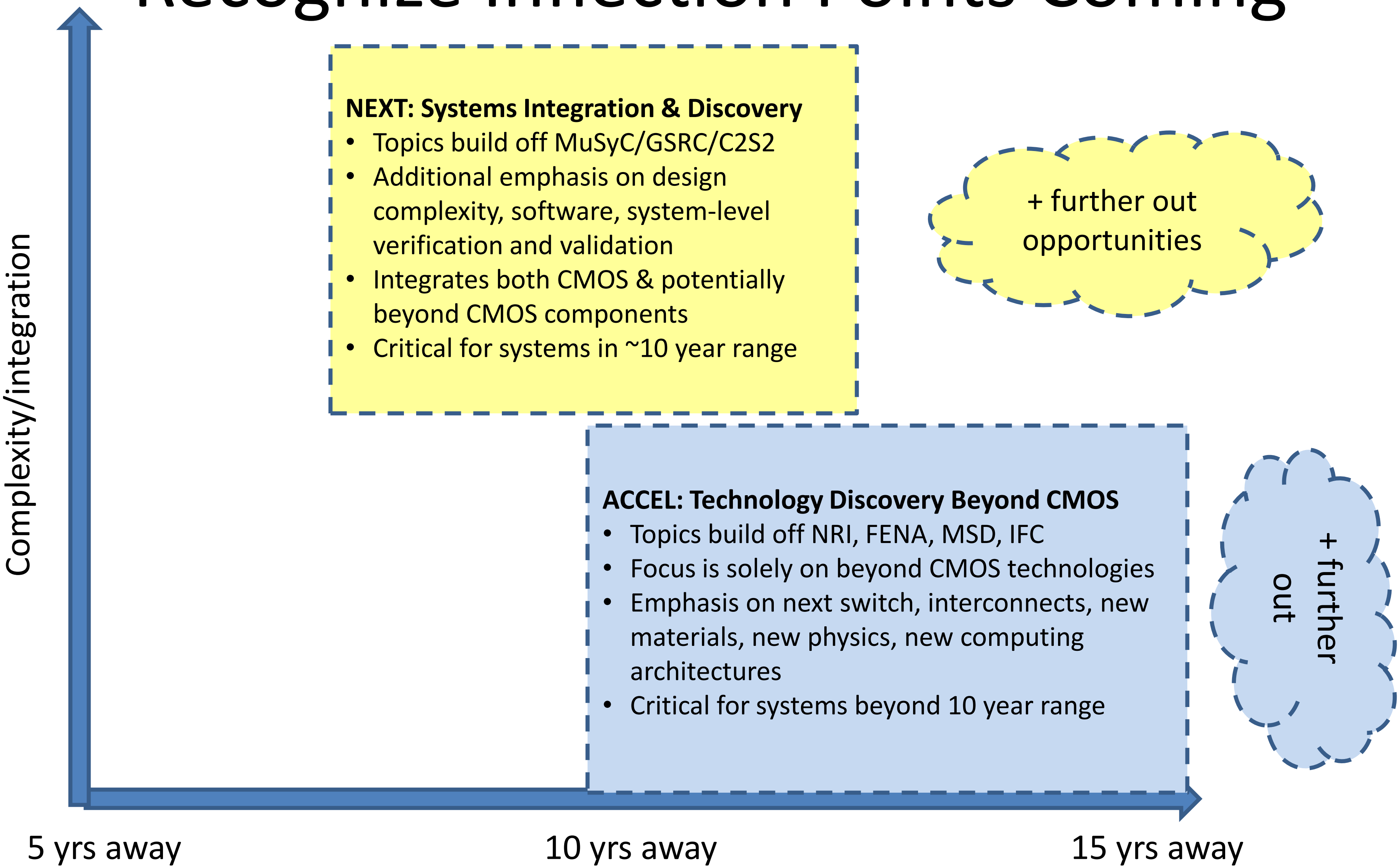
Example:
FCRP research becoming industry research



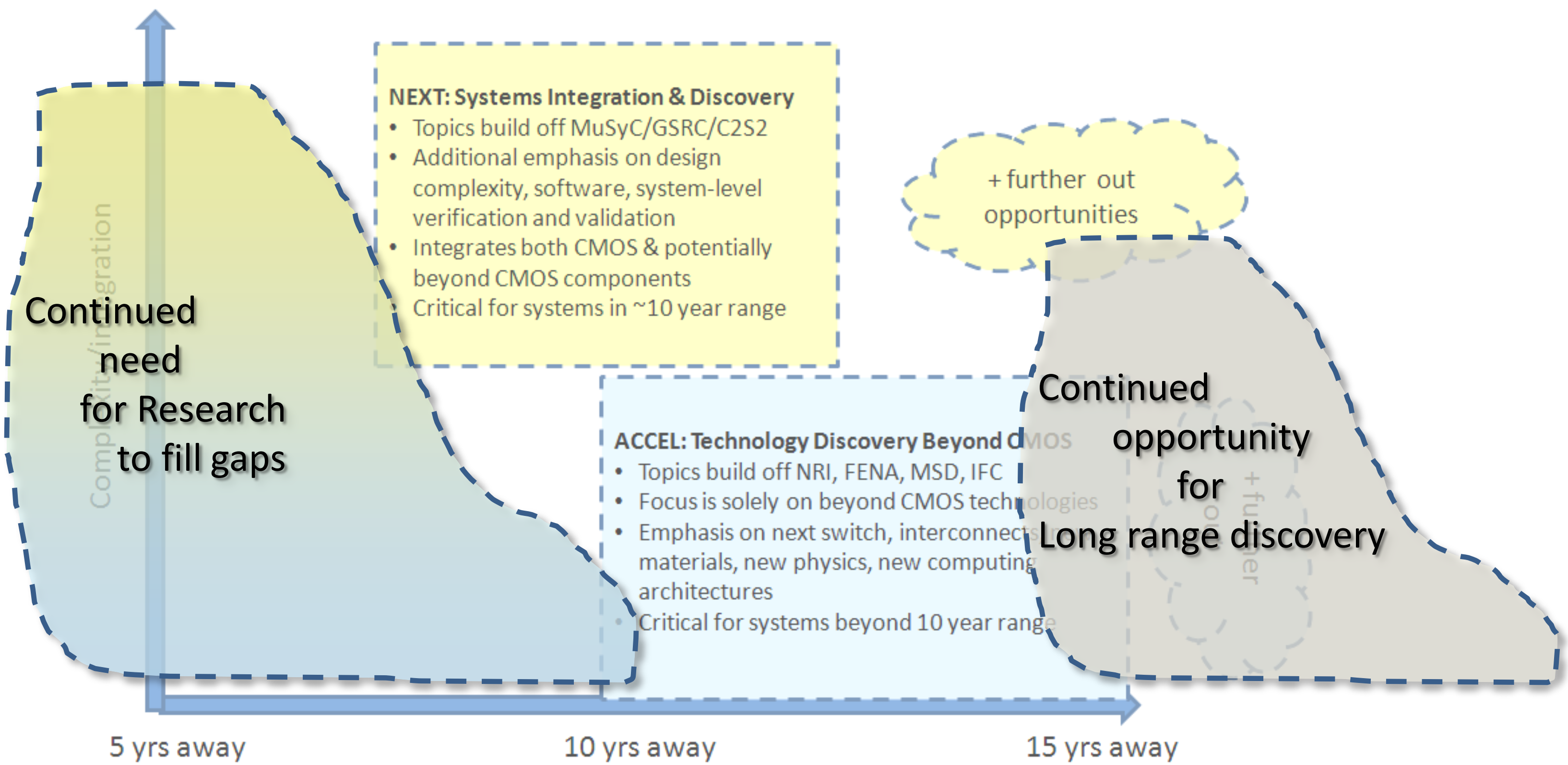
Source: Intel, Jan 2012

FUTURE

Push Further Out
Recognize Inflection Points Coming



Planned Research Landscape



Ongoing selections	2012 selections	2012 selections
GRC-Industry	FCRP-Industry-DARPA	NRI-Industry-NIST-NSF

NEXT – Highly Complex Systems

Mission: Enable highly complex systems with capabilities well beyond those available today, i.e., to augment beyond the "sum of the parts."

Focus on system – building blocks, methods, capabilities

- Zone 1: Complex heterogeneous networked systems
- Zone 2: Highly parallel centralized computation systems

Technology Areas for NEXT –

- High performance analog for high speed wireless; THz electronics for imaging, sensing, novel power devices
- Vehicle and Distributed Sensor Networks
- Computing System Architectures based on CMOS technology
- Tools and methods for design, verification, and predictive modeling, including physical modeling of thermal and structural impacts on functionality and the physics of failure of proposed components.

Opportunity to fund some emerging areas
as special projects outside of main focus areas

ACCEL – Semiconductor Technologies Beyond CMOS

Mission: Identify and accelerate progress for new mainstream technologies beyond digital CMOS

- Focus areas structured with both focus on most promising concepts and continued seeding future technology ideas
- Necessary to look beyond simple replacements of existing digital CMOS elements, building blocks alone are not sufficient
- Anticipate and work at or beyond inflection points

Technology areas for ACCEL –

- Nonconventional material systems
- Quantum engineered devices and new sensors and transducers
- Integrated circuits and computing architectures

Opportunity to fund some emerging areas
as special projects outside of main focus areas

Example Inflection Points

End of Scaling is Near – Decades of predictions

"Optical lithography can't do sub-micron"

"Optical lithography will reach its limits in the range of 0.75-0.50 microns"

"Optical lithography should reach its limits in the 1990-1994 period"

"X-ray lithography will be needed below 1 micron"

"Minimum geometries will saturate in the range of 0.3 to 0.5 m

"Channel lengths can be reduced to approximately 0.2 micr

"Minimum gate oxide thickness is limited to ~2 nm"

"Oxide reliability may limit oxide scaling to 2.2 nm"

"Plasma etched aluminum will not happen in our lifetime

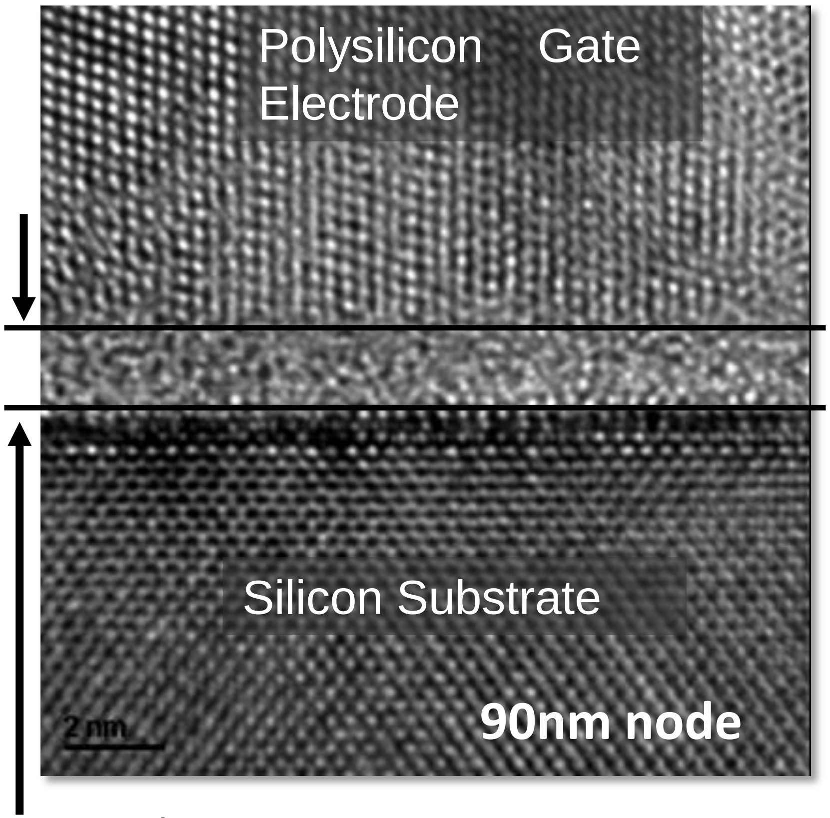
"Copper interconnects will never work"

"Scaling will end in ~10 years"

Inflection Points

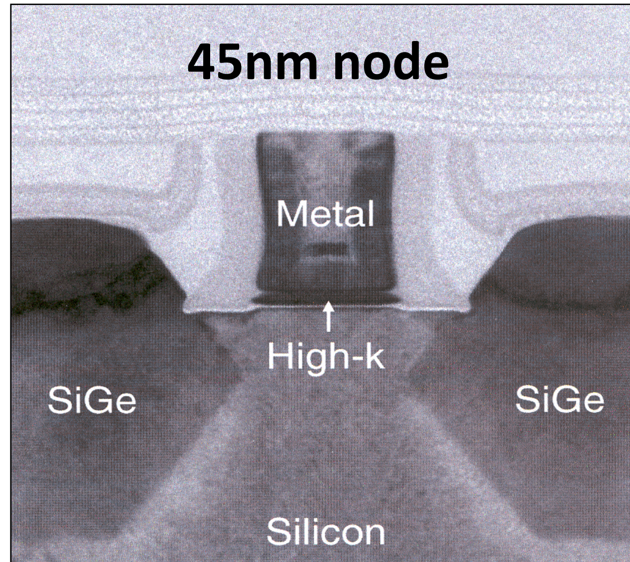
- Size Limited by Granularity, Process Control
- Size limited by Electrical behavior (tunneling)
- Voltage scaling limited by Mobility
- Interconnects limit Performance
- …

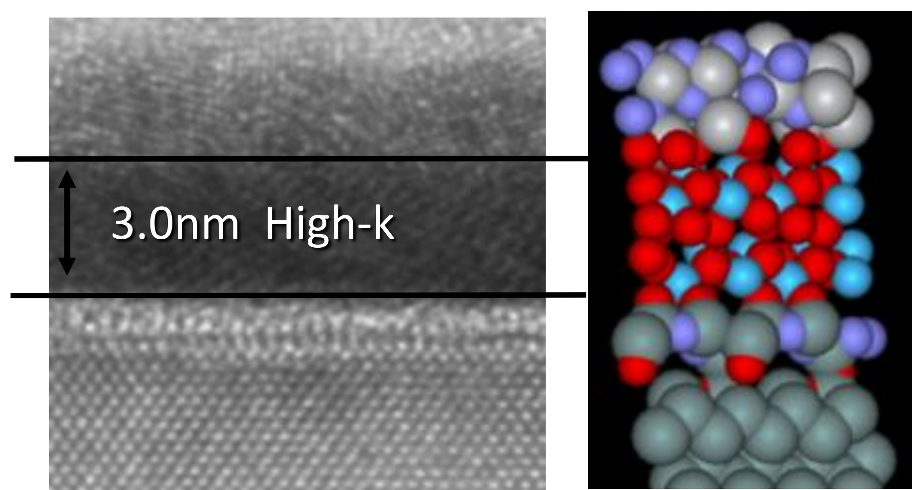
Inflection Point: Granularity Limits Size
Switch to Chemistry Driven Processes



1.2 nm SiO_2

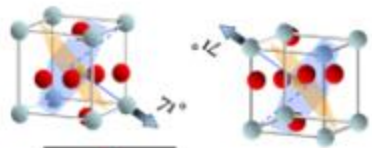
3-4 atoms thick



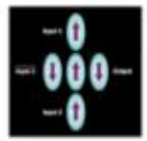


Inflection Point: Size limited by Electrical behavior
Switch to Different Device Operation
Nanoelectronic Research Initiative – Search for Next Switch

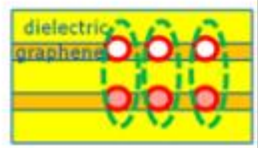
1. **Charge, current, voltage (Q,I,V)**
2. **Electric dipole (P)**

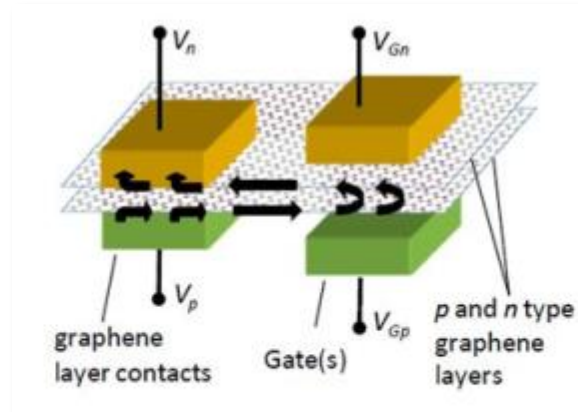


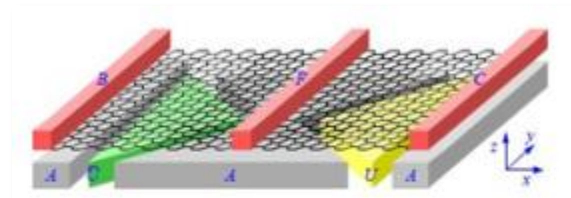
3. **Magnetic dipole = spin (M)**

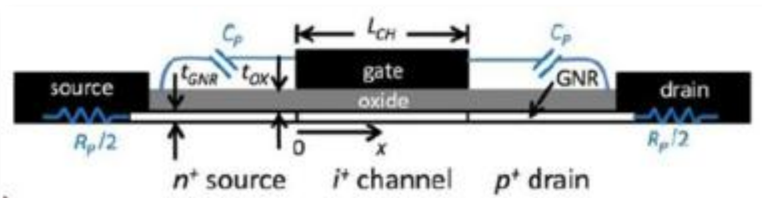


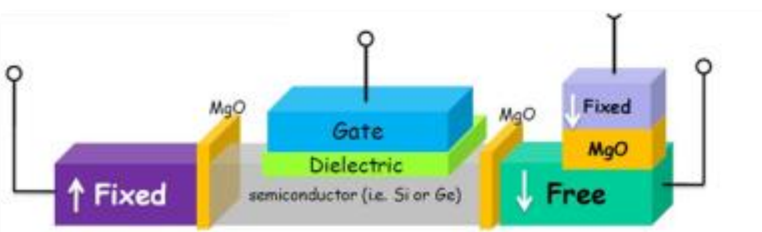
4. **Orbital state (Orb) in e.g. quantum well, molecule, crystal, also excitons, esp. Bose condensate (Cond)**

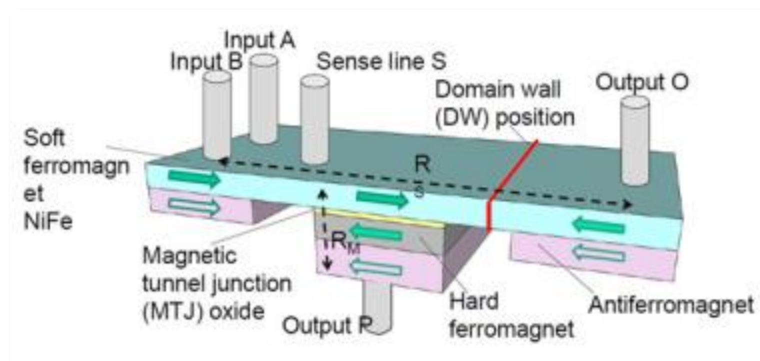




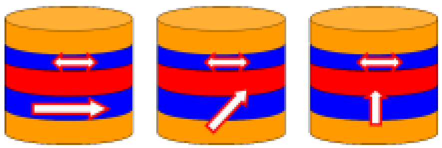


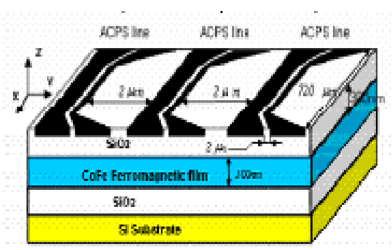


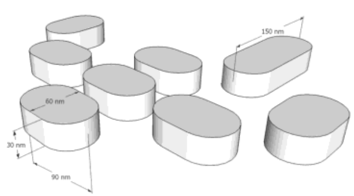




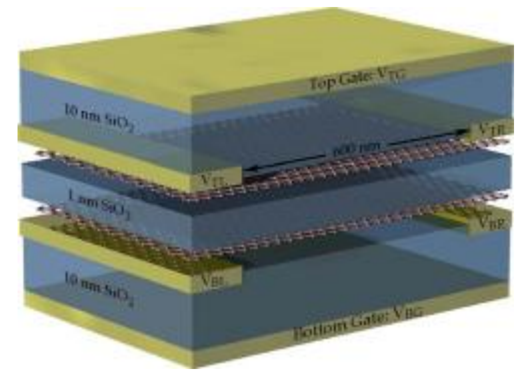
NRI: 18 New Devices Benchmarked as a Next Switch
Most can be built with multiple active layers

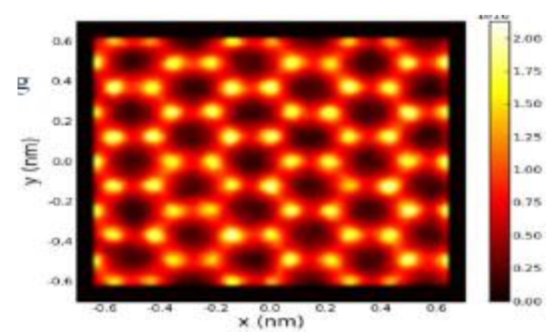






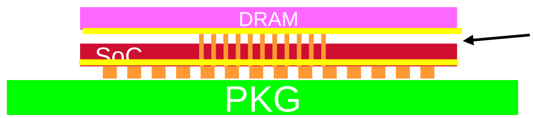
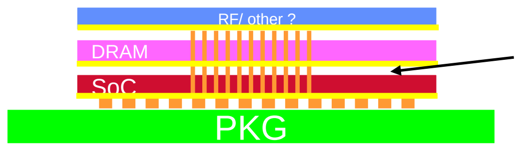
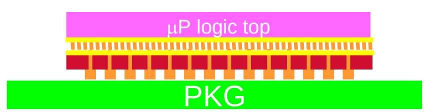
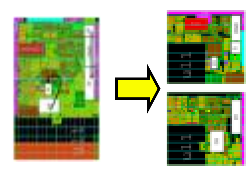
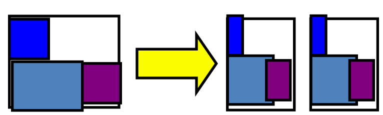
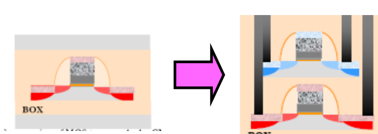
Code	Device
	Units
REF-H	15 nm CMOS
REF-L	15 nm CMOS
I-01	Excitonic FET
I-04	MTJ Logic Switch
I-05	All Spin Logic
I-07	Graphene PN Junction
I-08	Electronic Ratchet
M-01	Graphene thermal logic
M-02	BDD Architecture
M-04	Nanomagnet logic
M-05	gnrTFET
M-06	InAs TFET
N-02	e-Struct. Modulation Trans
N-03	RAMA
S-01	BiSFET
S-02	RIEFET
S-03	HetTFET
W-02	Spin Wave
W-04	MTJ/STT
W-05	Spin Torque Amplifiers





Conventional →

Rethinking 3D

Possible Application	Bonding/ Fabrication Method	Connections	Stacking Objective
Memory + Logic	 Face to back/DtD	**~1000s**	**Reduce wiring/ form factor**
Multiple die stacking	 Face to back/DtD	**~1000s**	**Reduce wiring/ form factor**
Smart unit repartitioning (logic+logic)	Face to face/ WtW or DtD  	**~1M+**	**Reduce wiring (upper layer)**
Within unit repartitioning (logic+logic)	 Face to face/ WtW or DtD	**1µm/0.5µm ~10M-100M**	**Reduce wiring/ density?**
Circuit /device repartitioning	Sequential processing  NOT TSV	**5-10nm ~10B+**	**Density/ Disparate Integration**

Novel →

FCRP workshop – M Mayberry, May 2012

Rethinking Computation

Conventional →

Novel →

Compact Full Adder: Non-Boolean Logic

- **Option1:** conventional ASL (44 magnets)
- **Option2:** functionality enhanced ASL (5 magnets)

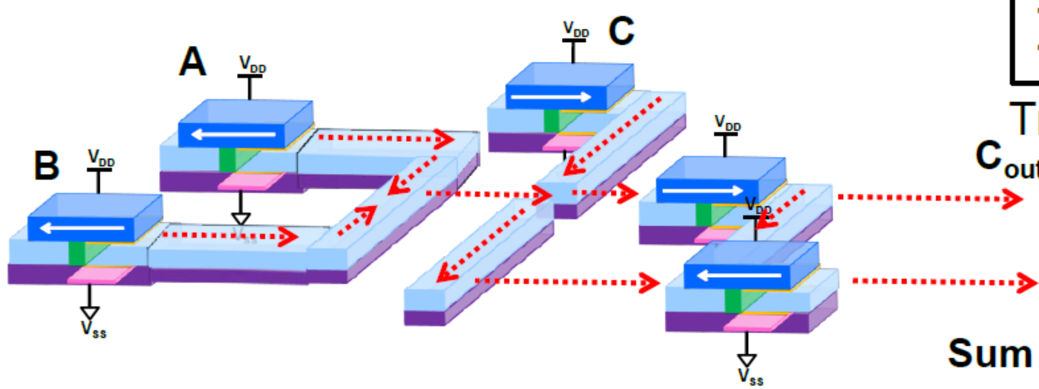
Inputs: A, B and C
Outputs: Sum and Cout

$$Sum = A \oplus B \oplus C$$

C_{out}=AB+AC+BC=M (A,B,C)

A	B	C	C'_{out}		Sum
0	0	0	1	1	0
0	0	1	1	1	1
0	1	0	1	1	1
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	0	0	0
1	1	0	0	0	0
1	1	1	0	0	1

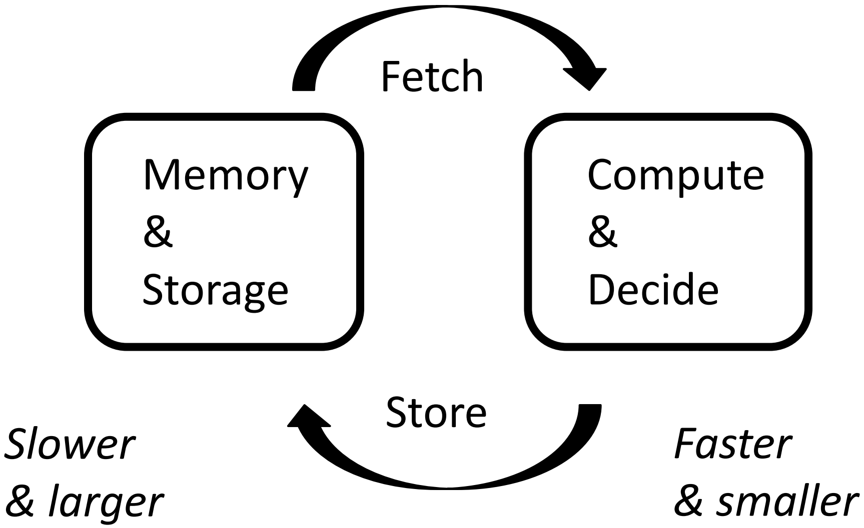
Truth Table for SUM



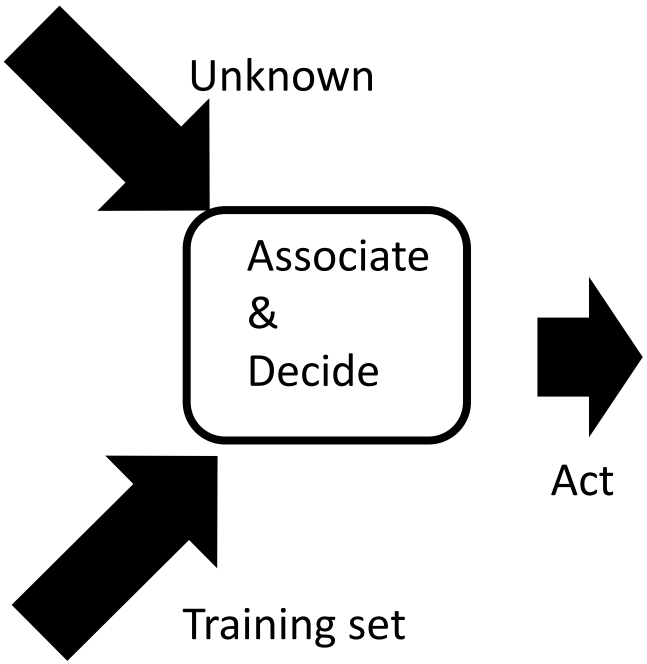
Functionality Enhanced ASL (FEASL)

C. Augustine et al., NanoArch, 2011

Exploring Other Ways to Compute



"Von Neumann"



Bottleneck = memory/storage
Transport limited devices make it worse

Bottleneck = training
Potentially favorable for novel devices

Conventional

Novel

Interconnects are Pervasive

- New materials needed for novel interconnects
- Not sufficient to only explore device behavior
- Transducers to convert between domains
- Novel transport in highly interconnected 3D
- Working around transport limited computation
- …

Key Messages

- All Paths forward require Materials Research
- We need to rethink our approaches to both device & design technologies
  - Systems can have unique abilities not planned at building block level. Use cross-functional approaches
  - Interconnects and transport work differently for novel devices, how can we exploit that ?
  - Optimal computation might be very different, where are the opportunities ?
- We want to identify & fund **novel** long term research, not just gaps that we can see
- Surprise us !