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nanoelectronics RESEARCH INITIATIVE

NRI Proposer's Meeting

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Agenda

- Overview of the call for new center proposals

  http://www.src.org/compete/s201215/

- Solicitation and selection schedule
- Answers to some questions you've asked
- Open Q&A

NRI's Evolving Mission

- Phase 1.0/1.5 discovered many promising new devices, but no "next switch"
  - Many devices have some desirable properties and operate at low power, but lack one or more key attributes necessary to compete directly with the FET.
- Guidance from the NRI Governing Council on topics / direction
  - Maintain focus on a specific technology goal – but don't restrict to logic
  - Emphasize "non-conventional" options – could include logic, mem, interconnect, analog
  - Emphasize focus on "low energy / power" as the guiding mission statement
- White Paper on NRI Next Phase Mission: Demonstrate non-conventional, low-energy technologies which can outperform CMOS on critical applications in ten years and beyond.
  - These technologies should include both novel device and architecture approaches to achieve low-energy, high-functionality solutions, and can include logic, memory, sensor and analog components, with a particular emphasis on non-conventional devices whose properties span these categories.
  - To ensure the results are relevant and sufficient for proving out the new approach, simulation and experimental demonstration of all parts of the technology are included, from developing new materials and demonstrating new phenomena to fabricating, patterning, and characterizing devices and basic circuits.
  - Pursuing 5 primary research vectors (modified slightly from Phase 1/1.5)

NRI Research Vectors

- Device with alternative state vectors
  - Spin, photonic state, collective effects, etc.
  - Voltage-based devices are welcome, but must operate by novel principles
- Non-equilibrium systems
  - Phonon engineering, devices exploiting phenomena with timescales shorter than the thermal equilibration time, or devices conducive to use in energy-recovering or energy-conserving circuits
- Novel interconnect native to the information token
  - Novel transduction devices, contacts to the active device, novel circuit topologies
- High computational density devices (NEW)
  - High fan in/out, logic efficiency, combined memory/logic, etc.
- Architecture for non-conventional devices (NEW)
  - Non-Boolean, analog, bio-inspired, patterning/manufacturing friendly, etc.

NRI's Research Goals

Key Points from the RFP

- Overarching Goal: Promote research on topics which have potential for maintaining the historical trends in increasing computational power and decreasing cost of information processing.
  - Devices and circuits that compete favorably with tomorrow's high-performance CMOS technology for general purpose computation.
  - Devices and circuit architectures that perform well for specific and important applications or algorithms or at ultra-low power.
  - Devices with novel function beyond that of a simple digital switch, and circuits and application areas that exploit this behavior for maximum benefit.
- Ideally, the device and associated circuit architecture should outperform CMOS at the end of the CMOS scaling roadmap, and be extendable *beyond* the end of the CMOS roadmap.
  - Note: Scaling means more than simply doubling the number of devices on a chip each technology generation. The focus should be on compounding increases in computational performance without being limited by physical and economic constraints on power dissipation.

What is unique about NRI?

Additional Key Points from the RFP

- The GRC, FCRP and NRI programs are being extended to explore and develop the technological possibilities of a post-CMOS world. NRI will continue to be positioned as the most forward-looking of these programs.
- NRI research will expand beyond its present focus on the logic device to include the circuit and architecture level. Each new center should:
  - Establish interdisciplinary teams to effectively address the key research problems engendered by each device and related circuit architecture, from materials growth to fabrication and characterization, and from basic physics and simulation to device design and circuit implementation.
  - Focus on 2-3 device technologies, with multi-PI and multi-university teams to cover all key areas of research to implement computation with that device.
  - Include a strong characterization and nano-metrology component, to link between experiment and simulation.

Schedule for NRI New Center Solicitation

- April NRI responded to NIST FFO
- Aug. 3 RFP for new/extended centers released to universities
- Sept. 19 NIST Award approved.
- Oct. 16 Proposer's Meeting (WebEx)
- Nov. 13 Deadline for submission of NRI center proposals
  (FCRP proposers notified of outcome Oct 13; final selections Oct. 30)
- Dec. 21 Final selections
- Jan. 14 Next phase NRI center awards announced
- 1Q13 Start next phase centers (as close to 01/14/13 as possible)
  (No Cost Extensions to March 31 have been granted to existing centers.)

Questions and Answers

The following questions were received and answers were prepared prior to this Proposer's Meeting.

Q&A

- Q: Is NRI interested in truly new device concepts?
- A: Of course, but please provide physical arguments (the more rigorous, the better) for why the new concept, if developed, could provide important advantages over the field effect transistor when used for computation. Don't forget to consider circuit architecture(s) which best exploit the characteristics of the new device.

Q&A (continued)

- Q: The call for proposals emphasizes the application of non-conventional technologies to digital applications. We believe that the technology we are interested in could also be applied to DACs and ADCs. Is this an acceptable area of research?
- A: Yes. The proposal calls for devices with higher computational density. Examples include but are not limited to devices which combine memory, logic, *analog* or other functions, devices which are conducive to high fan-out and/or high fan-in circuits, reconfigurable circuits, or any other approach to greater logic efficiency.

Q&A (continued)

- Q: Will NRI fund research on devices based on graphene or carbon nanotubes?
- A: Yes. As long as the materials are used to realize a device concept with the potential to take computing beyond the voltage-scaling and other constraints of the conventional FET. Conversely, NRI will not fund research on conventional field-effect transistors, regardless of the choice of channel material.

- Q: Is NRI only interested in devices for digital logic?
- A: In Phase 2 of NRI, the focus remains on technologies for computation, but we've broadened the research goals to encompass device and architectural approaches to achieve low-energy dissipation and high-functionality. An architectural solution might include logic, memory, and analog functions, perhaps combined in a single device.

Q&A (continued)

- Q: Is NRI interested in funding research on quantum devices?
- A: It depends on what you mean by quantum devices.
  - We solicit proposals for new devices implemented in novel circuit architectures. That could mean a device in which digital state is represented by a single quantum state or a small ensemble of quantum states. Note, however, that the device and associated architecture should not require bulky refrigeration. We want to enable ubiquitous "room temperature computing".
  - NRI will not fund research in devices and architectures for quantum computing. Government funding of such research is large and growing, and despite rapid progress in the field, widespread application of quantum computing still appears to be decades away.

- Q: Is NRI interested in biological computing?
- A: Not unless the proposed device and associated architecture can compete with the transistor in power and performance for some important computing applications. NRI *is* interested in *biologically-inspired* devices and architectures such as neuromorphic systems.

Q&A (continued)

- Q: How broadly are the architectures in Research Vector 5 defined (beyond computation)? What about manipulating multi-modality information, e.g. electrical, chemical, acoustic, optical and thermal information, in an integrated monolithic device/system?
  - Research Vector 5: Architectures to exploit non-conventional device behavior for manipulating information.
    Examples include but are not limited to non-Boolean, analog-like, and neuromorphic or other biologically-inspired architectures, and architectures which trade digital precision for reduced power consumption or which are conducive to cost-effective nanoscale regular/modular patterning and fabrication.

- A: We are interested in manipulating multi-modality information, but in your proposal, please tell us as much as you can about the interesting computational tasks or applications that will benefit from this approach.

Q&A (continued)

- Q: In Research Vector 3, are interfaces limited to chip level? How about new interconnect technologies in novel systems, for example, that could provide large-scale bi-directional information transfer between electronic and biological systems?
  - Research Vector 3: Novel interconnect approaches native to the information token *Examples include but are not limited to novel transduction devices (if the logic device is not externally voltage-based), advanced contacts to the active device, and novel circuit topologies.*

- A: The intent is that research on novel interconnections should be motivated by the characteristics of the proposed device and associated circuit architecture. If you propose research towards a specialized application (i.e. information transfer between electronic and biological systems), please tell us the advantages of your new device and its associated architecture in that application.

Q&A (continued)

- Q: Does SRC have any plans to facilitate teaming arrangements by providing, for example, a forum where PIs could indicate their relevant expertise, unique relevant capabilities, including publications, and interest areas within the NRI solicitation? This should help bring missing expertise or unique capabilities into existing teams or nucleate new competitive teams.
- A: No. We are not providing such a forum, but you may contact me and/or members of the NRI Technical Program Group and describe your interests and expertise. We'll do our best to recommend others with related interests that you might contact regarding teaming.

Q&A (continued)

- Q: How much detail is needed regarding subcontractor's budgets?
  Do we need to submit detailed subcontract budgets using the budget form (FinancePlan.xlsx)?
- A: You should enter the total cost of all subcontracts on line E of the budget form (FinancePlan.xlsx). Also enter the names of the subcontracted universities on the same line. On a separate sheet, list the subcontracted projects and associated PIs, and the associated budget for each subcontractor, year by year. You may, if you wish, include a further high-level breakdown of each subcontractor's yearly budget on that sheet: PI and student salaries, significant equipment purchases, significant travel expenses, etc. However you need not provide this more detailed budget information for subcontractors at this time. Furthermore, **there is no need to ask subcontractors to go through their own internal approval processes and return signed approvals at this point,** particularly since NRI may request budget modifications in the contract negotiation phase for those proposals that are selected.

Q&A (continued)

- Q: For the proposal, are the items listed in the Overview of Research sufficient as in prior years, or must we also fill out the Research Catalog pages for the different Themes/Tasks? Also, what is the difference between Theme and Task?
- A: You should describe Themes and Tasks. A Theme is a broad research topic such as “All Spin Logic” or “Tunneling FETs”. Each Theme is divided into related research Tasks. Each Task is typically led by a different PI, but all PI’s are expected to work together to develop the Theme. Here’s an example of a current program from the SRC website:
  - THEME: **III-V Tunnel and Graphene FETs**
  - TASKS:
    - 5.1 Modeling and Analysis of Tunnel Transistors with NEMO/OMEN. PI: G. Klimeck (gekco@purdue.edu) Purdue
    - 5.2 Heterojunction p-n Tunnel Field-Effect Transistors. PIs: P. Fay (fay.9@nd.edu), T. Kosel (Thomas.H.Kosel.1@nd.edu), A. Seabaugh (seabaugh.1@nd.edu), M. Wistey (mwistey@nd.edu), G. Xing (hxing@nd.edu) Notre Dame
    - 5.3 Heterojunction p-i-n Tunnel Transistor Logic and Architectures. PIs: S. Datta (sdatta@engr.psu.edu), V. Narayanan (vijay@cse.psu.edu), T. Mayer (tsm2@psu.edu), Penn State
    - 5.4 Nanofabrication Platform for One Dimensional Nanowire Tunnel Transistors. PIs: T. Mayer (tsm2@psu.edu), S. Datta (sdatta@engr.psu.edu), Penn State
    - 5.5 Characterization of Tunnel Field-Effect Transistor Interfaces. PIs: R. Wallace (rmwallace@utdallas.edu), J. Kim (jiyoung.kim@utdallas.edu), UT-Dallas
    - 5.6 Graphene Nanoribbon Tunnel Field-Effect Transistors (GNR TFETs). PIs: D. Jena (djena@nd.edu), G. Xing (hxing@nd.edu), Notre Dame

Conclusion

Thanks!

We now invite further questions from listeners.

(The answers to the following questions are abbreviated versions of the off-the cuff answers given during the meeting.)

Q&A

submitted during the meeting

- Q: Can you give any update on the FCRP selection process? The Oct. 13 deadline has passed.
- A: If you have not heard that your FCRP proposal has been selected, then you may assume that your proposal was not among the first tier of selected proposals. You will receive a final yes or no answer in two weeks.

- Q: You said that the subcontractors do not need to run their budgets through their OSPs. Is that true for the primary university also?
- A: Primary universities should submit budgets that have been run through their normal internal approval process.

Q&A (continued)

submitted during the meeting

- Q: What are the highest priorities for nano-metrology? Electrical measurements? Critical dimensions? Material properties?
- A: The measurements pursued should be those most critical to demonstrating and developing the proposed device concept and it's associated circuit architecture. We cannot overemphasize the importance of putting device and architecture *first* in your proposal.

- Q: How close an involvement by NIST is acceptable? Can we have students and post docs working side-by-side with NIST personnel at a NIST location?
- A: We encourage strong collaborations, including students or post-docs working side-by-side with NIST personnel at a NIST location.

- Q: Can we budget for use of NIST facilities?
- A: You cannot use NRI funds to pay for use of NIST facilities. You could use matching university or state funds for that purpose.

- Q: Can NIST personnel serve as advisors for graduate students since their work under this grant would be part of their PhD research?
- A: That arrangement would be between the university and NIST.

Q&A (continued)

submitted during the meeting

- Q: Do we need preliminary results for the really new concepts you just talked about?
- A: No, but if the device concept and circuit architecture are purely theoretical, it is even more important to provide a physical argument or device model showing why this approach, if successfully demonstrated, will provide advantages over the field effect transistor for computing applications.

- Q: How essential is it to find university/state/federal matching funding? Is acceptance of a Center proposal by NRI contingent on the availability of such funding?
- A: Acceptance of a proposal is NOT contingent on the availability of university/state/federal matching funding. The availability of such funding will be one of many factors considered in proposal selection.

Q&A (continued)

submitted during the meeting

- Q: The RFP and this presentation mentioned new sensor devices. What sort of sensors would be of interest?
- A: We do not have preference for a particular sort of sensor, but generally speaking, we envision a sensor which provides input to and is an intimate part of a system or subsystem performing some important computational function.

- Q: When do we expect a similar call like this one if we can't meet the deadline this time?
- A: This new phase of the NRI program will run for 5 years. We do not have plans for a similar call for new center proposals during that time period. We do plan each year to jointly fund, along with NSF, new projects and smaller centers under NSF's Nanoelectronics for Beyond 2020 (NEB2020) program.

- Q: How many centers are you going to fund?
- A: As it says in the RFP, we plan to fund 2 to 3 centers. We would rather have adequate funding for each PI within a few centers than spread the funding thinly across many centers and many more PIs.

Q&A (continued)

submitted during the meeting

- Q: After the evaluation process, is there any plan for NRI to try to mix and match PIs from different proposals into a single center?
- A: We plan to select two or three of the proposals that we receive. We do not have a plan to "mix and match" PIs. However, if we see one or more particularly promising ideas that are not supported in the centers that we choose, we may enter into discussions about bringing the appropriate team or teams into one or more of the chosen centers.

- Q: Can a PI participate in both FCRP and NRI?
- A: Yes, as long as the FCRP-supported research is clearly distinct from the NRI-supported research.

- Q: If the work involves building a chamber to deposit the required novel material, can NRI funds be used for this capital?
- A: Yes. Any significant equipment purchases should be broken out in your proposed budget.