Semiconductor Manufacture and Potential Vulnerabilities

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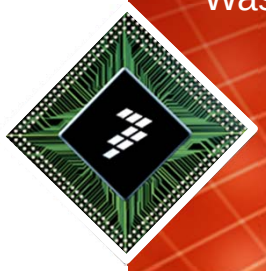
Software Assurance and Trustworthy Semiconductor Workshop
January 15 - 16, 2013
Washington DC



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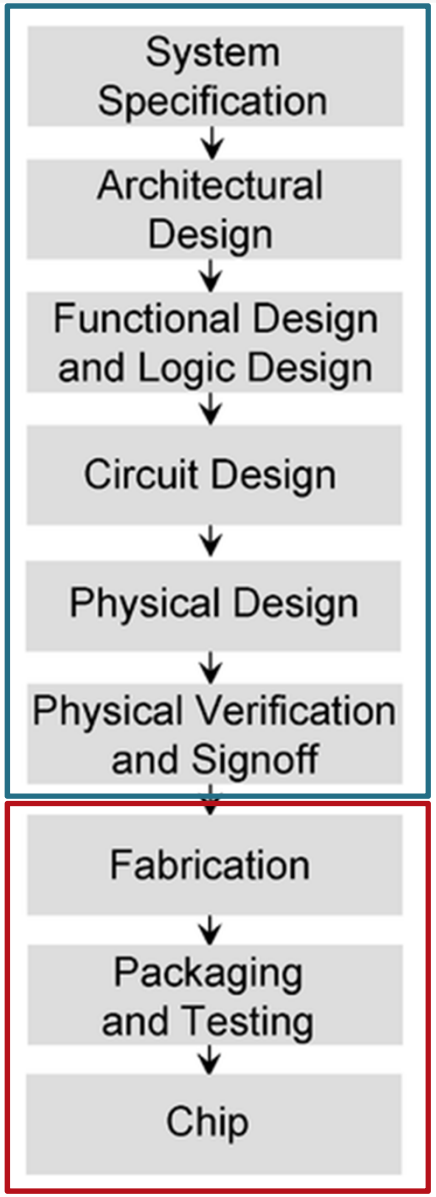
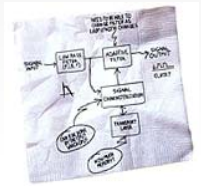
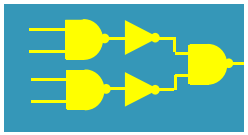
Integrated Circuit Design and Manufacturing Flow

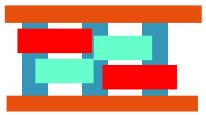




The first step is to define the functional specification and architecture of a chip to meet the needs of a particular application or market (e.g. computer processor, cellular transceiver, memory chip, microcontroller…)



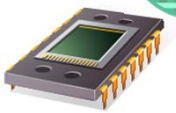
This step converts the specification into a register transfer level (RTL) description. The RTL describes the exact behavior of the digital circuits on the chip, as well as the inputs and outputs.



The chip design is assembled from the RTL using a library of available logic gates. This involves figuring out which gates to use, where to place them, and how to wire them together.

Many checks happen throughout the design process, and there is a detailed set of checks before the design is sent to the wafer fab.

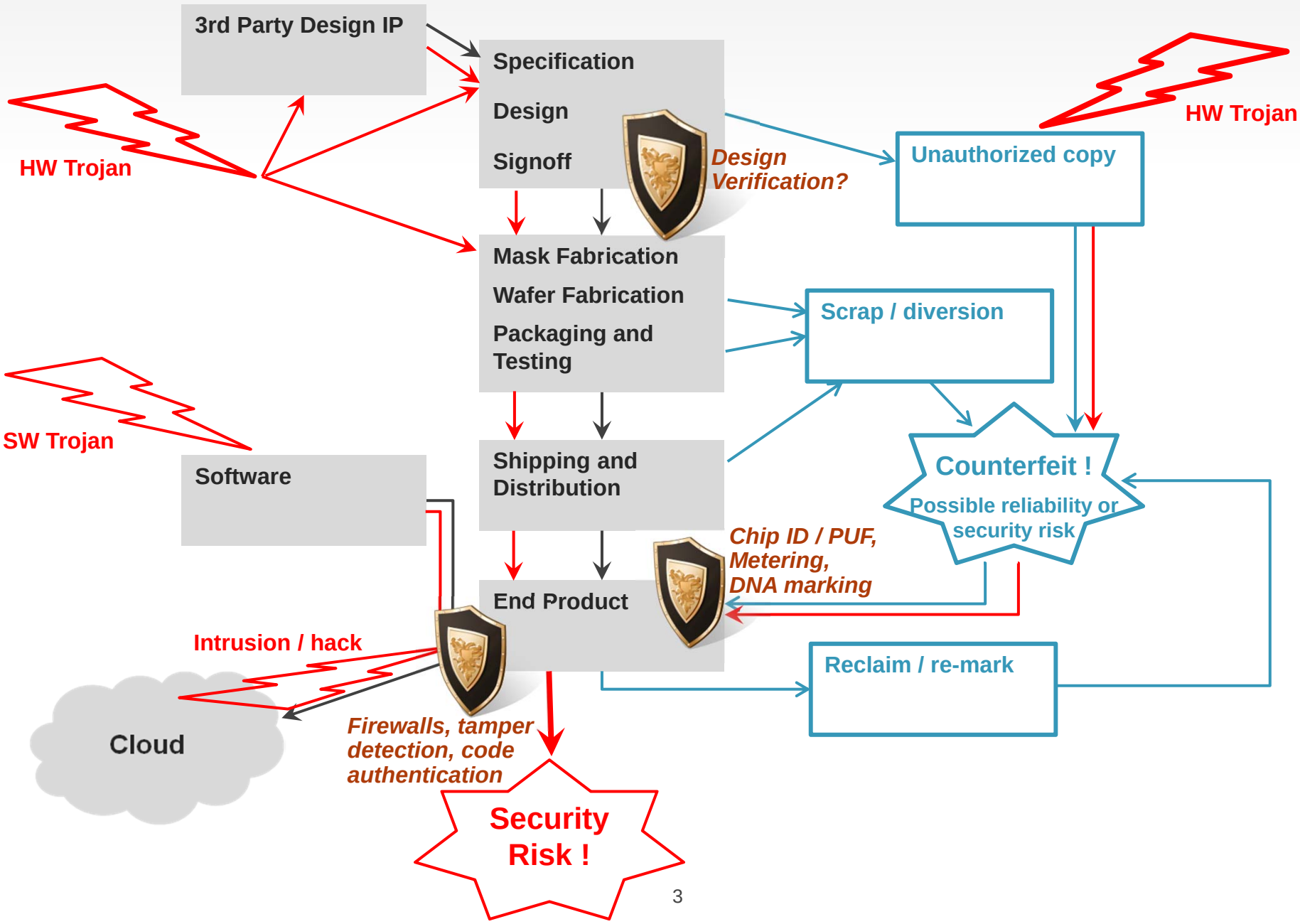
The physical design is etched into silicon wafers using a photolithography process to form the actual transistors and wiring.



Wafers are diced into chips and assembled in packages to be attached to a circuit board in the end product.

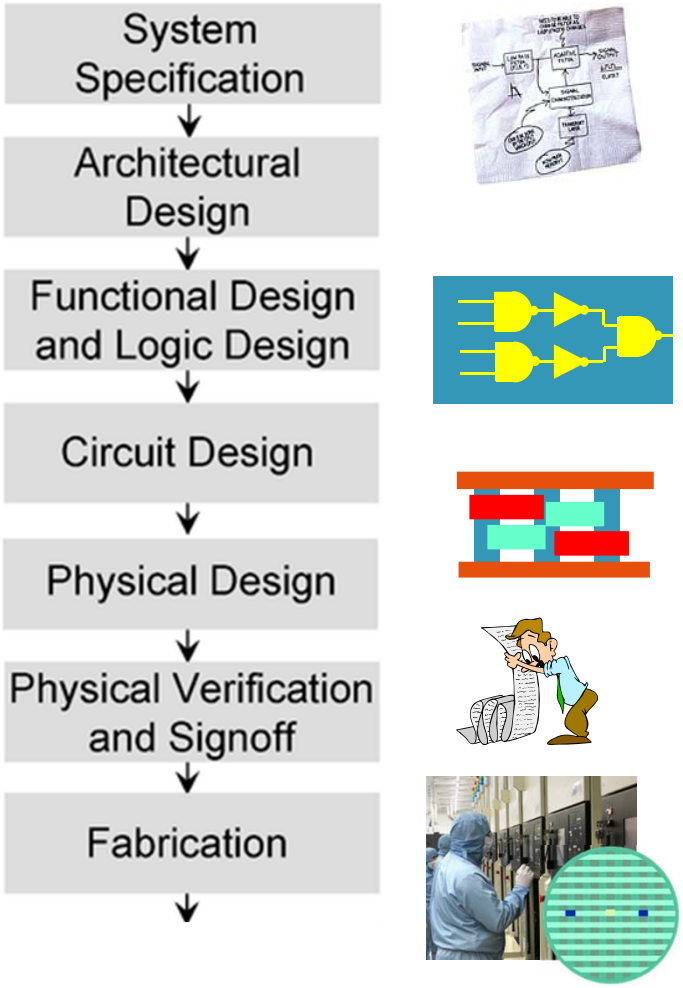
http://en.wikipedia.org/wiki/File:Integrated_circuit_design.png

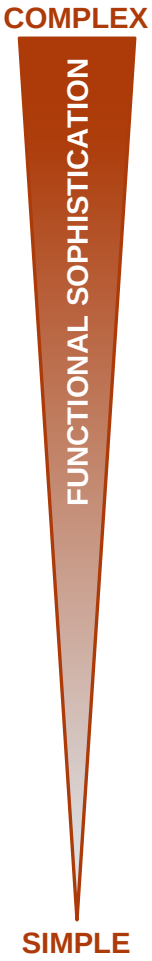
A Secure IC Design and Manufacturing Flow?



Hardware Trojans in IC Design Flow

Examples: Back doors, Time bombs, Side-channel communication paths…



HW Trojan Insertion

- Incorporate malicious behavior in specification / architecture
- Add logic triggers, counters, etc. to RTL
- Manipulate layout to add gates and wires
- Modify GDS data prior to mask fabrication
- Induce defects to reduce reliability or disable security features