Scalability of $BaTiO_3$ based ferroelectric tunnel junctions (FTJs)

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Semiconductor Research Corporation

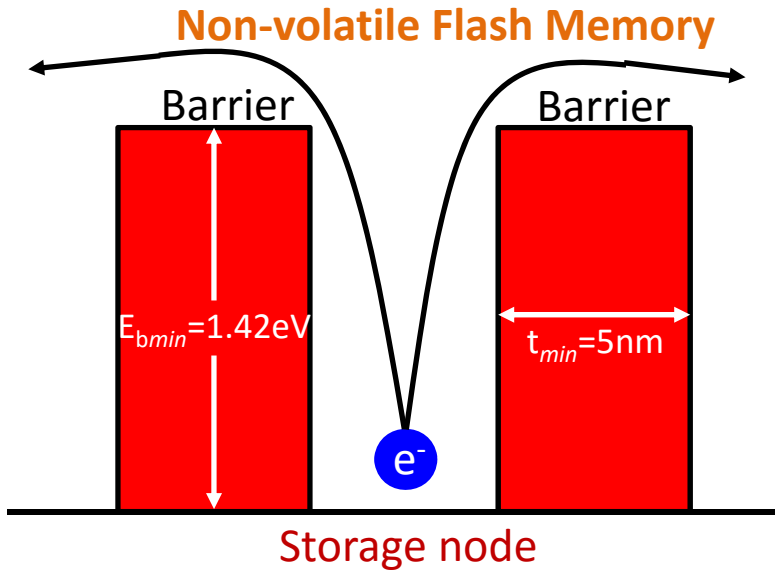
NRI Theme: 2398.002

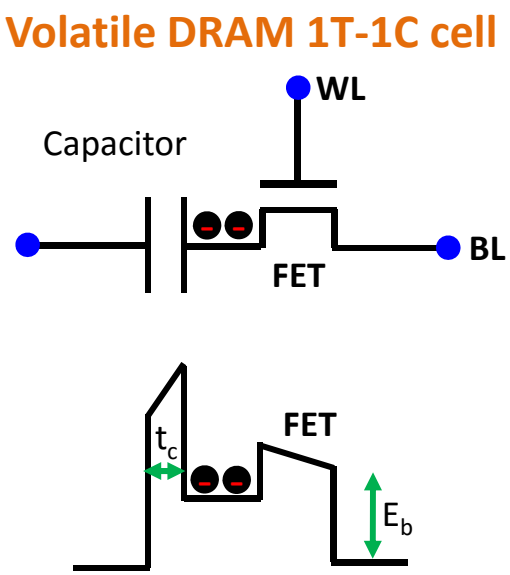
Outline

- Introduction and motivation
- Background and previous work
- Integrated sub-micron FTJ device process
- Measurement results
- Conclusion

Motivation

Scaling limit of charge-based memory (DRAM, SRAM, NAND/NOR Flash)



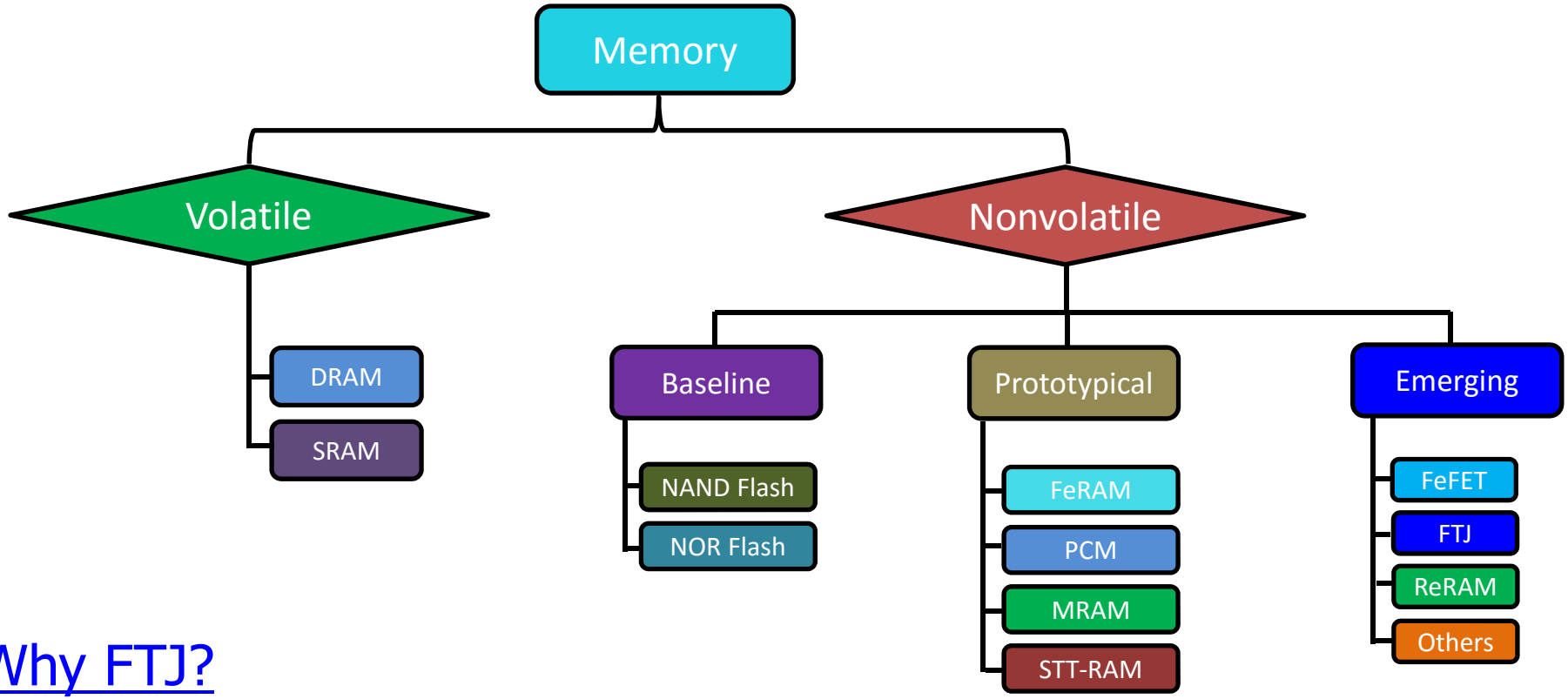


Scaling effects (t_c<5nm & A_c<10x10nm^2)

- Stored charge escaped by thermionic emission & quantum tunneling → poor retention → reliability issue.
- Min^m DRAM cell size ~10nm for readout & sensing.
- R_c in DRAM cell increased → E_{write} & speed suffers.

Motivation

Memory Taxonomy (ITRS 2013)

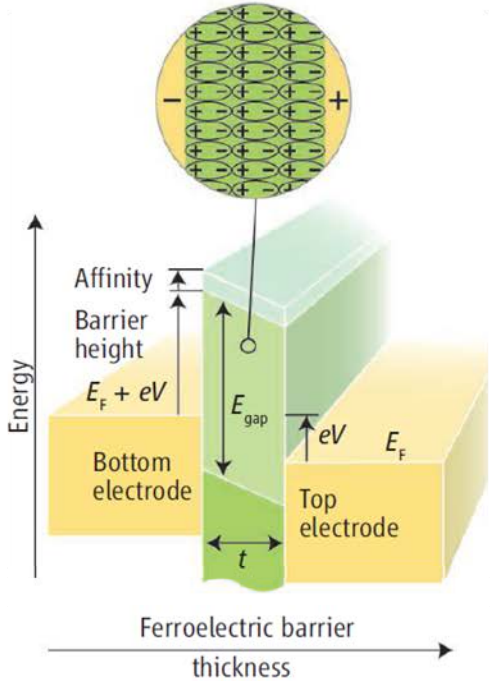


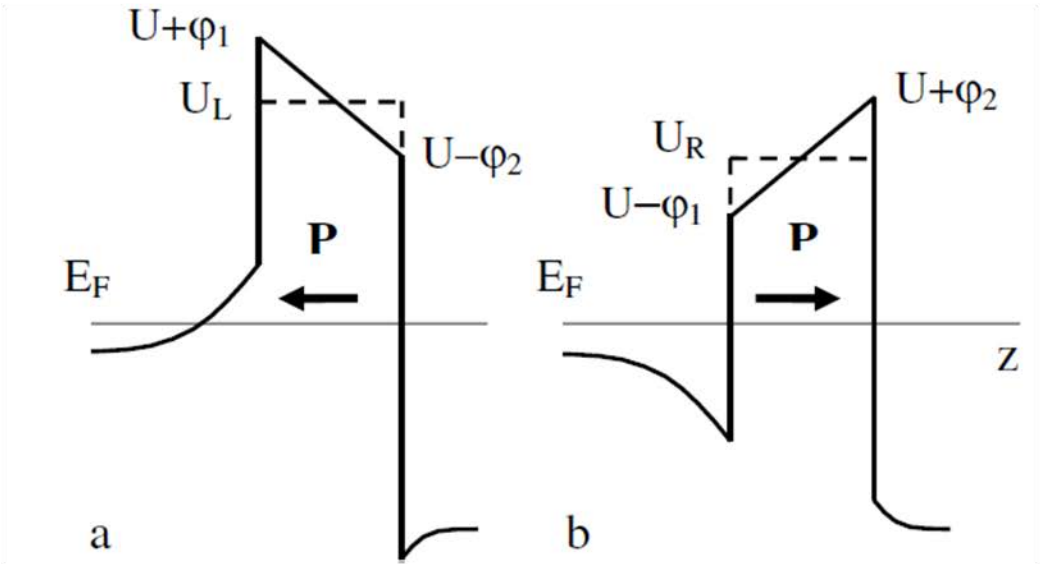
Why FTJ?

- Non-charge based beyond CMOS memory.
- Scaling beyond physical limit (t_c<5 nm).
- Cell size <10nm.
- Mechanism fully electronic.

Ferroelectric tunnel junctions (FTJs)

Tsymbal *et al.* Science 313(5784): 181-183.





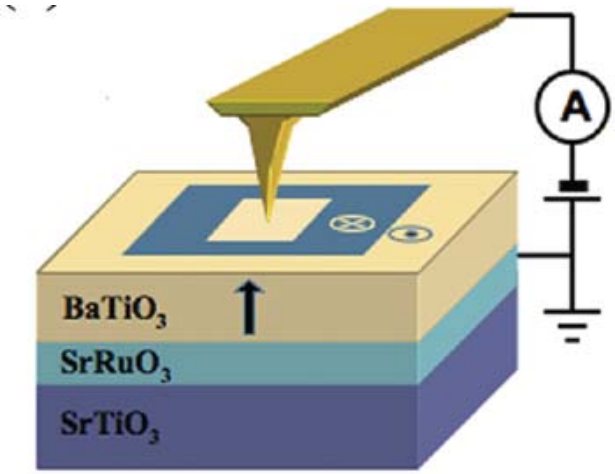
Zhuravlev, M. Y., *et al.* Physical Review Letters 94(24): 246802.

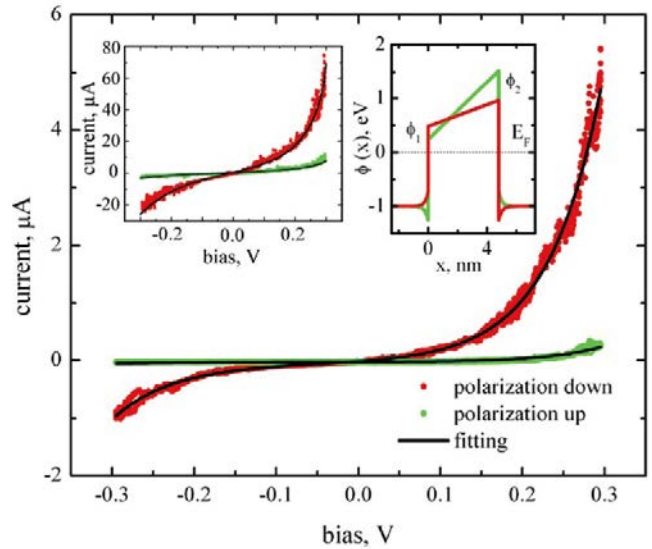
Ferroelectric tunnel junction (FTJ) devices

- Tunnel current modulated by the polarization of FE material
- Long screening length (l_s) for large ON/OFF ratio
- Small workfunction (Φ) difference for long FE retention
- Non-volatile state → novel FTJ based circuits

Non-integrated FTJs

Gruverman, A., et al. (2009). Nano Letters **9**(10): 3539-3543.



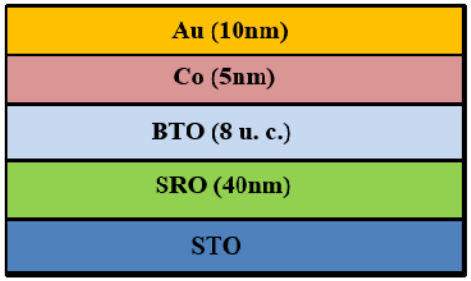


FTJ using PFM techniques

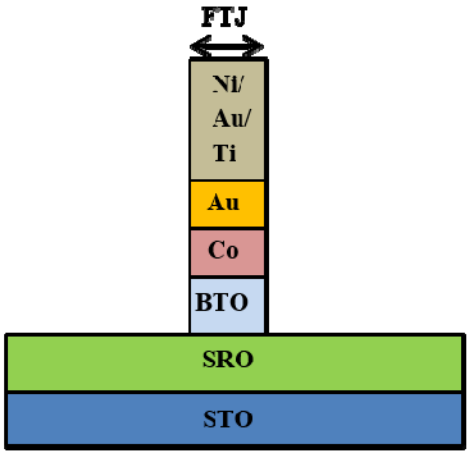
- Measure ferroelectricity & switching to test device structure.
- PFM can't be probed <50nm FTJs
- Hard to check scalability & CMOS compatibility
- High speed switching & RF measurement not possible

Full integration required for benchmarking of FTJ?

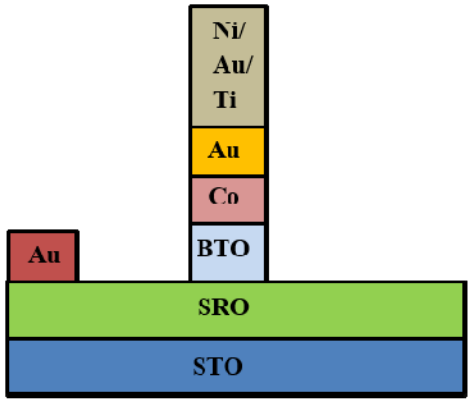
Scalable sub-micron FTJ process flow



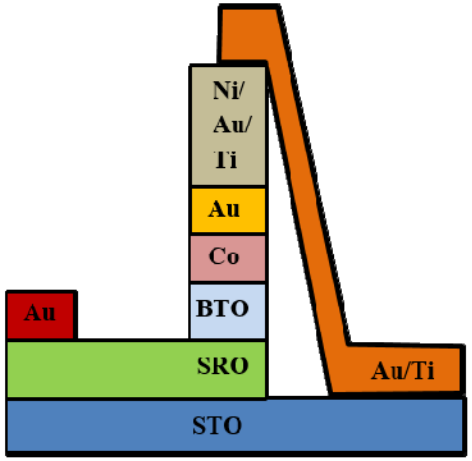
(a) Blanket SRO/BTO/Co FTJ



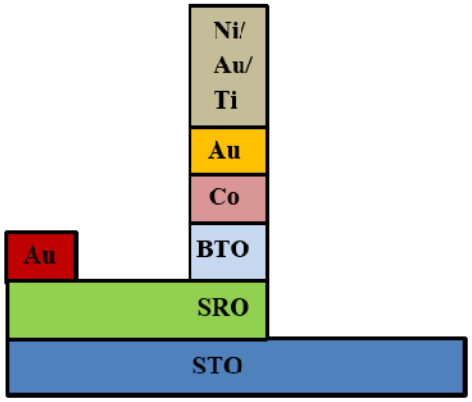
(b) FTJ EBL patterning & RIE



(c) Bottom metal contact PAD (Au)

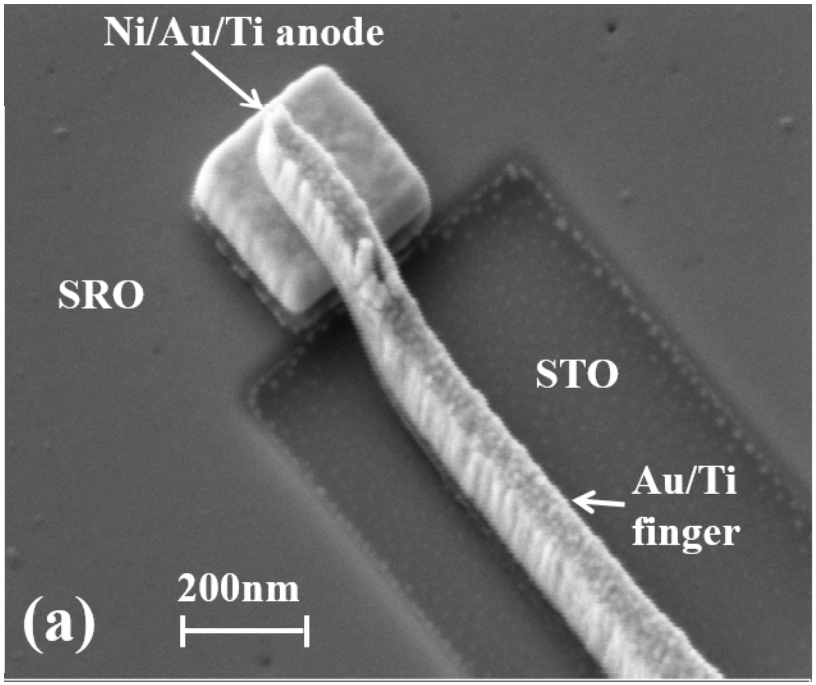


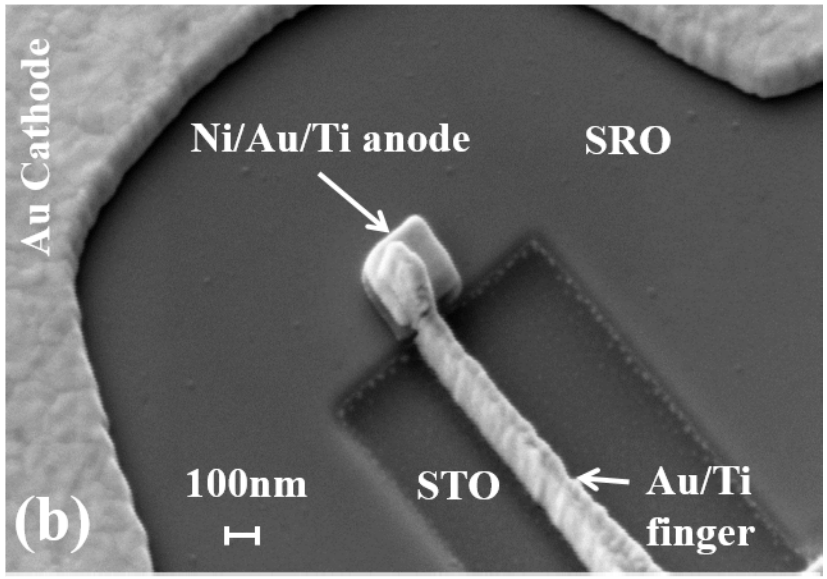
(e) Contact PAD with finger



(d) FIB to etch SRO

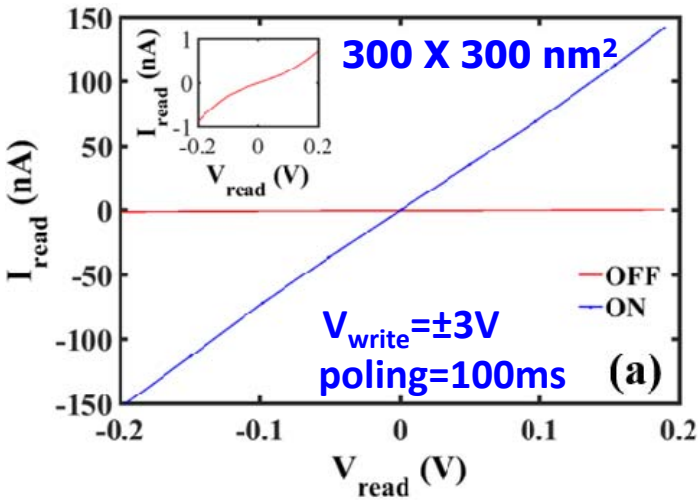
Fully integrated submicron FTJ

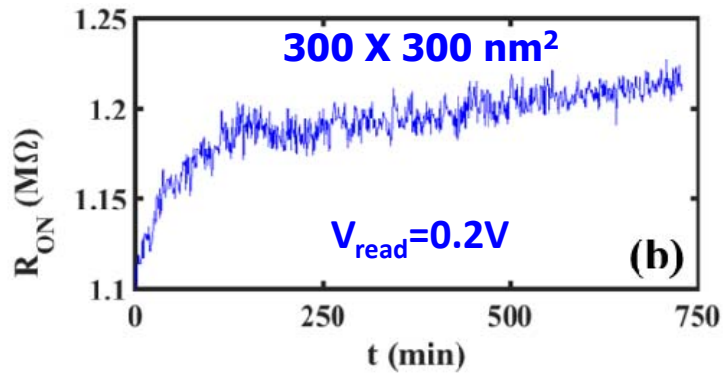




- Minimum device area 300 X 300 nm^2
- Leakage current is negligible (3μA/cm^2) through STO
- Process yield is poor
- FTJs show switching behavior

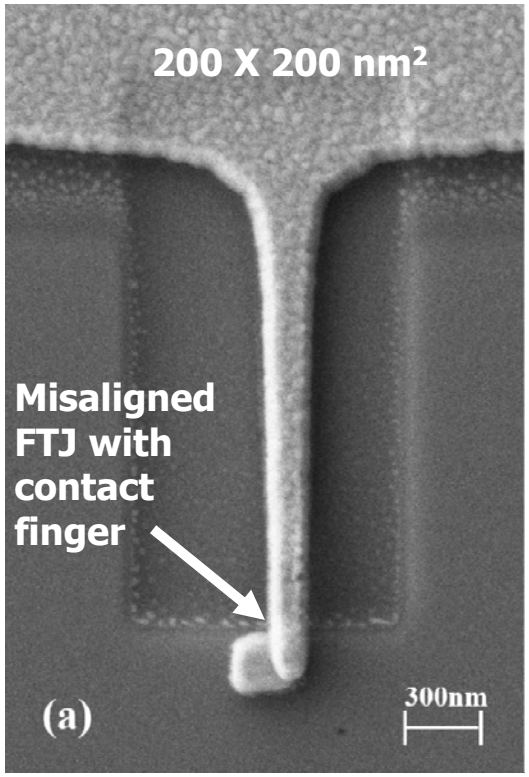
Integrated submicron FTJ switching

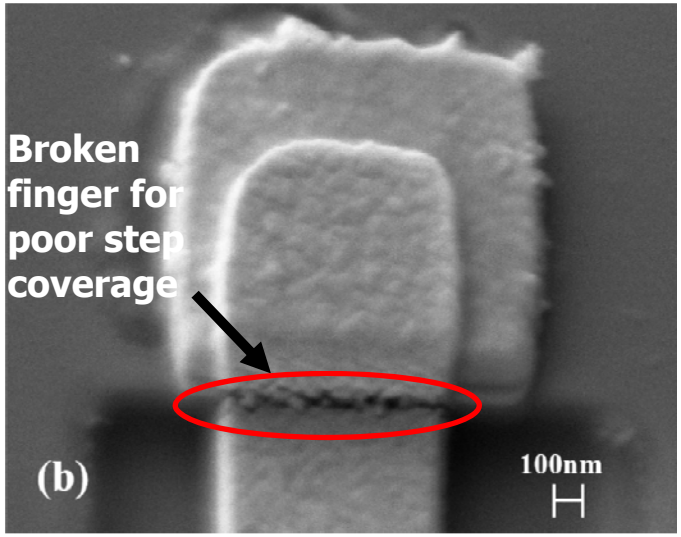




- Hp-4155B parameter analyzer used for I-V
- V_{write}=±3V, poling=100ms, V_{read}=0.2V
- J_{ON}=75A/cm^2, J_{OFF}=0.28A/cm^2, ON/OFF ratio=270
- Large J_{ON} promising for scaling sub-50nm FTJ
- R_{ON} decay (10%) over 12h→ by LABVIEW program

Challenge's below sub-100nm FTJ processing

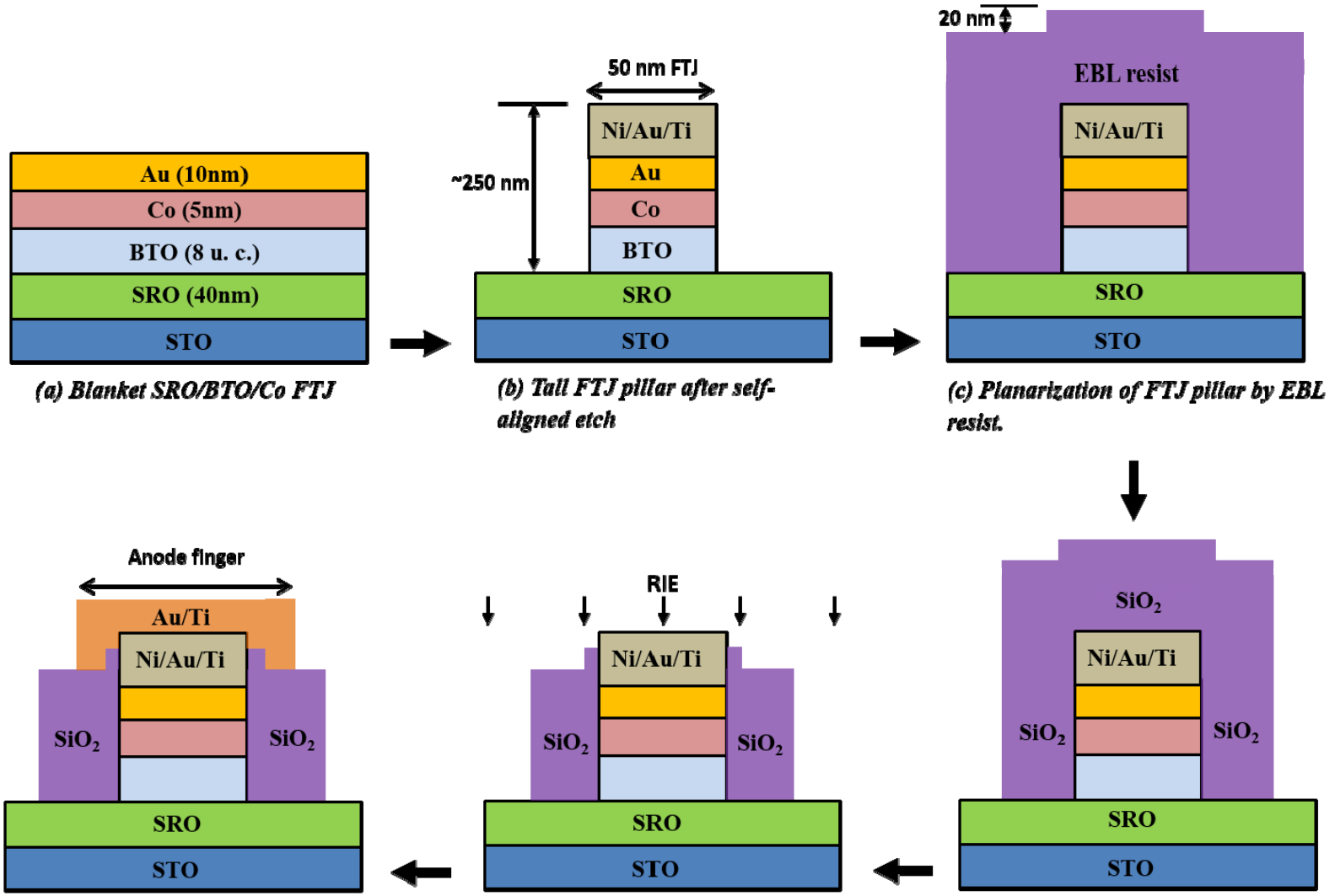




- Alignment is critical below 100nm
- FIB ion-milling difficult→ damages intrinsic FTJ
- Sidewall metallization difficult→ poor yields

New process required for sub-50nm FTJ!!

Sub-50nm FTJ process flow



(a) Blanket SRO/BTO/Co FTJ

(b) Tall FTJ pillar after self-aligned etch

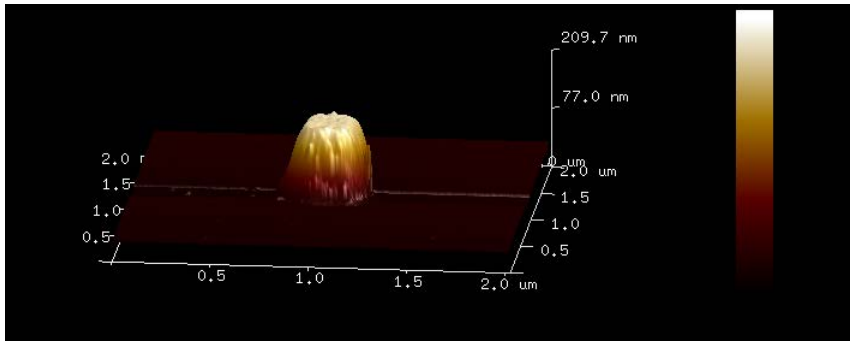
(c) Planarization of FTJ pillar by EBL resist.

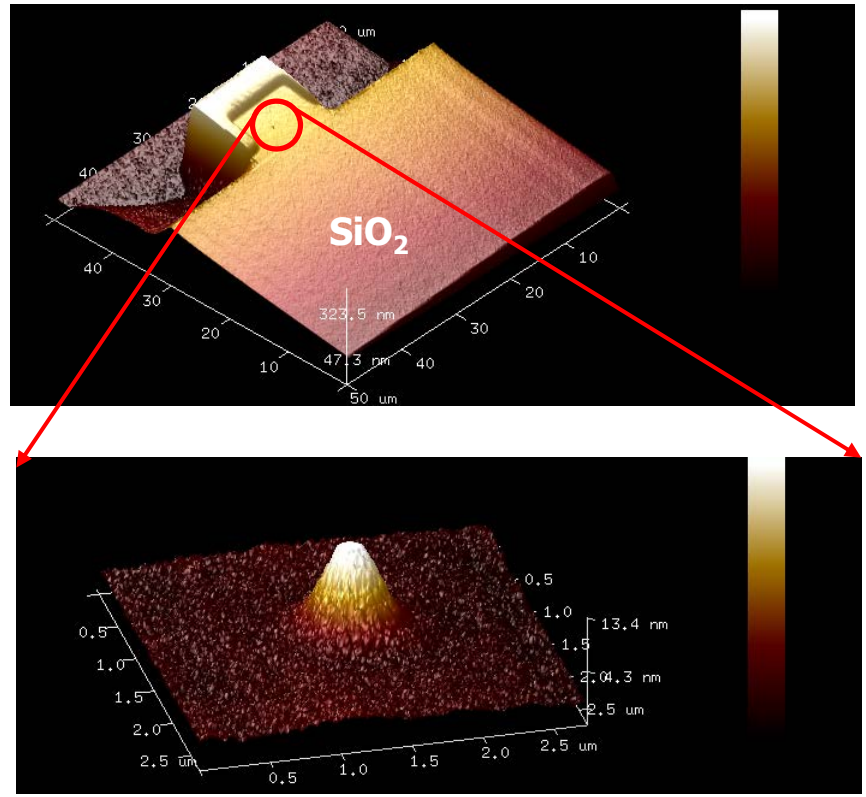
(d) EBL resist exposed and developed for patterning SiO_2 pillar on FTJ.

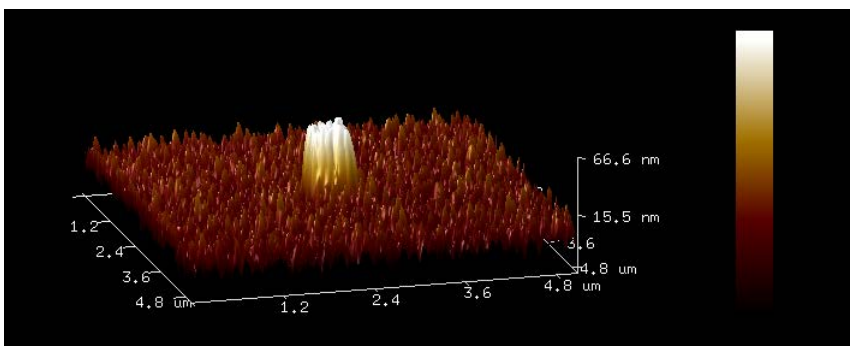
(e) Blanket RIE of SiO_2 to uncover FTJ pillar top metal (Ni/Au/Ti).

(f) Au/Ti anode finger on SiO_2 to connect FTJ top metal (Ni/Au/Ti).

Sub-50nm FTJ planarization

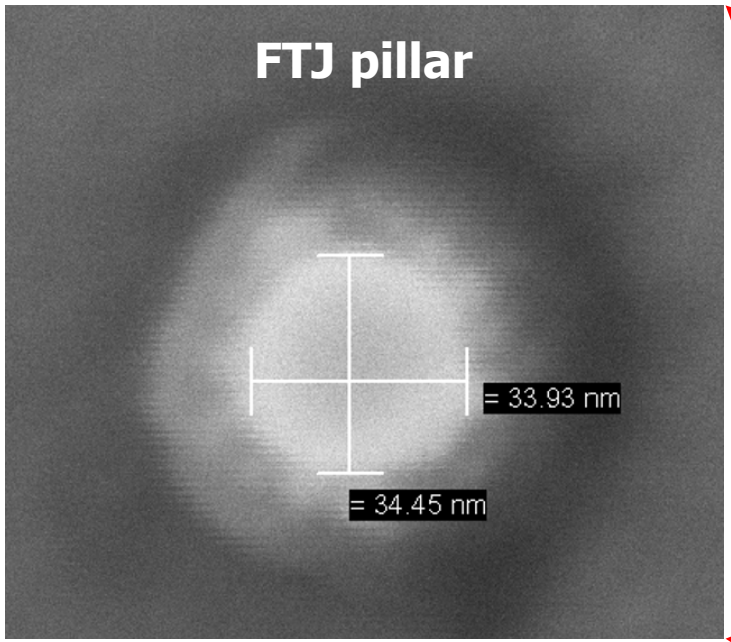


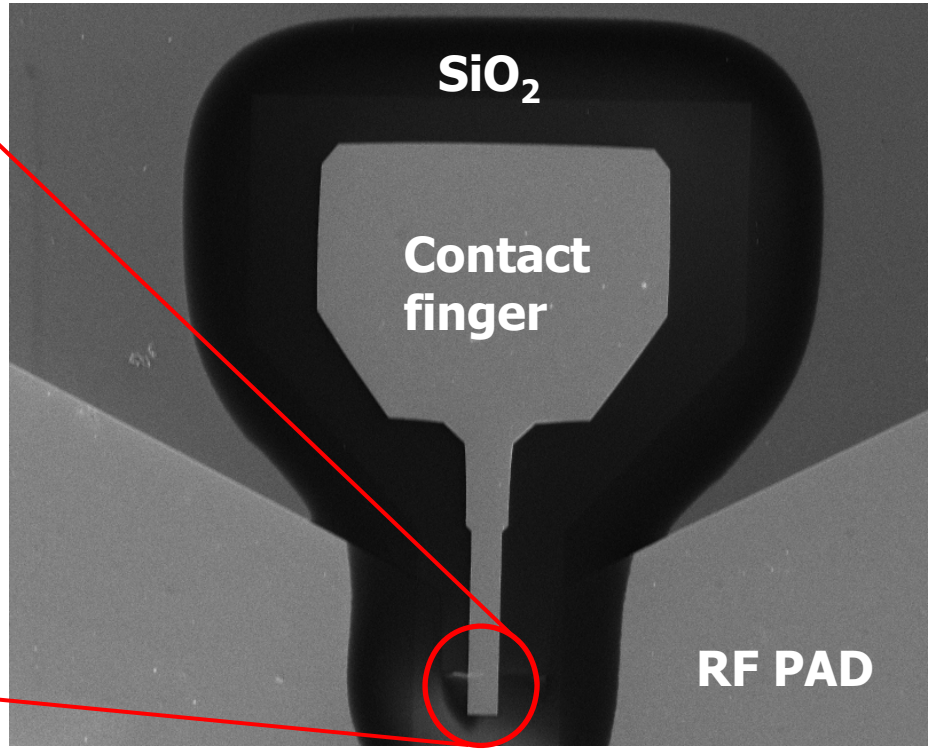




- The 200nm FTJ pillar planerized by EBL resist
- Bump height is ~20nm
- Etching SiO_2 by RIE open FTJ top

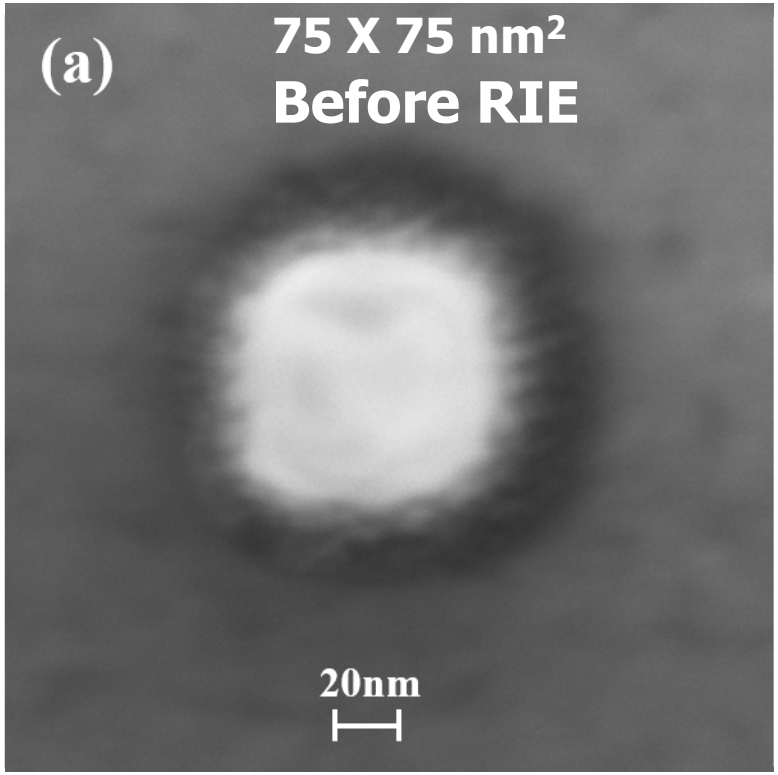
Sub-50nm FTJ fabrication

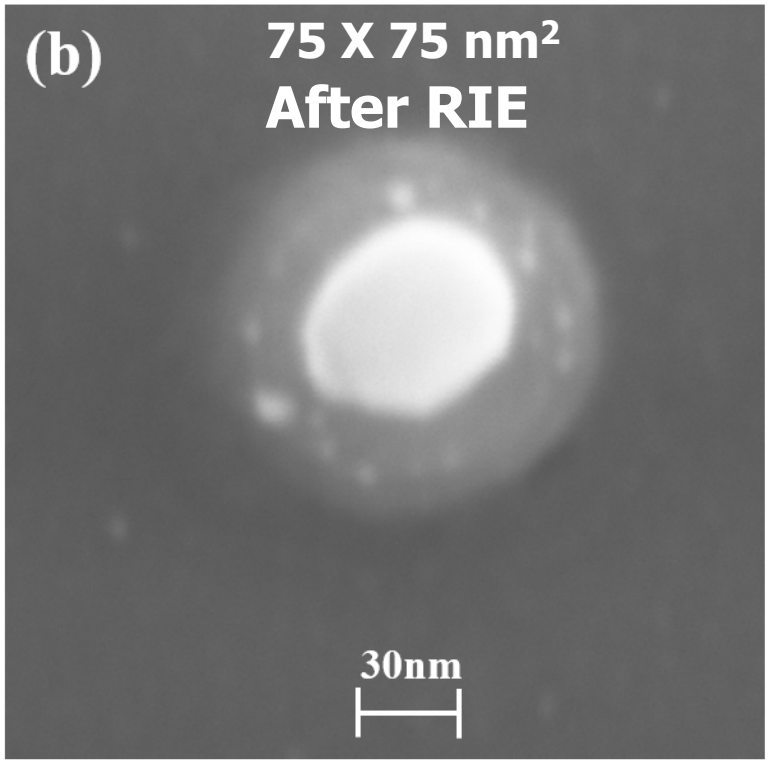




- JEOL JBX 100kV EBL used
- Minimum FTJ fabricated 30 x 30 nm^2
- FTJ pillar height ~200nm

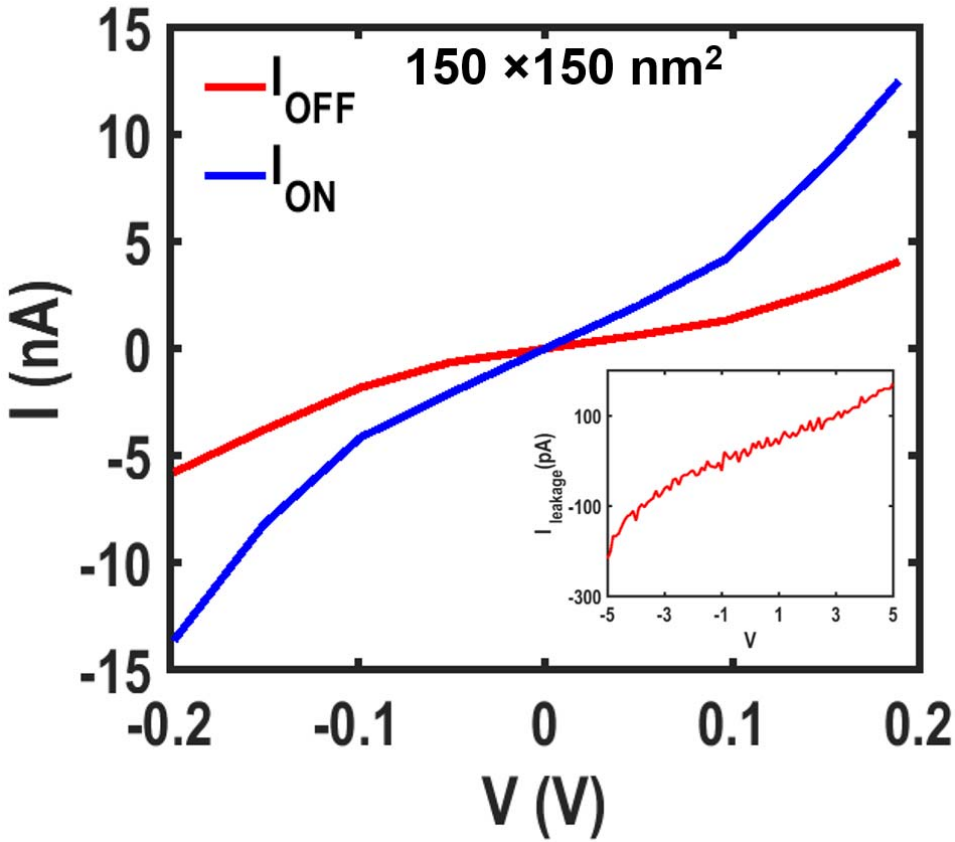
Self-aligned etch sub-50nm FTJs

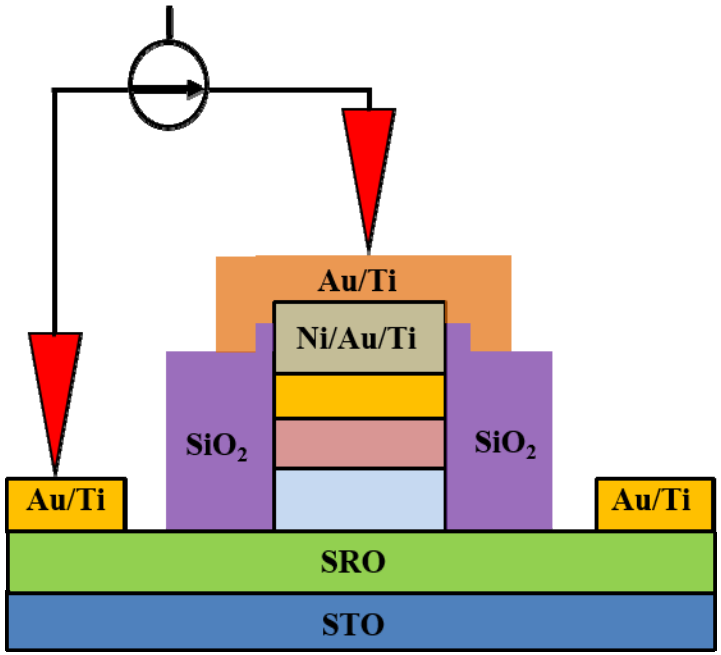




- Undercut →FTJ size reduction
- RIE damages FTJ sidewall→ FE layer dmagaes
- Solution→ BTO sputtering

Measurements of integrated FTJs





- Hp4155B & probe station was used for I-V
- Switching observed for 150x150 nm^2 FTJ
- Leakage through 400nm SiO_2 $I_{leakage}$ (100pA)<<I_{OFF} (5nA)

Conclusion and future work

- **Integrated submicron FTJ process demonstrated**
- **FTJ switching in sub-micron process**
- **Adressing sub-100nm FTJ process challenges**
- **Sub-50nm fully integrate FTJ process demonstrated**
- **Sub-50nm FTJ device fabrication and results**
- **High speed and RF measurement in future**

Tech Transfer

Industry liaison's:

Intel, Micron, IBM, GLOBALFOUNDRIES

Peer Review Journals:

1. "Scaling of Electroresistance Effect in Fully Integrated Ferroelectric Tunnel Junctions", M. Abuwasib, H. Lu, T. Li, P. Buragohain, H. Lee, C.-B. Eom, A. Gruverman and U. Singisetti, Applied Physics Letters, 108, 152904, (2016).
2. "Contact resistance to $SrRuO_3$ and $La_{0.67}Sr_{0.33}MnO_3$ epitaxial films", M. Abuwasib, H. Lee, C.-B. Eom, A. Gruverman and U. Singisetti, Applied Physics Letters, 107 (24), 242905, (2015).

Conference Publications:

1. "CMOS compatible integrated ferroelectric tunnel junctions (FTJ)", M. Abuwasib, H. Lee, P. Sharma, C-B. Eom, A. Gruverman and U. Singisetti, 2015 IEEE Device Research Conference (DRC), Ohio State University, Columbus, OH, USA.
2. "Fabrication and Characterization of Integrated Ferroelectric Tunnel Junctions (FTJs)", M. Abuwasib, H. Lee, P. Sharma, C.-B. Eom, A. Gruverman and U. Singisetti, TECHCON 2015, Semiconductor Research Corporation (SRC) Annual Conference, Austin, Texas, USA.

Poster Presentations:

1. "Deep-sub-micron integrated FTJ devices: process, scaling challenges and solutions", M. Abuwasib, Hyungwoo Lee, Haidong Lu, C. B. Eom, A. Gruverman, J. P. Bird, U. Singisetti, Center for Nanoferroic Devices (CNFD) Onsite Review, University of Nebraska/Lincoln on September, 2015.
2. "Fabrication and Characterization of Ferroelectric Tunnel Junction (FTJ) Diode for Future Non-Volatile Memory Cell", M. Abuwasib, Hyungwoo Lee, C. B. Eom, A. Gruverman, J. P. Bird and U. Singisetti, Center for Nanoferroic Devices (CNFD) Onsite Review, University of Nebraska/Lincoln on September 23, 2014.

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