A Concatenable Magnetoelectric Magnetic Tunneling Junction (MEMTJ) Computational Device

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NRI THEME 2624.001

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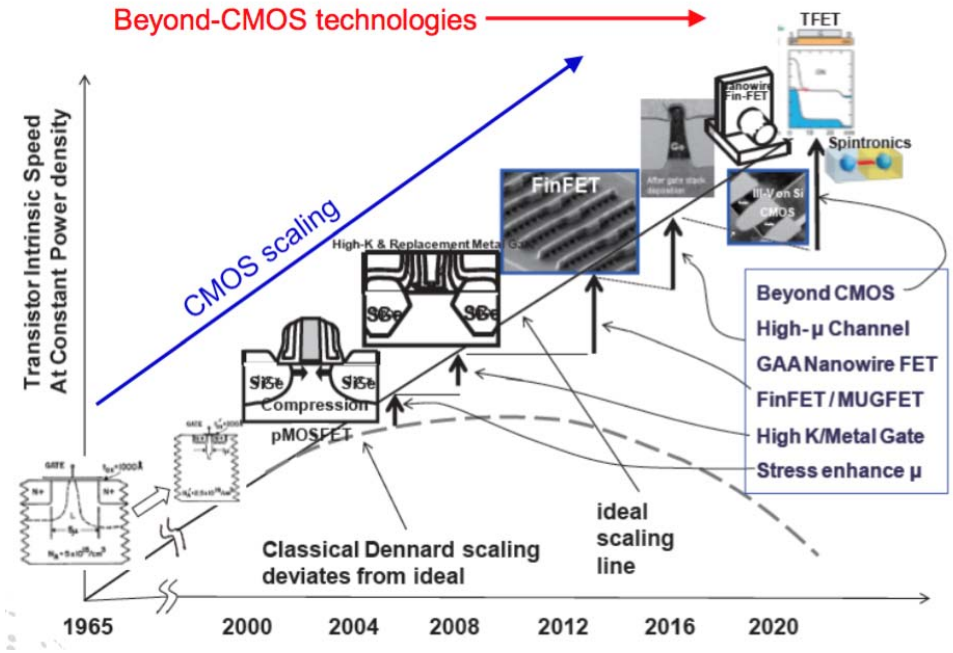
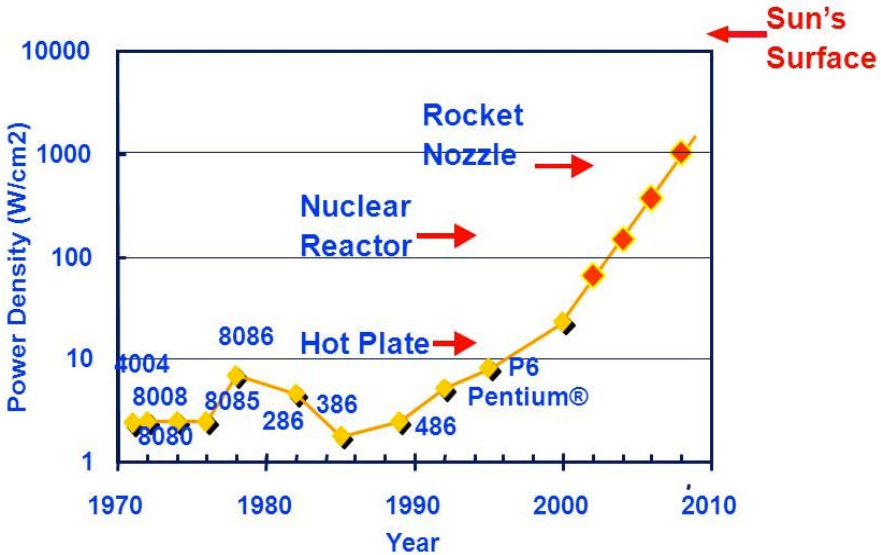
50 years of Moore's Law



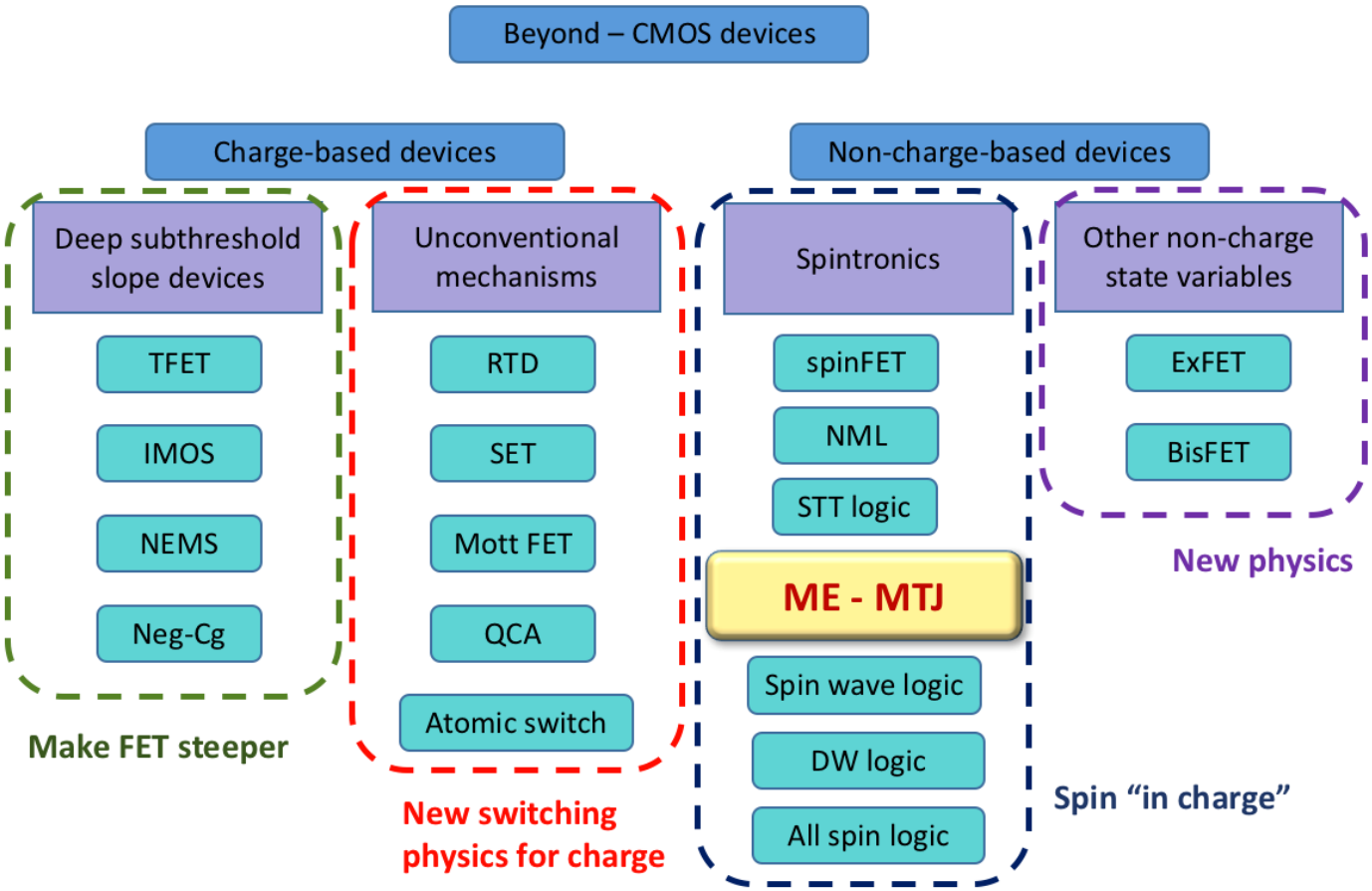
Source: Sun, J Y-C., *VLSI Technology (VLSIT), 2013 Symposium on*. IEEE, 2013.



Source: Borkar, De Intel

Emerging devices

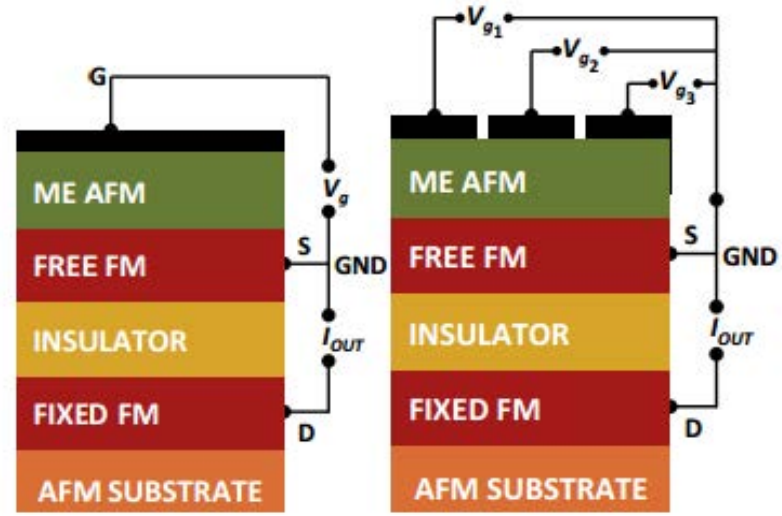
Beyond-CMOS devices for low-power solution?



Adapted from: www.electroiq.com/;
IEDM 2012-Nanoelectronics provide a path beyond CMOS

Magnetoelectric Magnet Tunnel Junction (ME-MTJ)

Original proposal: Device/circuit concepts from N. Sharma, A. Marshall, J. Bird, and P. Dowben [1,2]



Basic Cell Majority Gate

Basic Operation

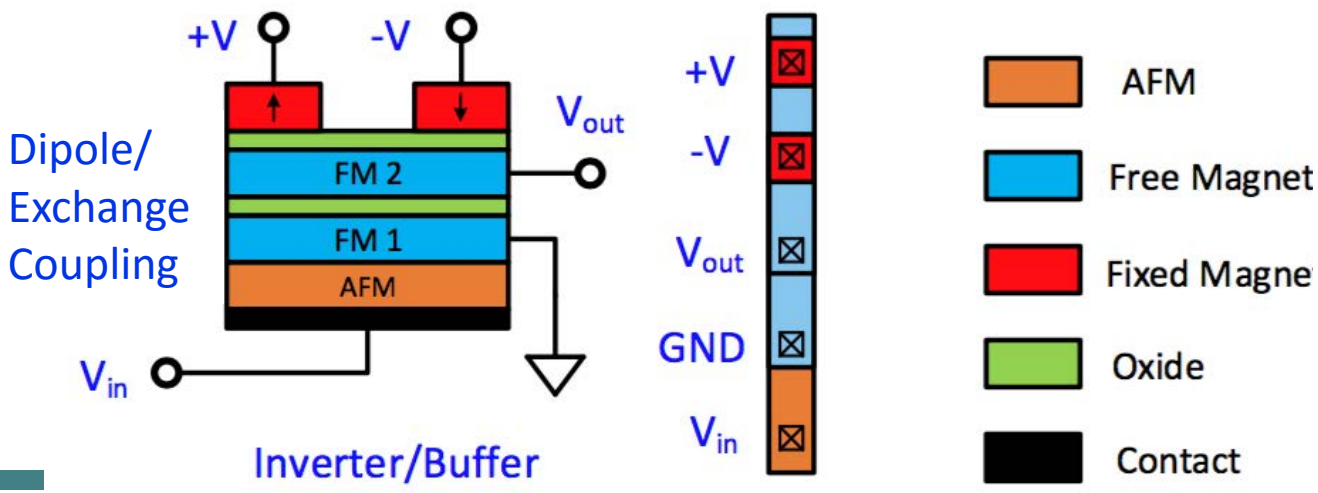
- ❑ Voltage induced change in boundary magnetization, generates exchange bias field to switch the free magnet
- ❑ Free magnet magnetization determines the output MTJ resistance
- ❑ MTJ resistance value converted to voltage by passing a current with a MOSFET.

[1] N. Sharma, et. al., *Energy Efficient Electronic Systems (E3S), 2015 Fourth Berkeley Symposium on*, 2015, pp. 1-3.
[2] N. Sharma, et. al., *Circuits and Systems Conference (DCAS), 2015 IEEE Dallas*, 2015, pp. 1-4.

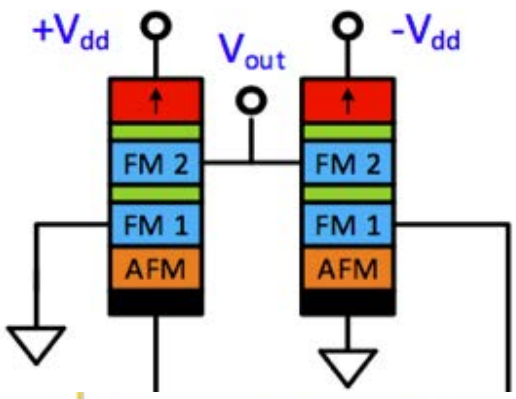
Proposed device structure

Modified structure

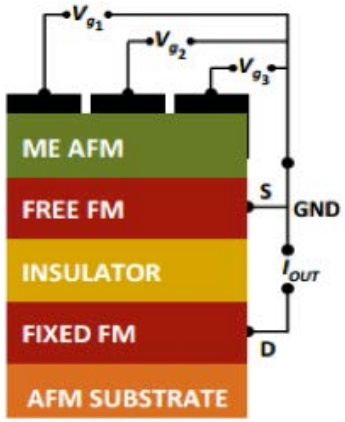
- A concatenable stand alone ME MTJ device with less number of FETs
- Using two MTJ stacks (opposite magnetization of fixed magnets) on top to provide complementary output
- Output voltage can directly drive next stage (concatenability)
- Separate pull-up and pull-down networks, same magnetization of fixed magnets on top – avoid fabrication challenges.



Alternative



Proposed majority gate using MEMTJ

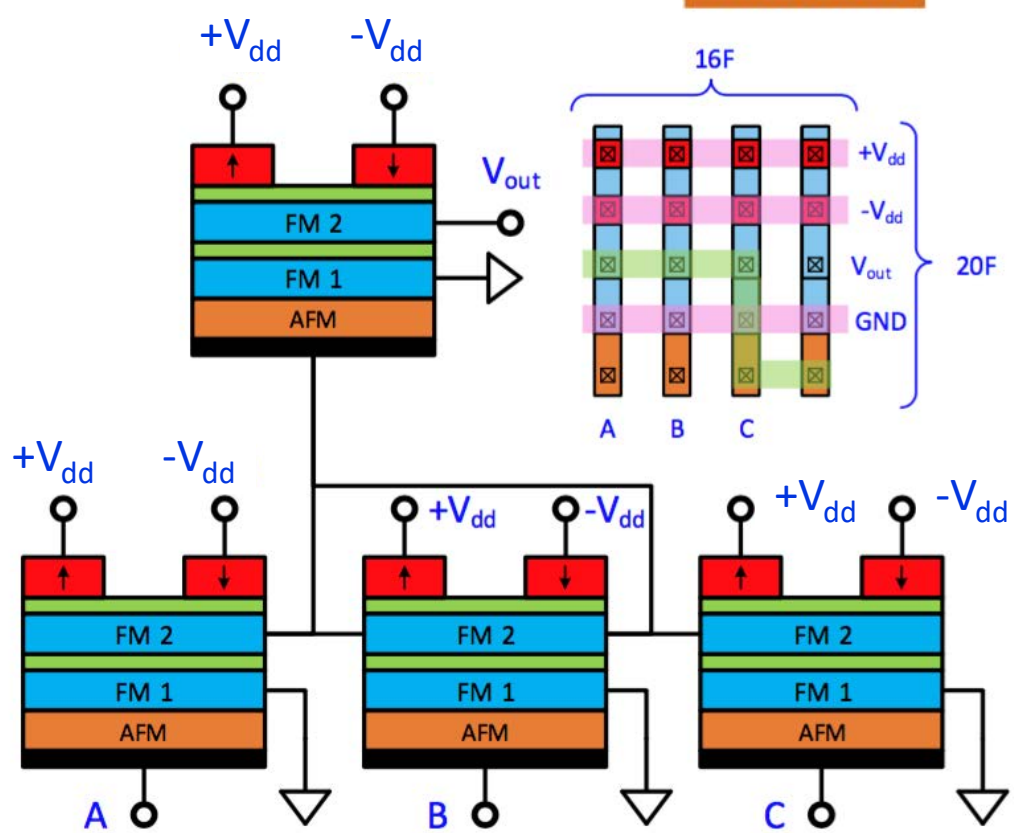


Previous proposal

- Connects the three inputs directly to the AFM
- Assumption of single-domain magnet switching may not be valid

Modified proposal

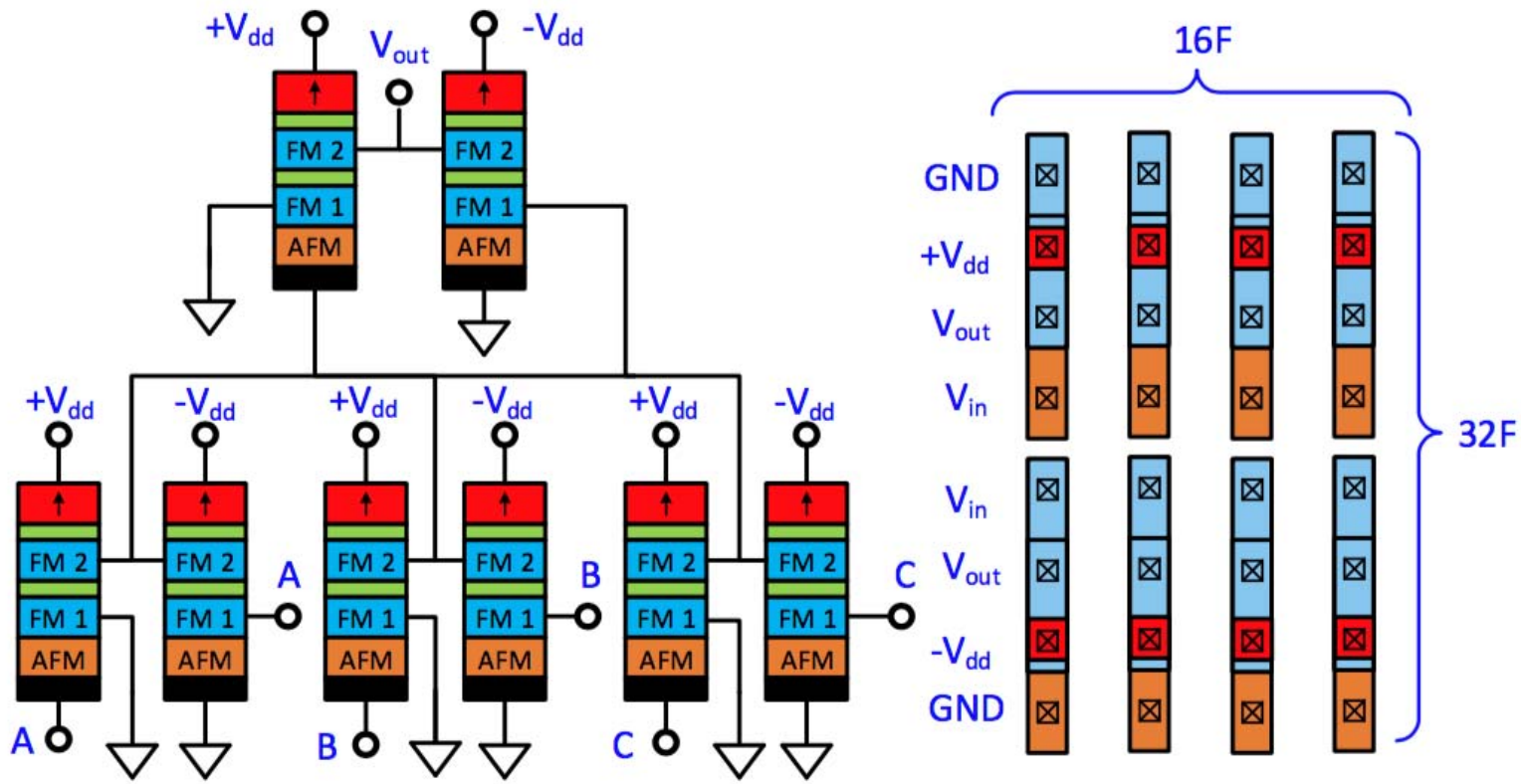
- Two-stage majority gate with four basic MEMTJ devices
- Stable error-free switching behavior



Proposed majority gate using MEMTJ

Alternative design

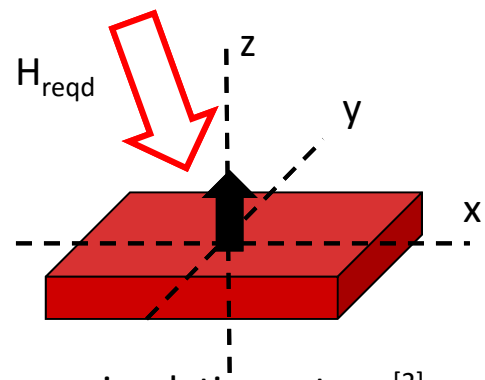
- Use separate pull-up and pull-down networks
- Larger footprint area and input capacitance due to the extra terminals and vias.



Modeling approach

Switching Time of Free FM layer

- Dimension = 210 x 30 x 10 nm^3
- Saturation magnetization M_s = 650 kA/m*
- Perpendicular anisotropy K_{PMA} = 0.19 MJ/m^3*
- Magnetoelectric switching field [1] E_{me} = 2.6 MV/m
- Magnetoelectric exchange bias [1] B_{me} = 9 mT
- Dielectric constant ε_{me}= 13
- Required ME field B_{reqd}= 35 mT (from simulation)
- Required electric field $E_{reqd} = \left(\frac{E_{me}}{B_{me}}\right) B_{reqd}$



simulation set up [2]

(working on a better approach to model exchange bias)

[1] He, Xi, et al., Nature materials 9.7 (2010): 579-585.
[2] Nikonov, D E. et. al., Journal of Materials Research 29.18 (2014): 2109-2115

* assumed for simulation

Georgia Institute of Technology

Modeling approach

Delay calculation

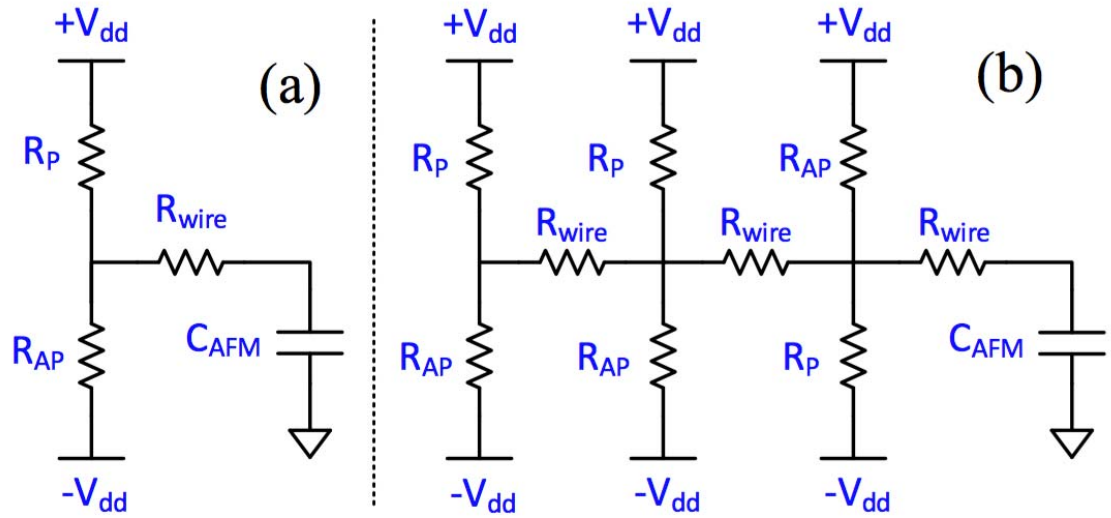
$$t_{\text{int}} = (R_p \| R_{ap} + R_{wire})C_{in} + t_{switch}$$

Energy Calculation

$$E_{\text{int}} = E_e + E_{Leak}$$

where $E_e = \frac{1}{2}(C_{AFM} + 2C_{MTJ})\ V^2$,

$$E_{Leak} = \frac{V_{dd}^2}{R_p + R_{ap}} t_{\text{int}}, \quad V = V_{dd}\frac{R_{ap}\ R_p}{R_{ap} + R_p}$$



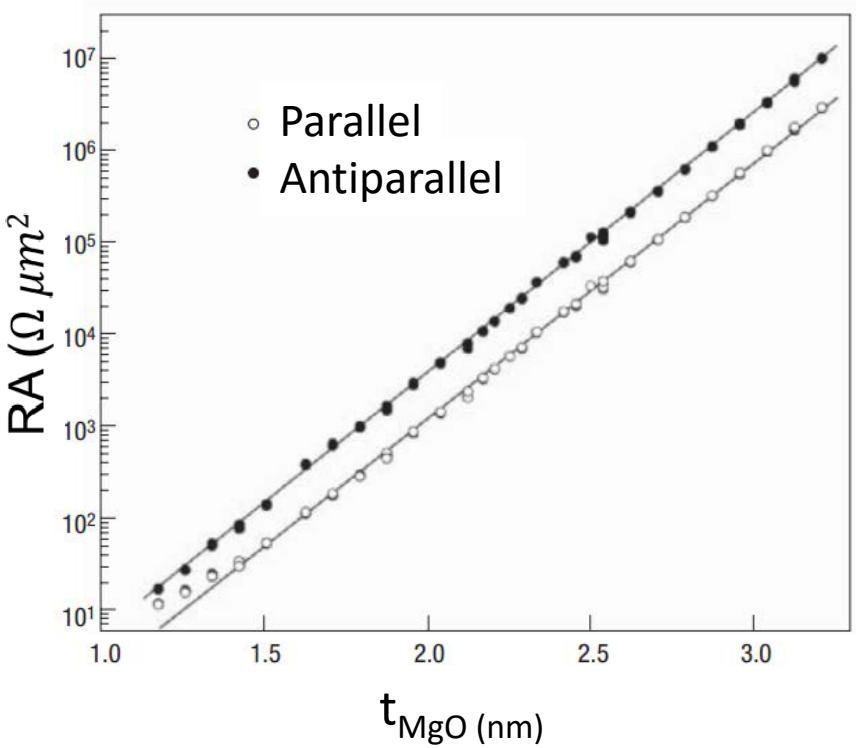
- ❑ High resistance high TMR MJTs are desired
- ❑ Magnet switching time t_{switch} obtained through numerical simulation,

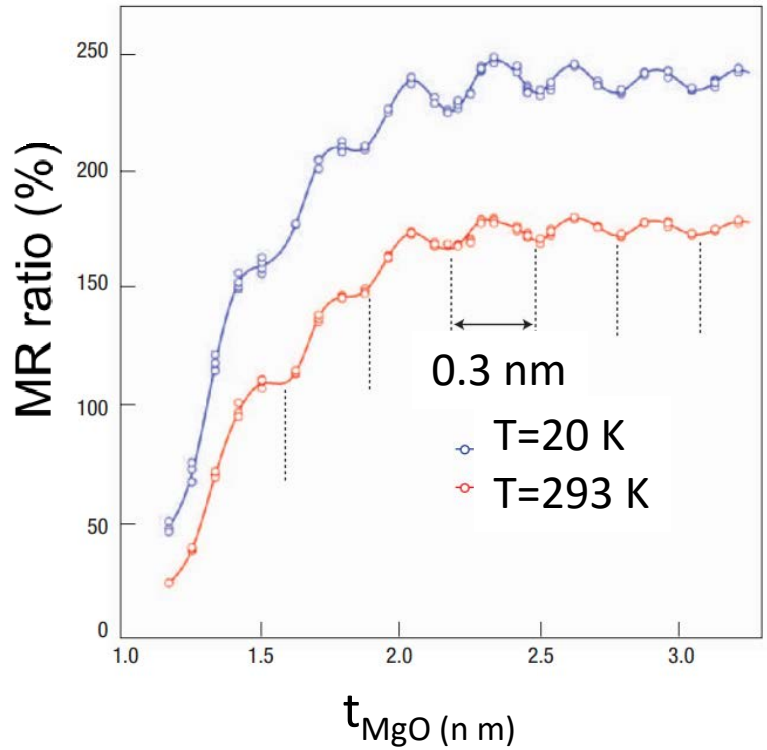
Further ongoing investigation of exchange bias field to obtain more accurate results

Modeling approach

Device Optimization

RA product and TMR vs. tunneling oxide thickness



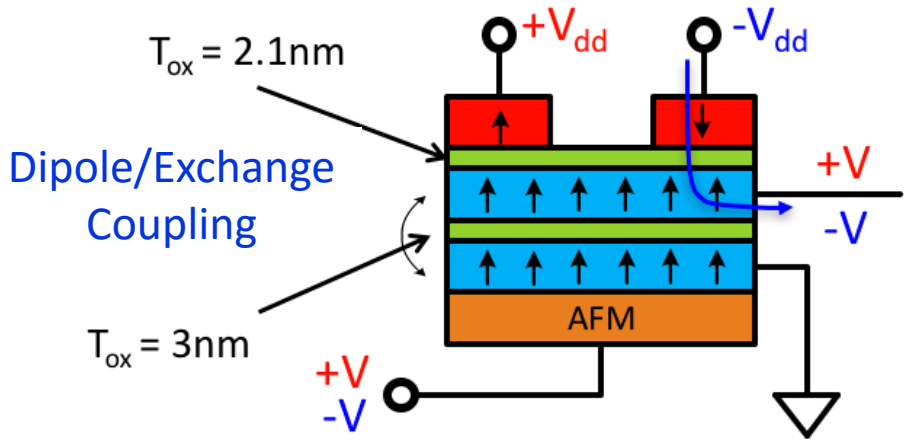


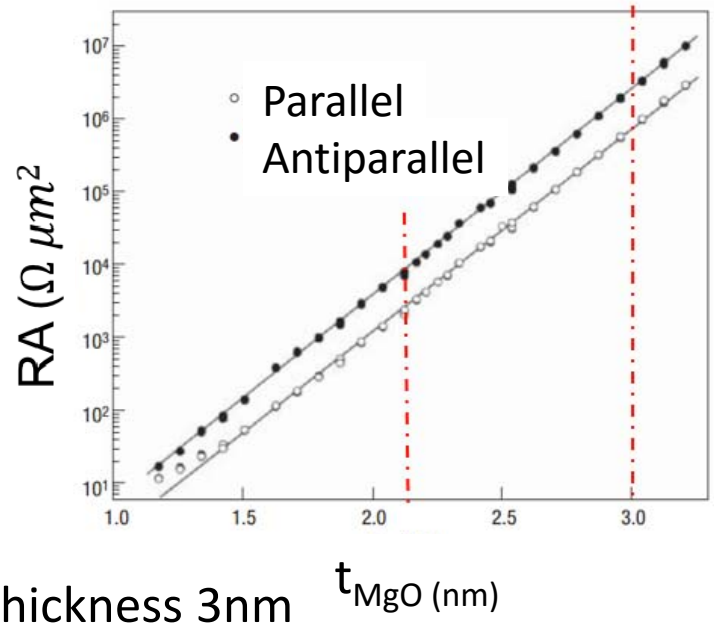
The RA product increases exponentially as the tunneling oxide thickness increases.

Yuasa, Shinji, et al., *Nature materials* 3.12 (2004): 868-871.

Modeling approach

Oxide Thickness Selection

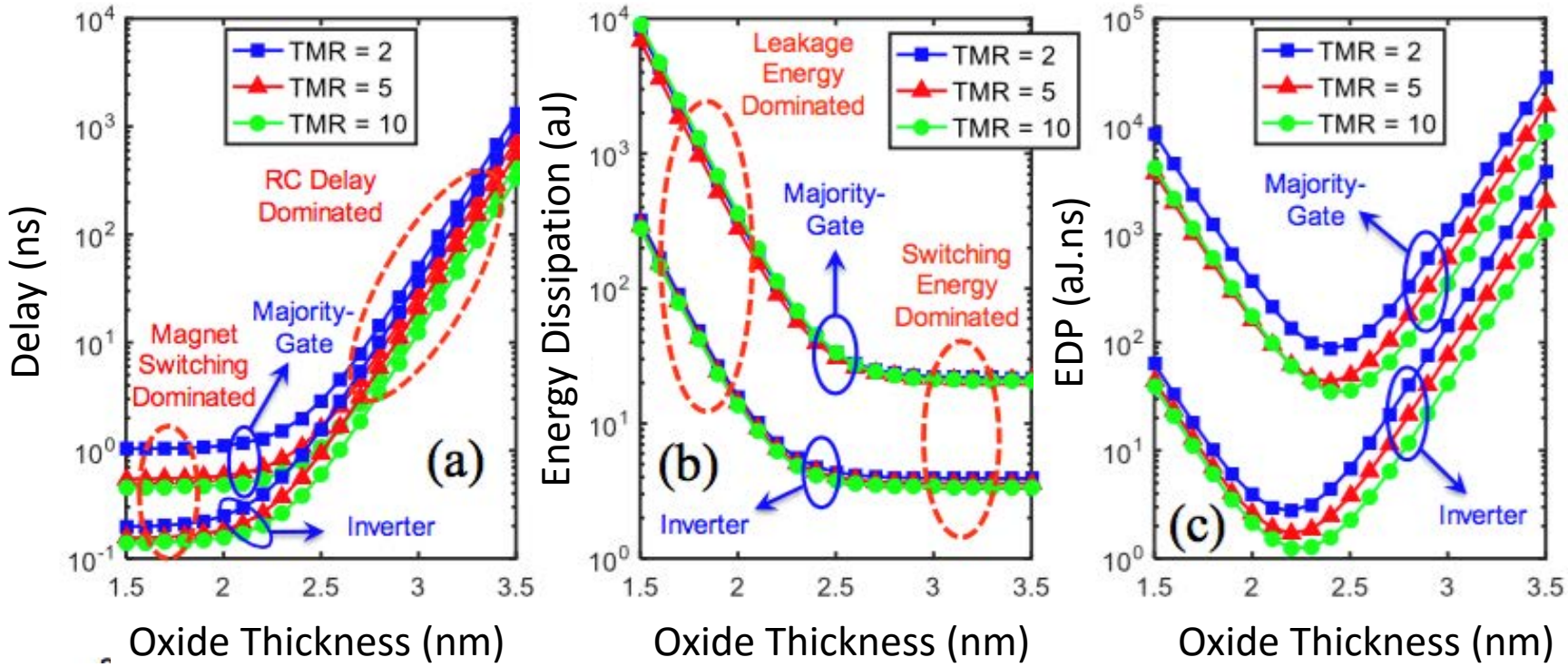




- ❑ MTJ oxide thickness 2.1nm , insulation layer thickness 3nm
- ❑ RA would be ~500X larger between the two free magnets compared to the RA of the MTJs
- ❑ 3nm separation between magnets allows good dipolar coupling.
- ❑ Alternatively, insulating magnet can be used
- ❑ For benchmarking, conservative TMR 200% and optimistic TMR 500% used

Performance analysis

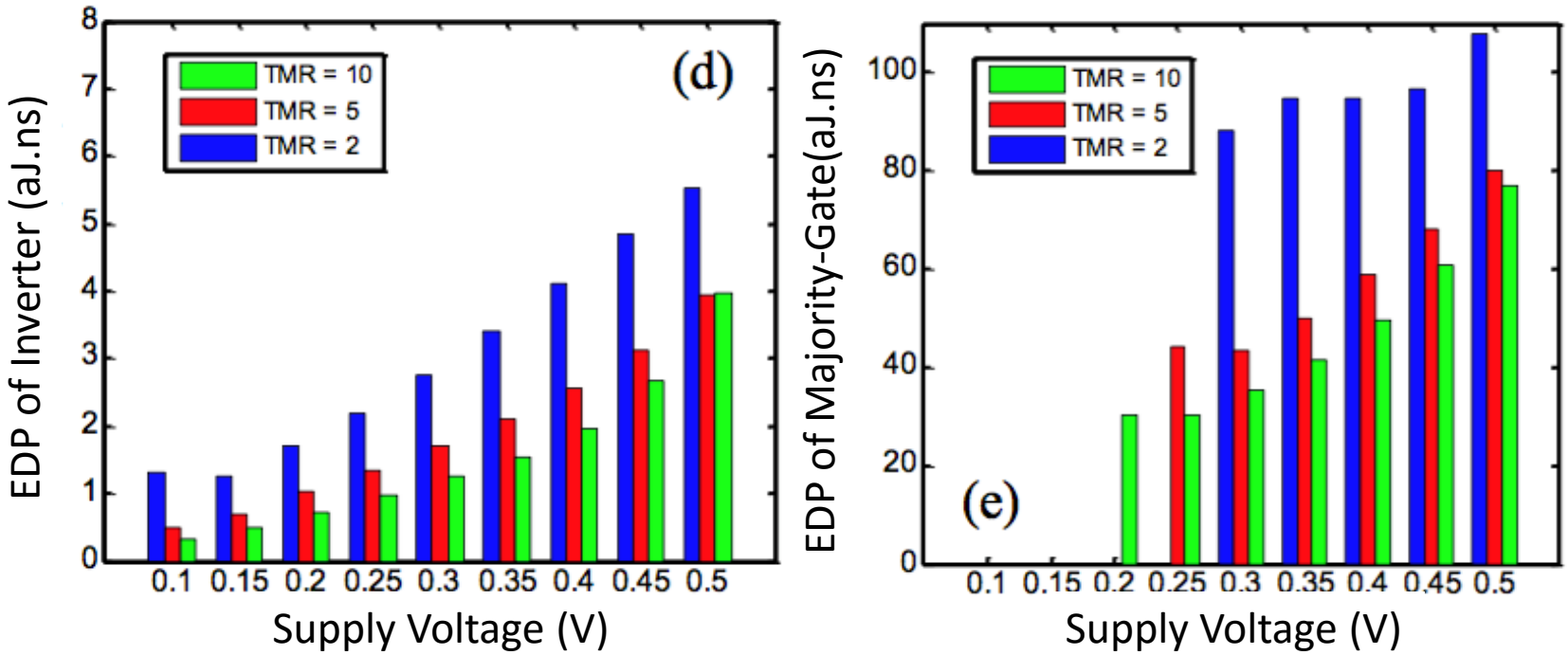
Intrinsic device and majority gate



- Delay is dominated by magnet switching time when t_{ox} is small.
- Energy is dominated by the leakage energy when t_{ox} is small.
- Optimal oxide thickness exists to minimizing the overall EDP

Performance analysis

Intrinsic device and majority gate

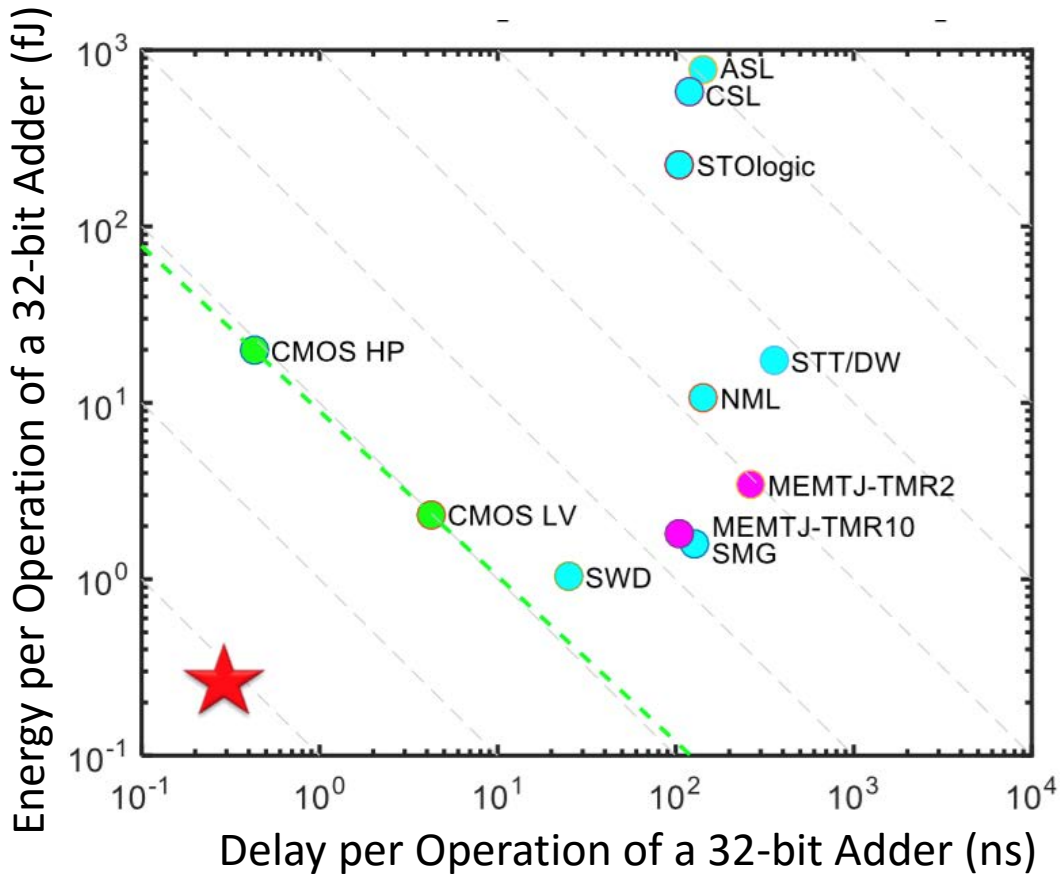


- EDP keeps decreasing with V_{dd} and saturates
- Since output voltage swing of the majority gate is smaller compared to a single inverter, needs higher V_{dd}

Performance analysis

Circuit level analysis

- Voltage controlled devices better than current controlled
- Spin devices are slow due to magnet switching time
- High-TMR MEMTJ provides about 2× improvement in delay and energy dissipation compared to its low-TMR counterpart



Nikonov, D.E., et. al., *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits* 1 (2015): 3-11.

Conclusion

- An concatenable MEMTJ device is proposed that satisfies five essential properties that allow it to be used as a stand-alone logic device
- Two schemes with different fixed magnet magnetization and layout are proposed to address the fabrication challenge.
- Optimal tunneling oxide thickness and supply voltage are found to minimize the overall EDP under different TMR assumptions.
- At the circuit-level analysis, MEMTJ devices are more energy efficient compared to their CMOS counterpart but operate slower due to the larger magnet switching time as well as the RC delay

Tech Transfer

Publications

- Dutta, S., Pan, C., and Naeemi, A., “A Concatenable Magnetoelectric Magnetic Tunneling Junction (MEMTJ) Computational Device”, SRC website

THANK YOU!

Questions?