Scalability of $BaTiO_3$ based ferroelectric tunnel junctions (FTJs)

M. Abuwasib[1], Hyungwoo Lee[2], C. B. Eom[2], A. Gruverman[3], U. Singisetti[1]
[1]Department of Electrical Engineering, University at Buffalo, Buffalo, New York 14260
[2]Materials Science & Engineering, University of Wisconsin-Madison, 1415 Engineering Drive, Madison, WI 53706
[3]Department of Physics & Astronomy, University of Nebraska - Lincoln, NE 68588-0299

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Motivation

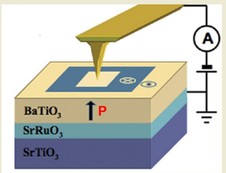


Fig 1. $BaTiO_3$ FTJ with AFM probe[1]

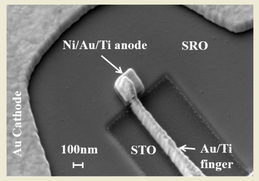


Fig 2. Fully integrated sub-micron FTJ

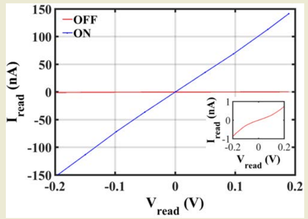


Fig 3. Fully integrated sub-micron FTJ switching

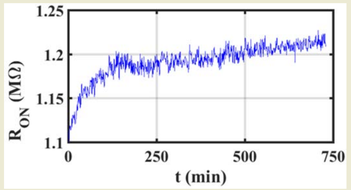


Fig 4. Polarization retention for 300x300nm² FTJ

- $BaTiO_3$ based FTJ operation verified by PFM/AFM[1].
- 300x300 nm² fully integrated FTJ demonstrated.
- Large ON current density J_{ON} (75 A/cm²) and long FE polarization retention (>12h) observed.

Possibility to scale down sub-50nm FTJ to investigate ultimate scaling limit and switching dynamics

[1] A. Gruverman *et al.*, Nano Letter, 9(10), 3539-3543, (2009)

Sub-micron FTJ process challenges

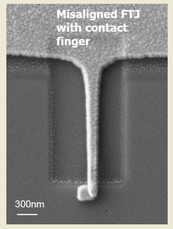


Fig 5. Critical for sub-100nm FTJ alignment

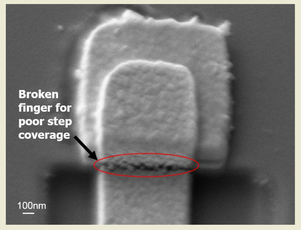
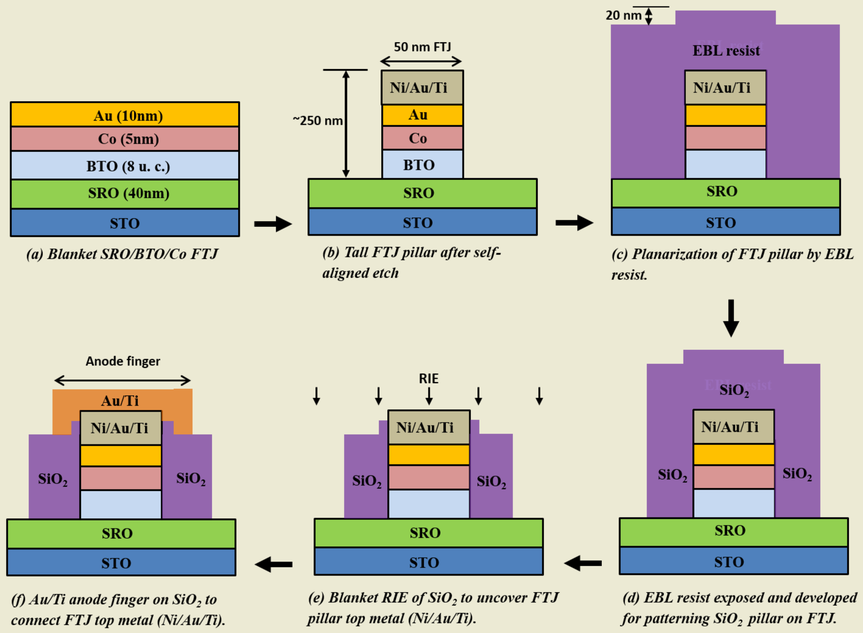


Fig 6. Poor sidewall step coverage

- Alignment is critical below 100nm.
- FIB ion-milling is difficult→ damages FTJ.
- Sidewall metallization difficult→ poor yields.

Fully integrated sub-50nm FTJ process required to overcome these challenges.

Sub-50nm FTJ process flow



(a) Blanket SRO/BTO/Co FTJ

(b) Tall FTJ pillar after self-aligned etch

(c) Planarization of FTJ pillar by EBL resist.

(d) EBL resist exposed and developed for patterning SiO_2 pillar on FTJ.

(e) Blanket RIE of SiO_2 to uncover FTJ pillar top metal (Ni/Au/Ti).

(f) Au/Ti anode finger on SiO_2 to connect FTJ top metal (Ni/Au/Ti).

Fig 7. Sub-50nm FTJ process

Sub-50nm FTJ planarization process

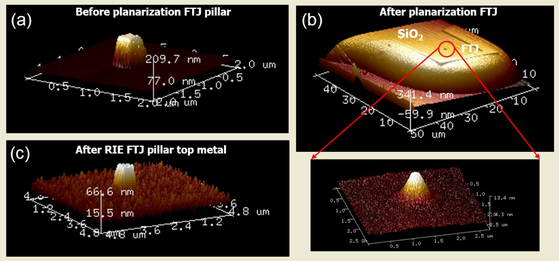


Fig 8. Sub-50nm FTJ planarization process

- FTJ pillar (h~200nm) planerized by EBL resist
- FTJ bump height is ~15nm
- Etching back SiO_2 by RIE opens FTJ top metal

Conclusion and Future works

- Demonstrated Sub-micron process challenges for FTJ fabrication
- Sub-50nm fully integrate FTJ process demonstrated
- Sub-50nm FTJ device fabricated and tested
- High speed and RF measurements will be performed in future

Sub-50nm FTJ fabrication

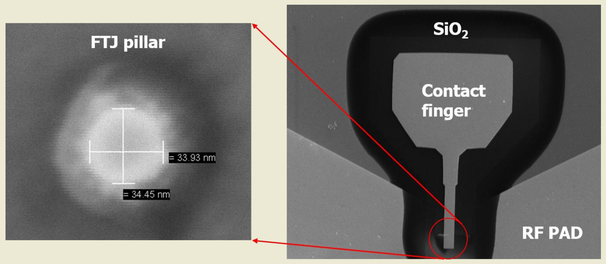


Fig 9. SEM images fully integrated Sub-50nm FTJ

- JEOL JBX 6300 EBL used for FTJ fabrication
- Minimum FTJ size 30 x 30 nm²
- FTJ pillar height ~200nm

Sub-50nm FTJ process yield

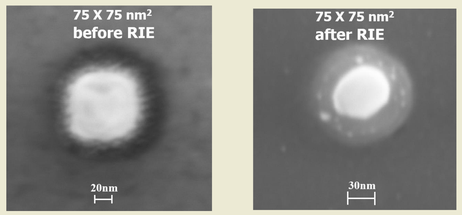


Fig 10. RIE damages Sub-50nm FTJ sidewall

- RIE undercuts FTJ→ size reduction
- RIE damages→ FTJ sidewall

I-V measurement of FTJ

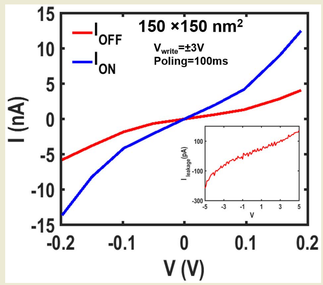


Fig 11. I-V of 150x150nm² FTJ

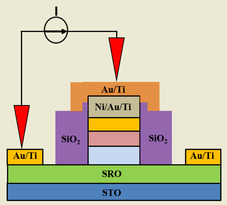


Fig 12. Crossection of measured FTJ

- Sub-50nm FTJ process was used
- Switching observed for 150x150 nm² FTJ
- Leakage through 400nm SiO_2 $I_{leakage}$ (100pA)
- $I_{leakage} << I_{OFF}$(5nA)