Why do we need novel steep transistors?

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Motivation Statement and Key Result Statement

Theme 2383.002 :
Quantum Engineered Steep Transistor

Task D.2.4:
Atomistic Carrier Transport Modeling for Steep Devices

Device/Collaboration:
TFETs based on 2D materials.

Motivation Statement:
2D materials have specific properties which can be used to solve TFETs' challenges: 1) sub 10nm dimension scaling, and 2) low ON-current.

Key Result Statement:
Novel TFET designs are proposed and shown to solve the above mentioned challenges based on the state-of-the-art atomistic quantum transport simulations.

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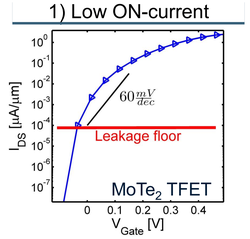
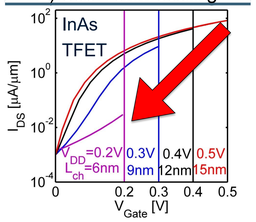
Main challenges of TFETs

1) Low ON-current



2) Sub-10nm scaling



Low I_{ON} → Low performance
→ Leakage floor hides steep part of I-V

L_{ch}↓ + V_{DD}↓ → I_{ON} ↓
→ I_{OFF} ↑
→ I_{ON}/I_{OFF} ↓

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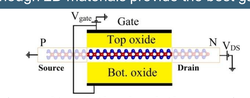
2D material TFETs for I_{ON} challenge

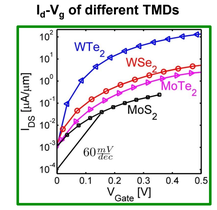
Although 2D materials provide the best gate control, depletion width avoids High I_{ON}



Key messages:
- Thin channel is **NOT** enough for high I_{ON}
- Depletion width at source is limiting I_{ON}.

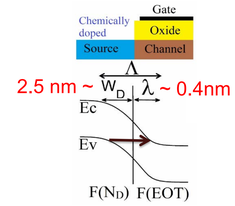
Atomistic simulation

I_d-V_g of different TMDs



N_D = 1e20 cm^{-3} V_{dd} = 0.5V
EOT = 0.5nm L_{ch} = 15nm

Analysis



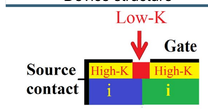
W_D is limiting factor [5,7]

I_{ON} challenge: Dielectric engineered TFET (DE-TFET)

How to increase E-field and decrease the tunneling distance in 2D TFETs?

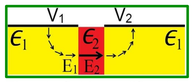
Answer: Dielectric engineering

Device structure



- Combination of low-k & high-k
- Low-k is usually air gap

Idea



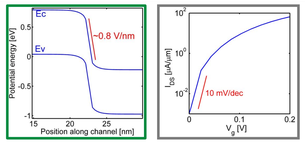
Electric field amplification

$$\epsilon_1 E_1 = \epsilon_2 E_2$$

$$\epsilon_2 \ll \epsilon_1 \rightarrow E_2 \gg E_1$$

Atomistic simulation

Vdd = 0.2V



- Monolayer WTe_2 channel
- Low-k = air gap
- High-k = HfO_2
- L_{ch} = 12nm

DE-TFET Challenges

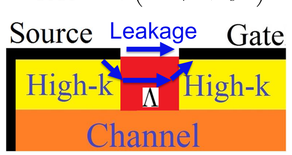
How to reduce the leakage between contacts?

Answer: Wokfunction engineering of contacts

Small spacing btw. contacts

Small Λ → high transmission

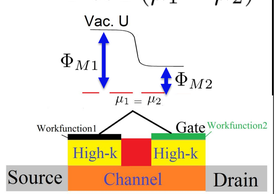
$$T_{BTBT} = exp\left(-C\sqrt{m_t^* E_g}\,\Lambda\right)$$



Solution

Landauer formula

$$I \propto T(\mu_1 - \mu_2)$$



Shorting 2 different metals on top → No leakage current
→ No parasitic capacitance

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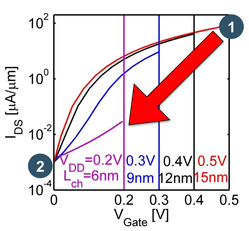
2nd Challenge: Channel length scaling beyond 10nm

Scaling challenge

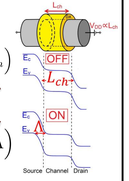


Scaling consequences

1. V_{DD} ↓→Tunneling energy window ↓→I_{ON}↓
2. L_{ch} ↓ → I_{ON}/I_{OFF} ↓↓

$$T_{OFF} = exp\left(-C\sqrt{m_t^* E_g}\,L_{ch}\right)$$

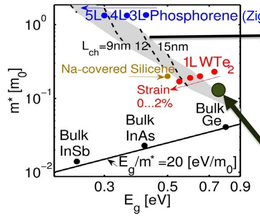
$$T_{ON} = exp\left(-C\sqrt{m_t^* E_g}\,\Lambda\right)$$



Scaling L_{ch} → L_{ch} ~ Λ → I_{ON} / I_{OFF} ↓

Best material choice for short channel TFETs

Best channel materials for TFET applications:
1) Low E_g ~ 1.2 V_{DD}
2) High m*



Shaded region: I_{ON}/I_{OFF} > 10^5

2L Phosphorene (armchair)

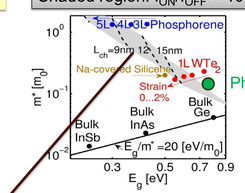
2D materials outperform III-V TFETs in sub 10nm channel lengths.

Best material choice for short channel TFETs

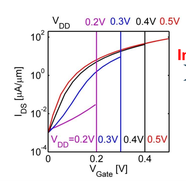
The solution of the scaling problem:

L_{ch}↓ V_{dd}↓ → E_g↓ Opt: $1.2qV_{DD}[eV]$; m*↑ Opt

Shaded region: I_{ON}/I_{OFF} > 10^5

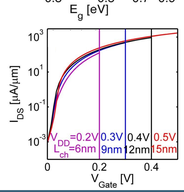


Some 2D materials have required material properties for sub-10 nm TFETs.



InAs

Optimum material for each node



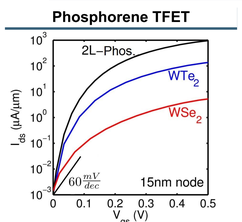
Different channel material is required for different technology nodes of TFETs

Phosphorene TFET

Bilayer Phosphorene is ideal for TFET application

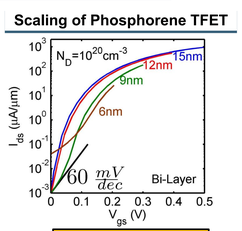
E_g of Bilayer Phosphorene ~ 0.8 eV = 1.3 V_{DD}

Phosphorene TFET



Phosphorene outperforms TMD TFETs → a proper bandgap

Scaling of Phosphorene TFET



Scales well for L_{ch} > 6nm

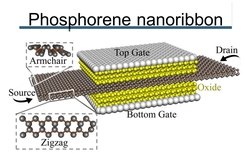
[8] SCIENTIFIC REPORTS — Few-layer Phosphorene: An Ideal 2D Material For Tunnel Transistors

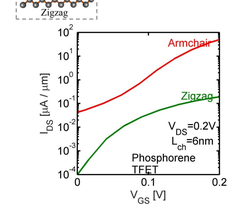
L-shaped phosphorene TFET

How to use anisotropic effective mass of phosphorene to scale below 10nm?

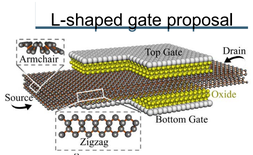
Answer: L-shaped gate

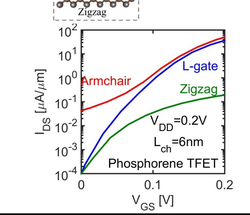
Phosphorene nanoribbon





L-shaped gate proposal





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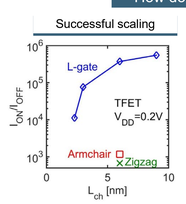
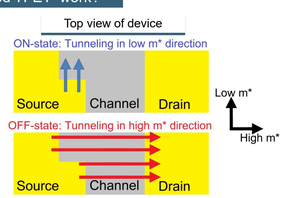
L-shaped phosphorene TFET

How does L-shaped TFET work?

Successful scaling



Top view of device



$$T_{ON} = exp\left(-C\sqrt{m_t^* E_g}\,\Lambda\right)$$

$$T_{OFF} = exp\left(-C\sqrt{m_t^* E_g}\,L_{ch}\right)$$

1) Low m* for high I_{ON}
2) High m* for low I_{OFF}

Using a material with anisotropic m* and L-shaped gate have benefits of
•High I_{ON} / I_{OFF}

[1] SCIENTIFIC REPORTS

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Future works

Next steps:
1) Model and study the impact of trap and dopant states on the transport properties of 2D TFETs.
2) Consider experimental non-idealities such as Schottky contacts and compare the simulation results with experiments.

[1] H. Ilatikhameneh et al., "Saving Moore's Law Down To 1nm Channels with Anisotropic Effective Mass" Scientific reports. (Publication ID: P087463)

[2] H. Ilatikhameneh et al., *"Dielectric engineered tunnel field-effect transistor"* IEEE Electron Device Letters, vol. 36, no. 10, pp. 1097-1100 (2015), (Publication ID: P084698)

[3] H. Ilatikhameneh et al., *"Design Rules for High Performance Tunnel Transistors from 2D Materials,"* IEEE JEDS DOI 10.1109/JEDS.2016.2568219 (Publication ID: P084699).

[4] H. Ilatikhameneh et al., "*Scaling Theory of Electrically Doped 2D Transistors,*" IEEE Electron Device Letters, vol. 36, no. 7, pp. 726-728 (2015), (Publication ID: P073786).

[5] H. Ilatikhameneh et al., "*Tunnel Field-Effect Transistors in 2D Transition Metal Dichalcogenide Materials,*" IEEE JXCDC 2015 (P073163).

[6] H. Ilatikhameneh et al., "*2D Tunnel Transistors for Ultra-Low Power Applications: Promises and Challenges*" E3S Berkeley Symposium (P084660).

[7] R. Salazar, H. Ilatikhameneh et al., "*A New Compact Model For High-Performance Tunneling-Field Effect Transistors*" JAP 2016 (P084669).

[8] T. Ameen, H. Ilatikhameneh et al. *"Few-layer Phosphorene: An Ideal 2D Material for Tunnel Transistors"* Scientific reports 1 (2016), (Publication ID: P086553).

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