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Chip Level Materials: Challenges and Potential Solution Paths

Solid State Technology Webinar
November 13, 2014

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SRC Established in 1982 by Visionary Industry Leaders

Objectives:

- ✓ Define relevant research directions
- ✓ Explore potentially important new technologies
- ✓ Generate a pool of experienced faculty & relevantly educated students

Erich Bloch

Robert Noyce

Jack Kilby

Semiconductor Research Corporation Research Portfolio: A Family of Uniquely Relevant Programs

Global Research Collaboration

Ensuring vitality of current industry

AMAT
AMD
Mubadala Tech
Freescale
GLOBAL-FOUNDRIES
IBM
Intel
Mentor Graphics
ON Semi
Qualcomm
RTI International
TEL
TI

Gov't Participants
State of Arizona
State of Texas
State of NY
NIST
NSF

Other Participants
SEMI
SIA
MOSIS

STARnet

Focus Center Research Program Phase VI

STARnet

Early research engagement of key long horizon semiconductor challenges

AMAT
GLOBALFOUNDRIES
IBM
Intel
Micron
Raytheon
TI
United Technologies

Government Participant
DARPA

Nanoelectronics Research Initiative

Beyond CMOS – the next switch and associated architectures

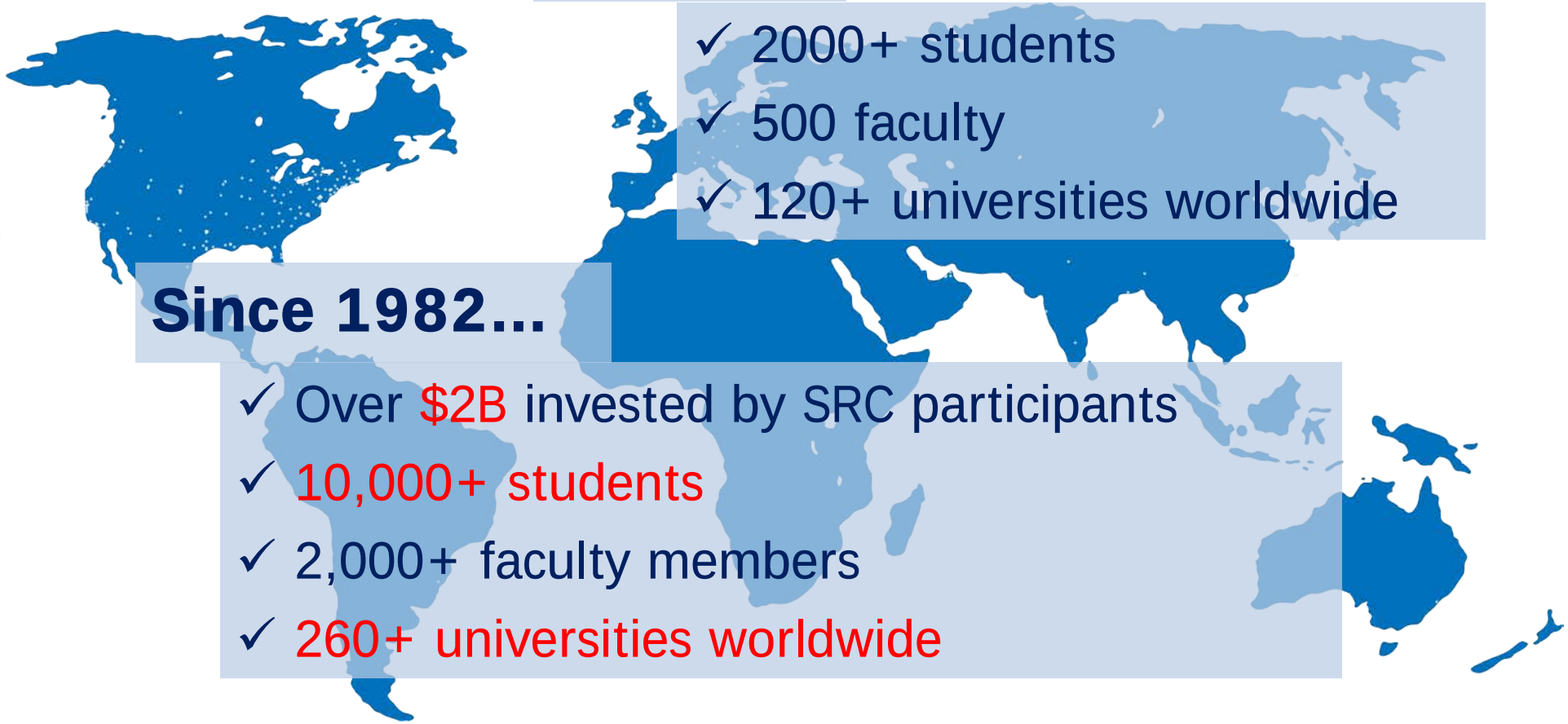
GLOBAL-FOUNDRIES
IBM
Intel
Micron
TI

Gov't Participants
NIST
NSF
State of Indiana
State of Nebraska
State of NY
State of Texas

Education Alliance

Attracting and educating the next generation of innovators and technology leaders

SRC created an industry-guided global university research ecosystem



In 2013…

- ✓ 2000+ students
- ✓ 500 faculty
- ✓ 120+ universities worldwide

Since 1982…

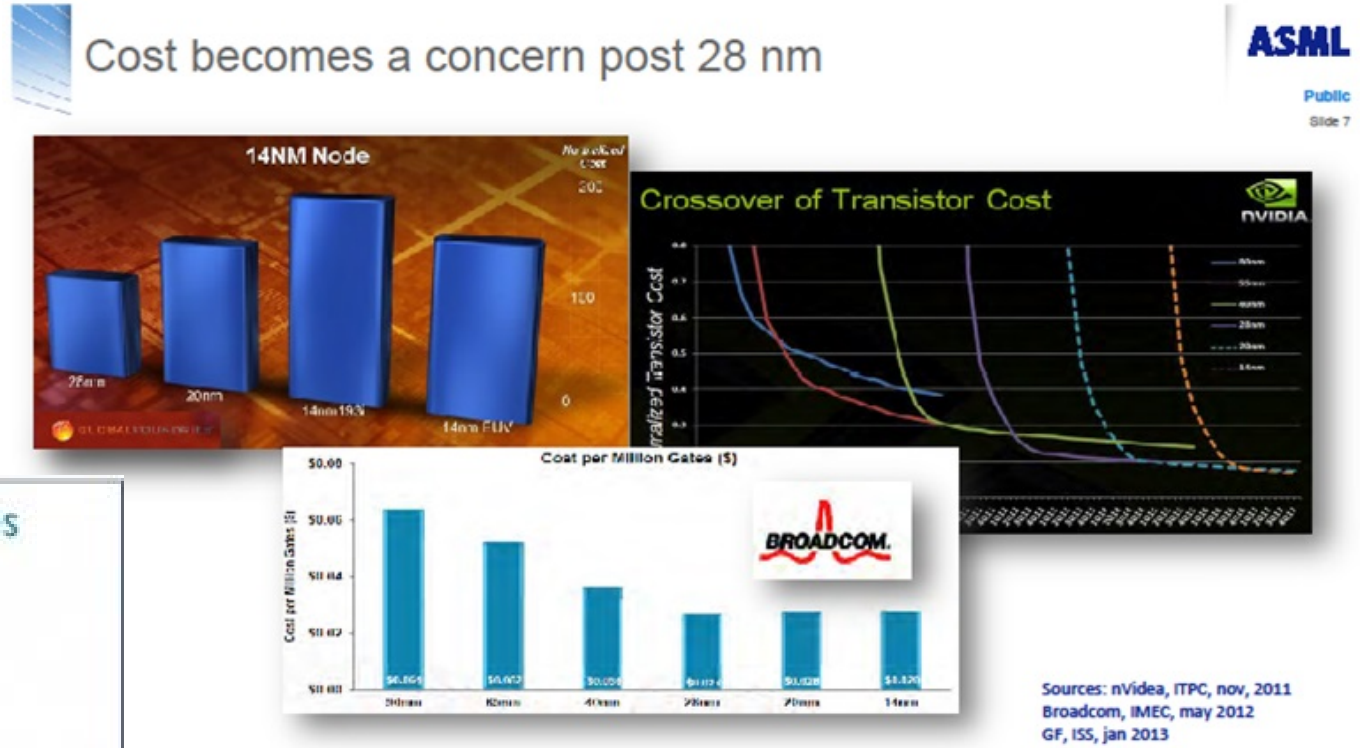
- ✓ Over $2B invested by SRC participants
- ✓ 10,000+ students
- ✓ 2,000+ faculty members
- ✓ 260+ universities worldwide

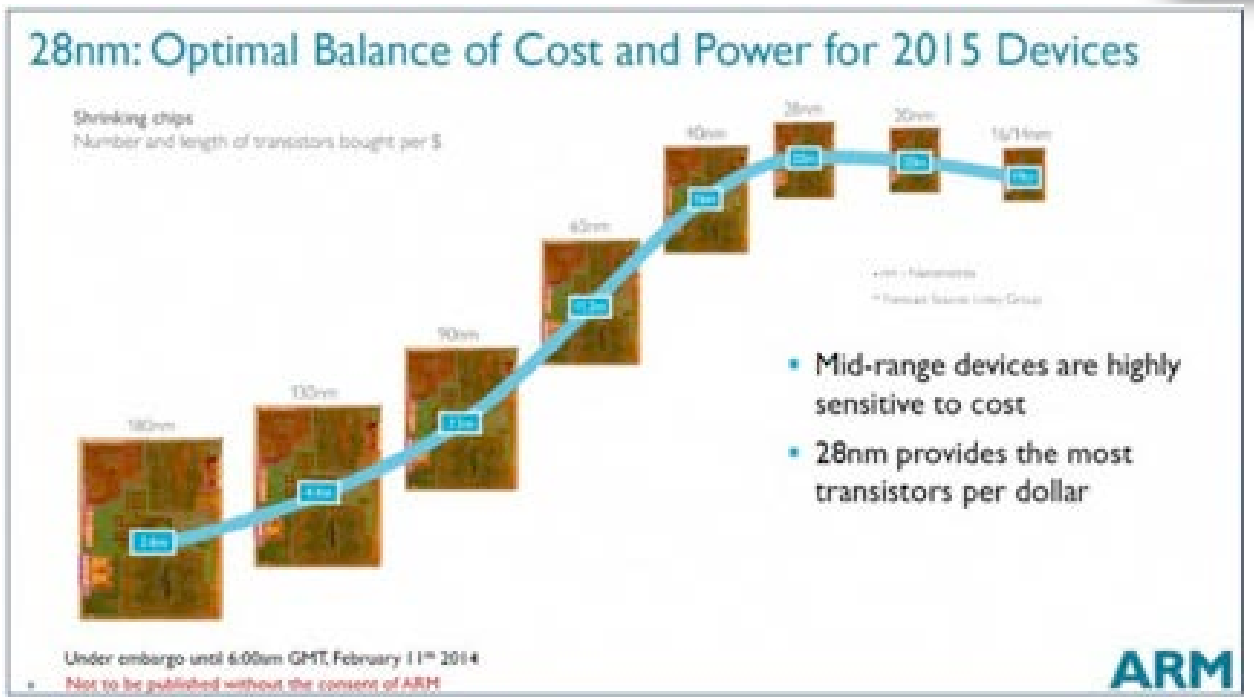
Outline

- **‘The Crisis’**
- **Device Materials Needs**
- **Lithography Challenges**
- **Interconnect Materials Issues**
- **Summary**

The Crisis – from economics perspective

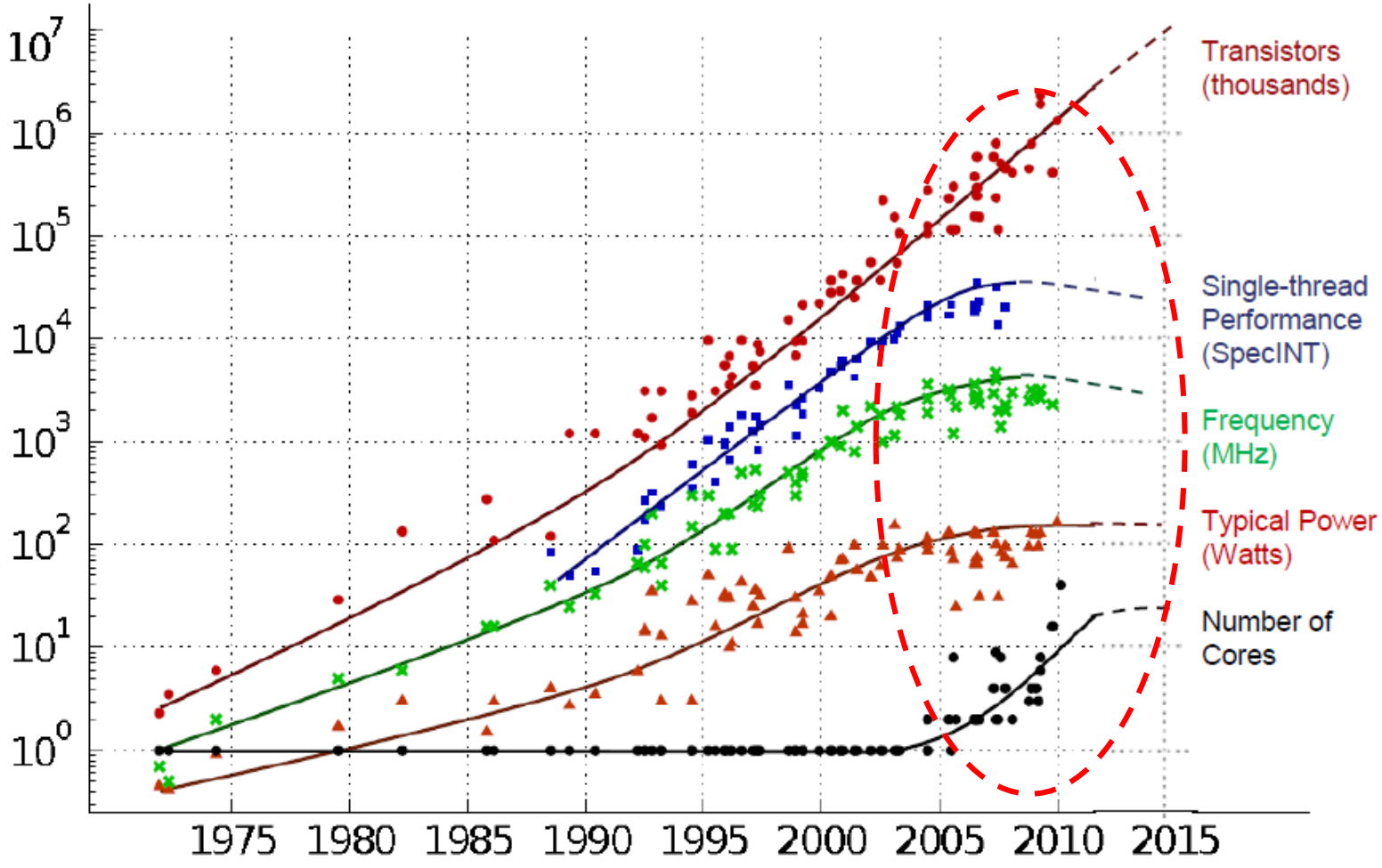
End of Moore's Law?





Cost per transistor plateau!

The Crisis – from performance perspective



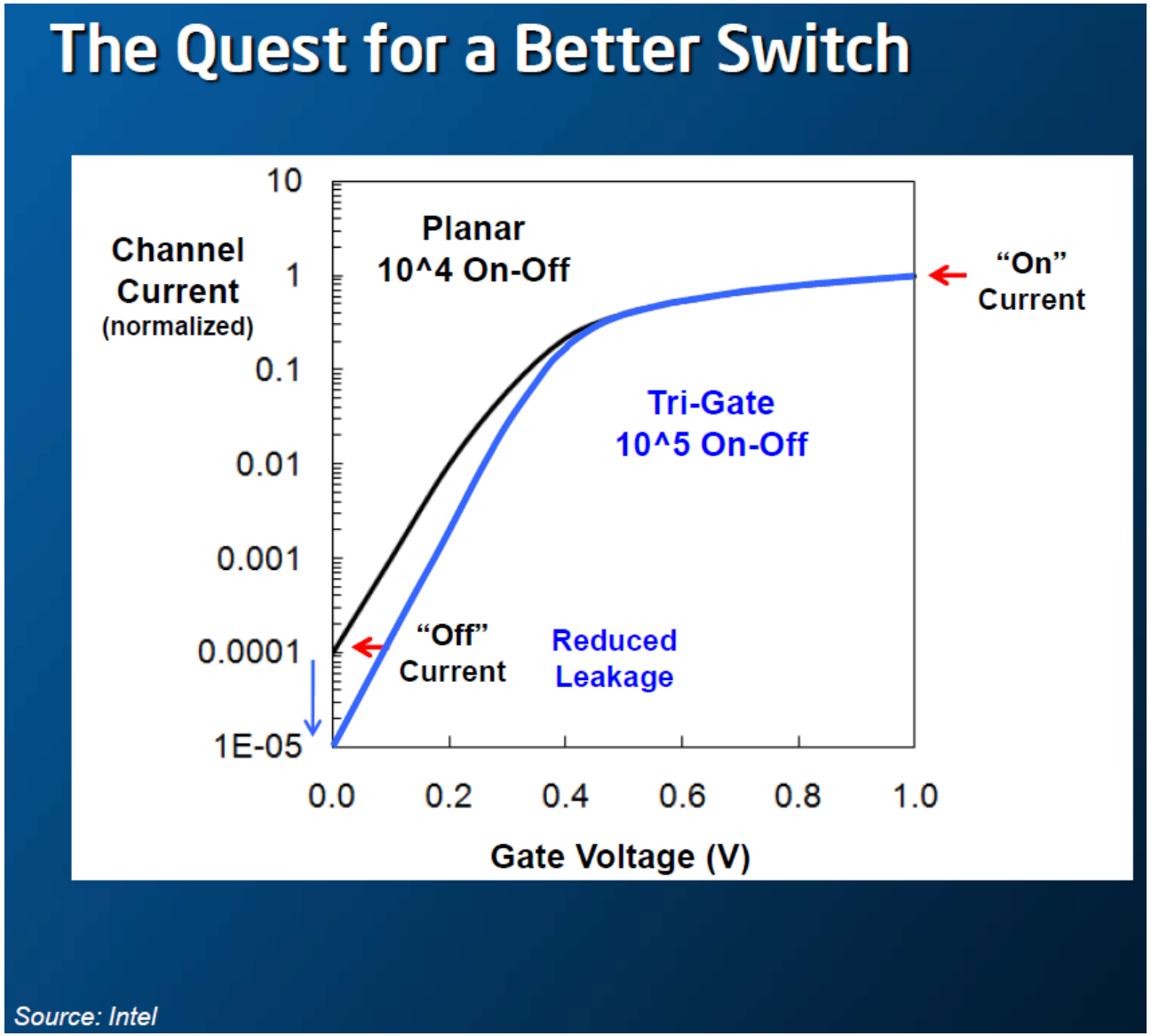
Original data collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond and C. Batten
Dotted line extrapolations by C. Moore

Device Challenges

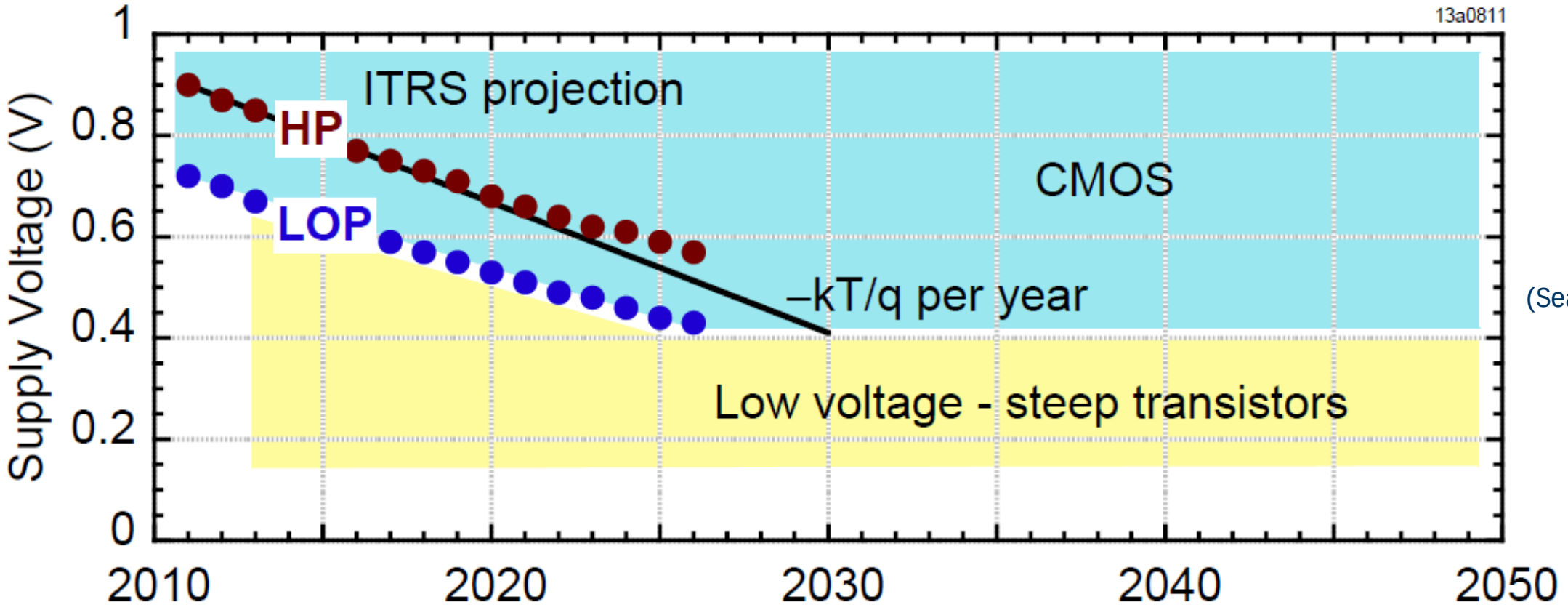
- We are entering the era of diminishing returns for physical device scaling ('Moore's Law')
  - Chip areas **limited by interconnects** (bond pads, wiring density, vias, repeaters)
  - **Power density** limited due to thermal issues
  - Minimum device **contact area** requirements
  - 'Running out of atoms'
    - Mostly a **control / yield** issue at this point
  - **Cost per transistor** scaling ending

- We are deep in to the era of energy-limited performance
  - Not able to utilize all transistors at the same time due to overheating ('dark silicon')
  - **Need to scale Voltages** to further reduce dynamic energy
    - Multicore designs saved energy by reducing the need for frequency scaling
    - Number of cores now limited by software capabilities as well as on-chip routing
  - **Need to limit device leakage** to minimize static energy
    - Most devices typically 'off' (see 1st sub-bullet above)

Device Challenges - performance



Device Challenges - performance

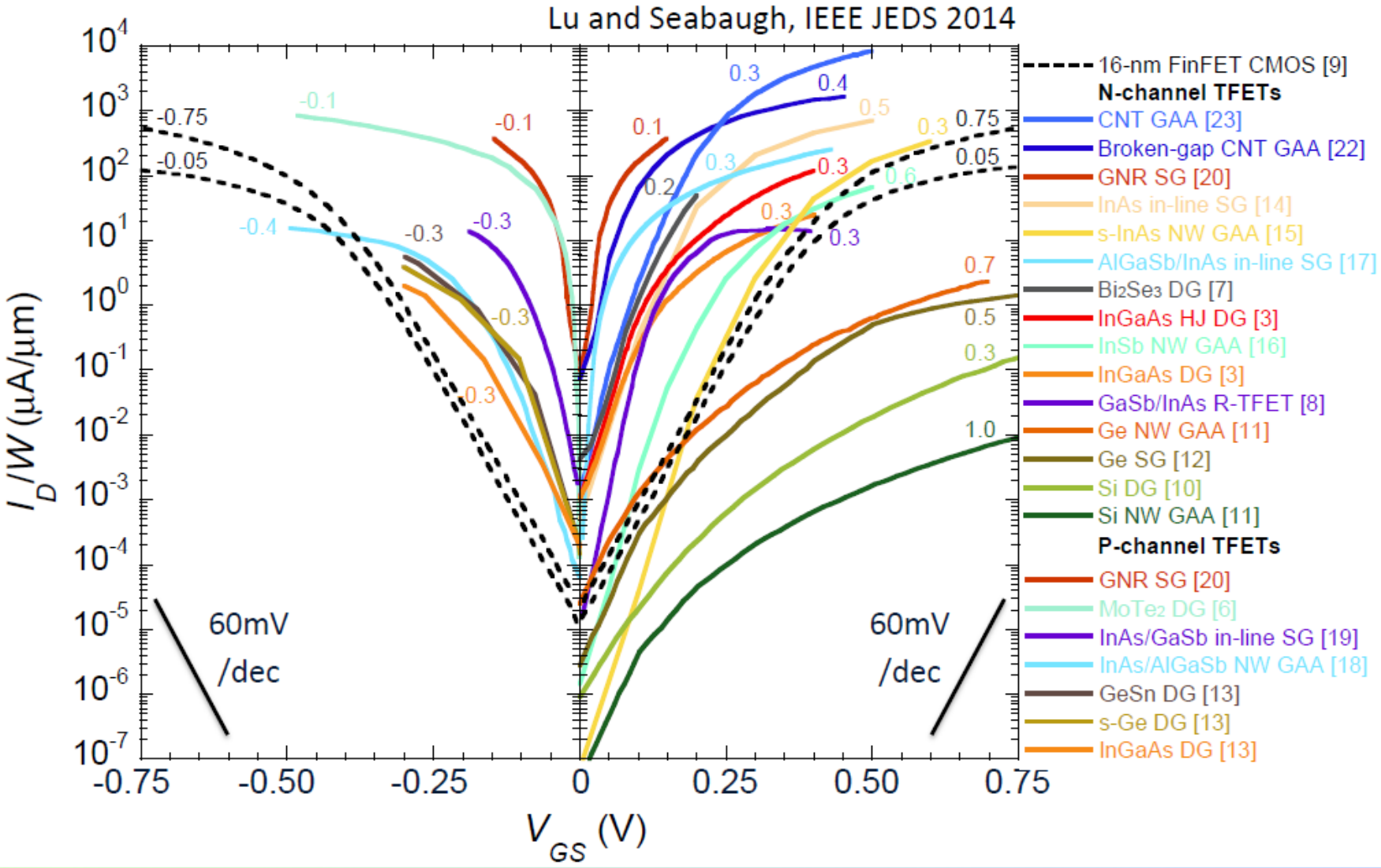


(Seabaugh, et al)

In order to lower supply voltages and maintain performance,
FETs have to turn off sharper without decreasing drive current – steeper sub-threshold slope

Device Challenges - performance

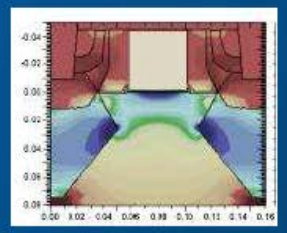
Tunnel FET state-of-the-art - simulations



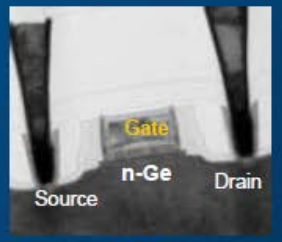
Device Challenges - performance

We Need Both New Materials & New Structures

Increasing Mobility



Strain

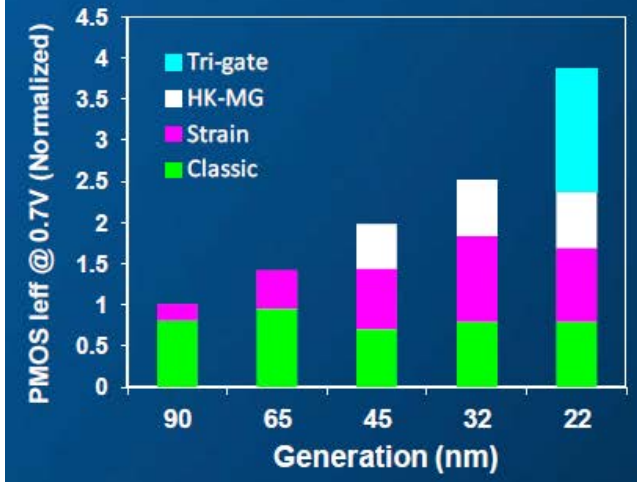


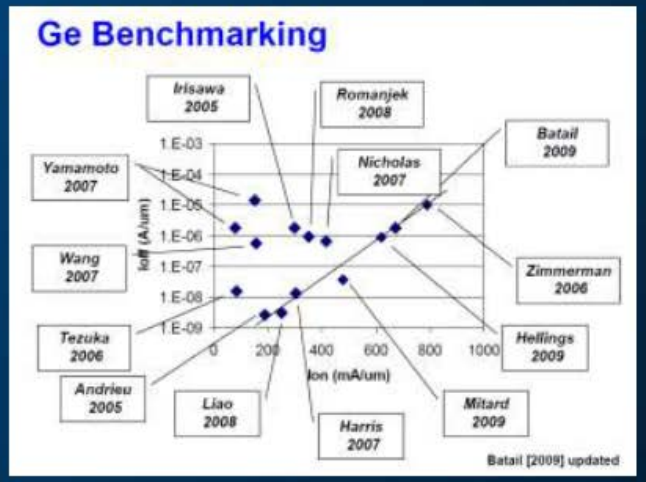
Ge

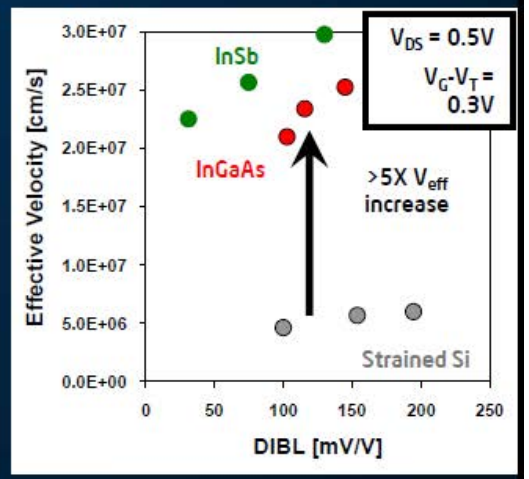
III-V

CNT

Graphene

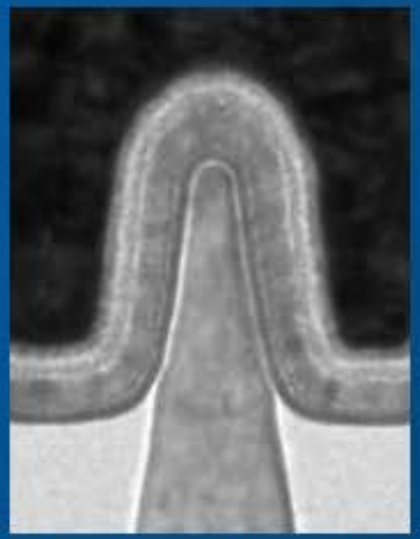






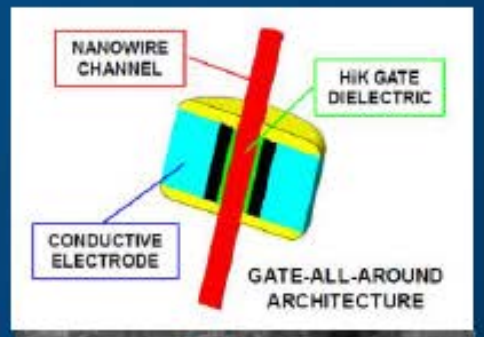
Source: Intel

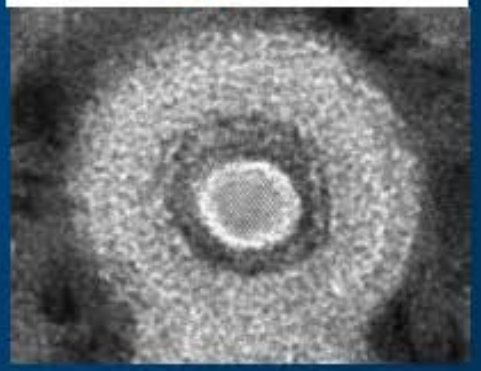
Device Challenges - control



Production 22nm Tri-Gate Transistors

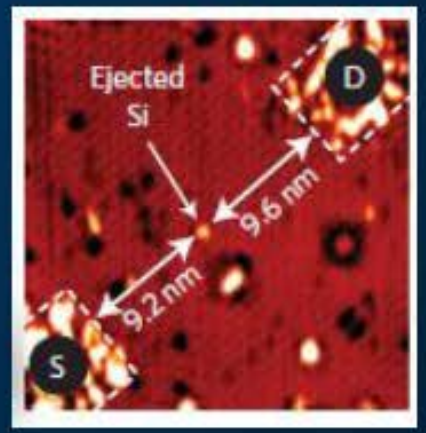
~400,000 atoms





Nanowire Transistors

~40,000 atoms



Single Atom Transistors

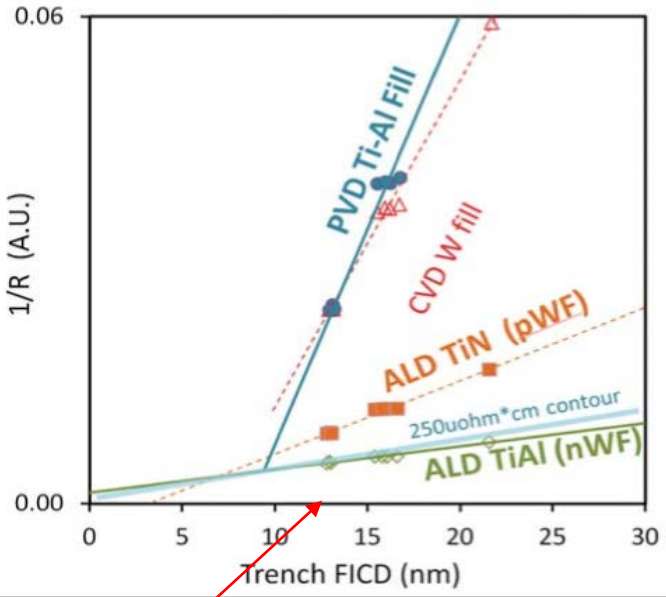
1 atom

Martin Fuechsle et al., Nature Nanotechnology, Feb. 19, 2012

Source: Intel

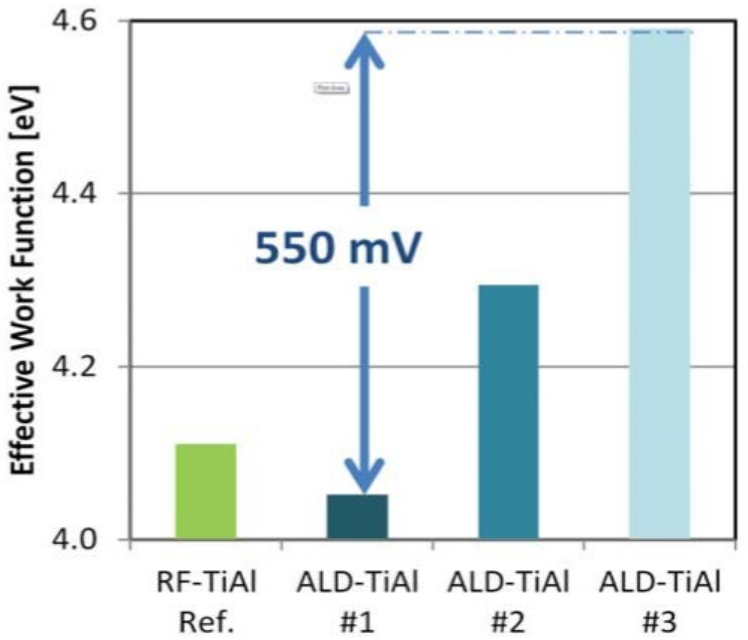
Emerging Device Material Solutions – gate metals

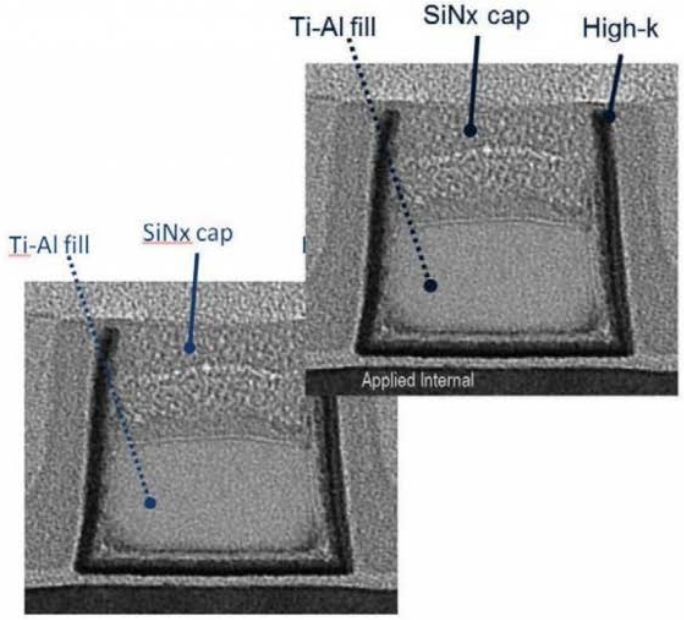
Conductance Curves for Various Transistor Gate Metal Processes down to 13 nm Gaps* without voiding



* **Projected 7 nm node requirement**

Work function & Threshold Voltage Tuning using Metal Gate Composition





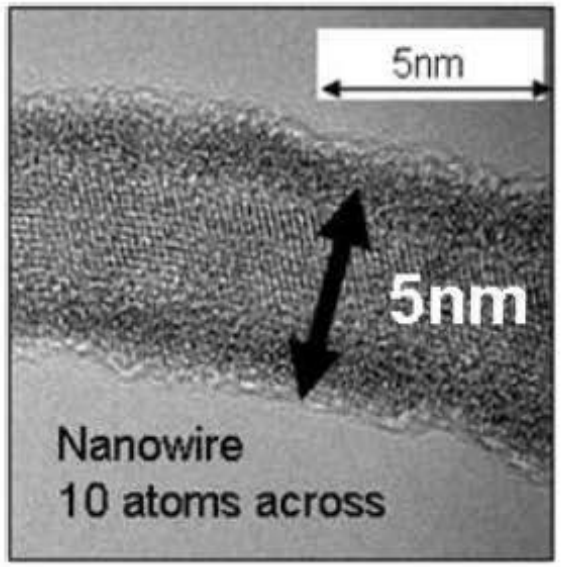
ALD TiAl self-aligned metal gate fill

(all from Applied Materials, Inc.)

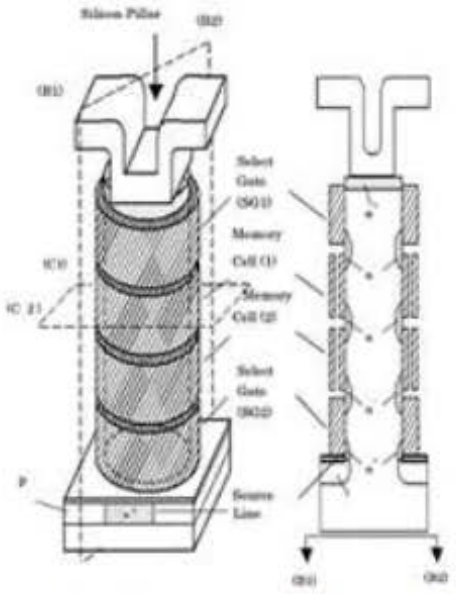
Emerging Device Material Solutions – nanowire FETs

Are there fundamental physical limits?

Source: Intel

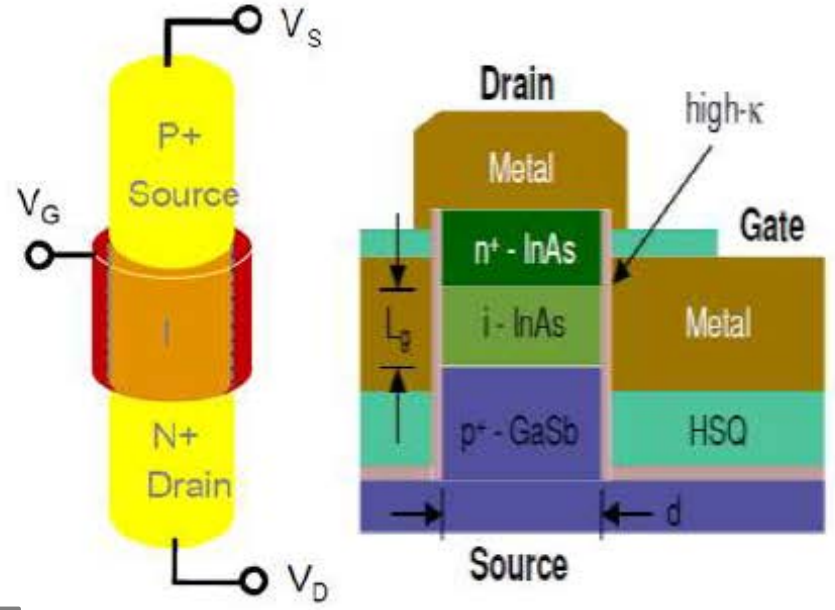


5nm device feature



Source: Endoh, TED 2003

Vertical Memory Cell



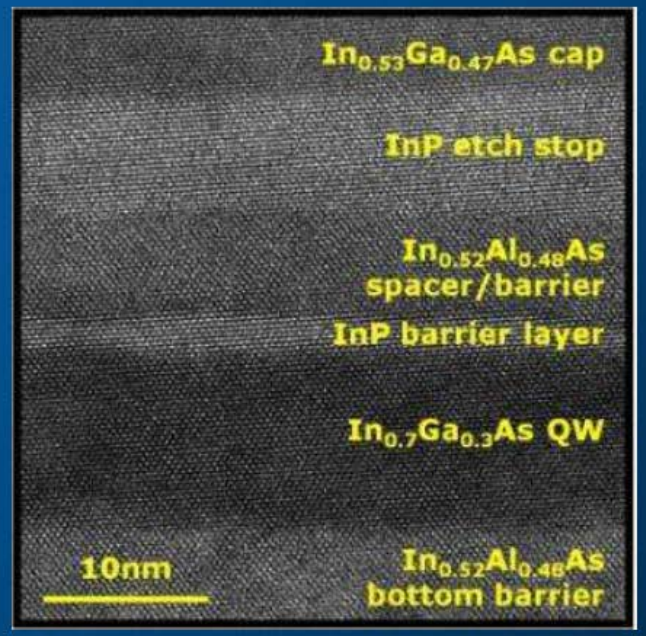
III-V Vertical Tunnel FETs

Vertical device structures and new materials

Device Roadmap – from structures to materials

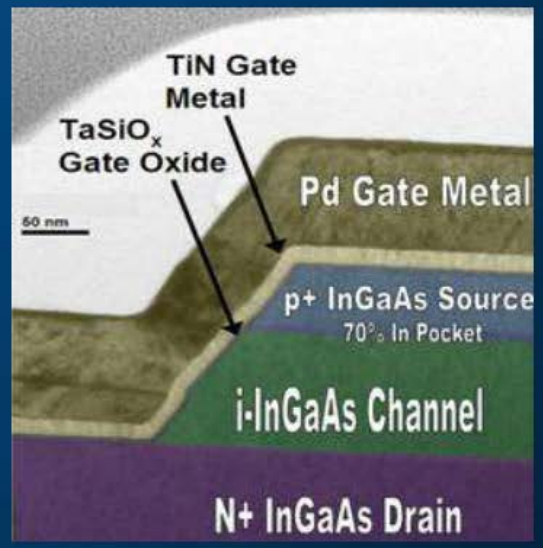
Fabrication of TFET

Source: Intel

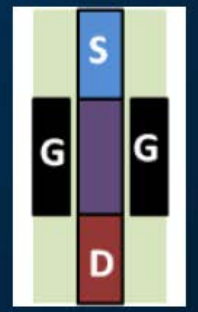


Radosavljevic et al. IEDM 2009
Dewey et al. IEDM 2011

What we can make



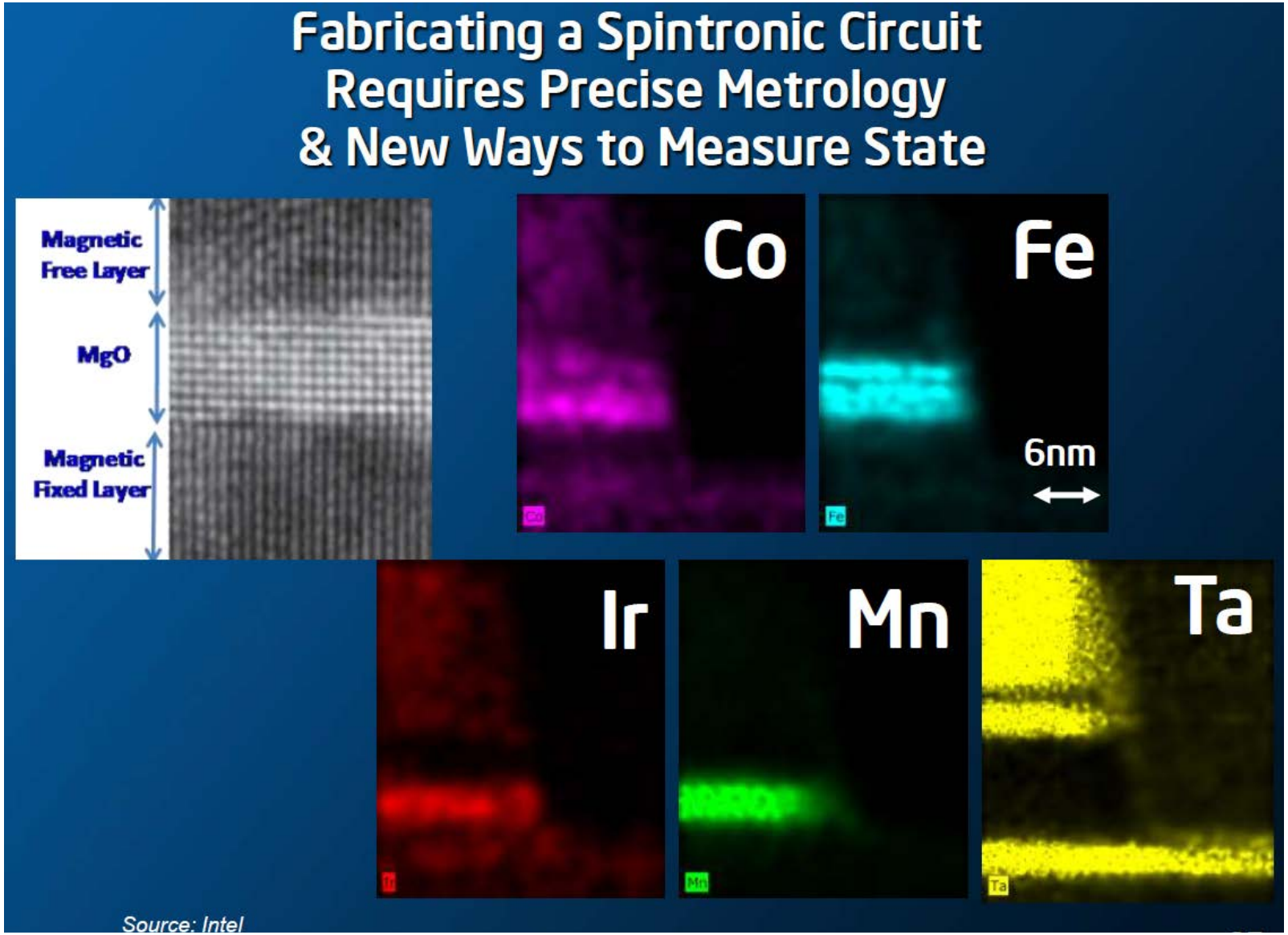
What we need to make



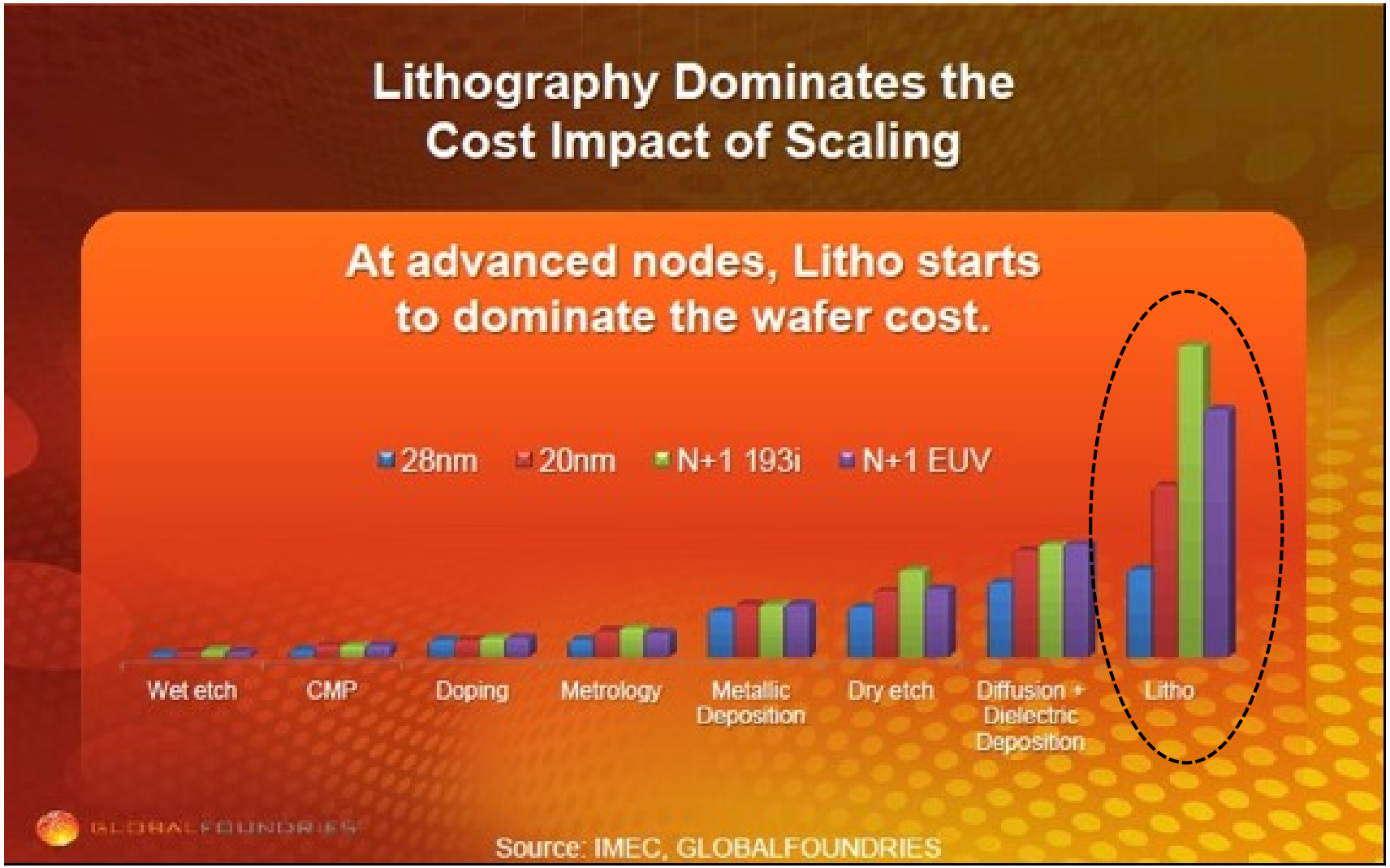
Fabrication challenges

- Multiple unique materials
- Molecular Beam Epitaxy & Atomic Layer Deposition used
- Atomic deposition precision needed across multiple critical layers
- Complex band edge engineering in 3D

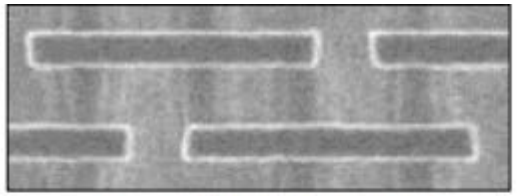
Emerging Device Material Solutions



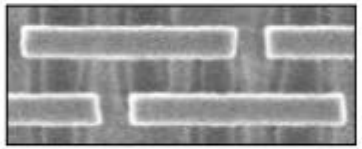
Lithography Challenges – not just about dimensions!



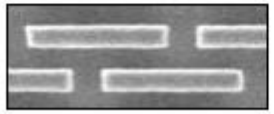
Lithography Challenges – overlay cost



45 nm, 0.346 um^2

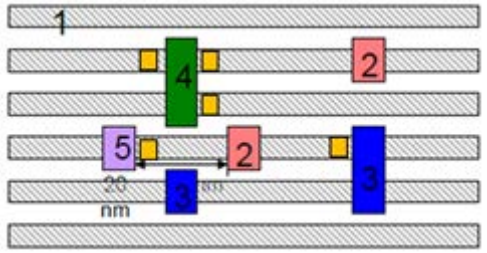


32 nm, 0.171 um^2

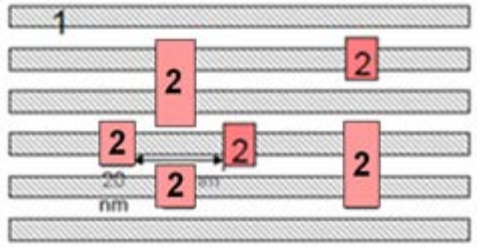


22 nm, 0.092 um^2

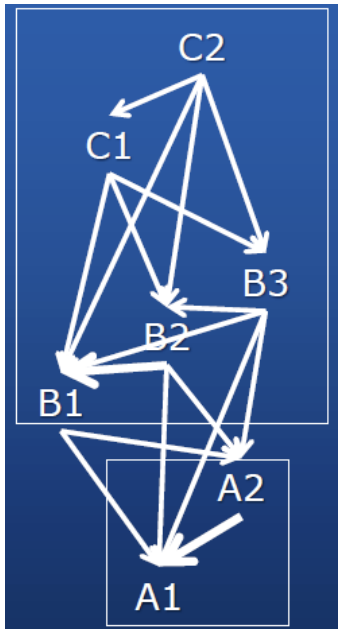
grating+cut litho



193i
5 masks



EUV
2 masks

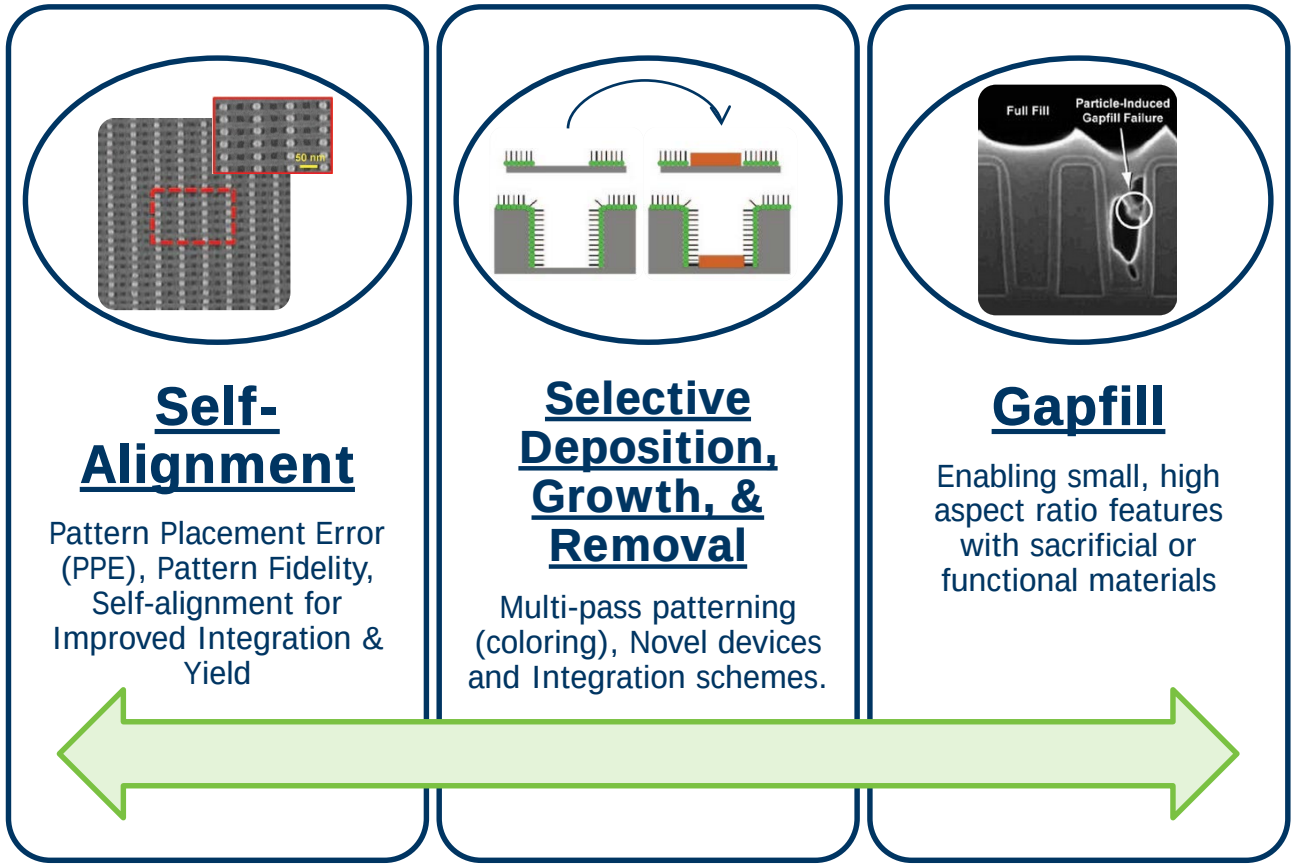


How do we manage this?

- Biggest challenges: managing **multiple mask passes** (per layer) & **pattern placement error**
- **EUV** attractive for resolution but also for process simplification, improved overlay, & reduced cost.
- Besides the light source, EUV also has other new material requirements (resists/developers, pellicles, etc.)

Sources
Mark Phillips, SPIE Adv.-Litho 2014
Florian Gstrein, ICPST-31 2014

Continued 2D-scaling via complementary techniques



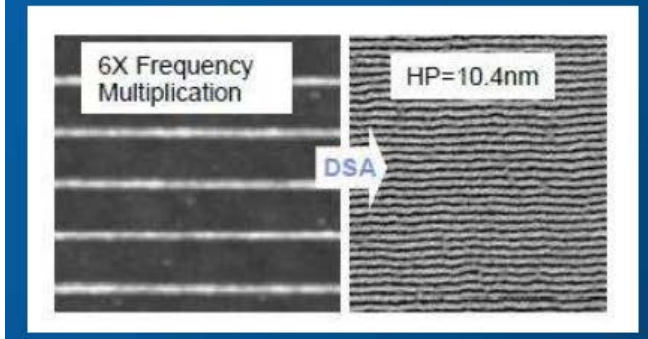
Ackn.
Todd Younkin, Intel 2014

- Enabled by the tools, integration, & **novel materials**.
- Must '**design for manufacturing**' to have timely success.
- **Pattern integrity & defectivity control** must meet rigorous manufacturing requirements.

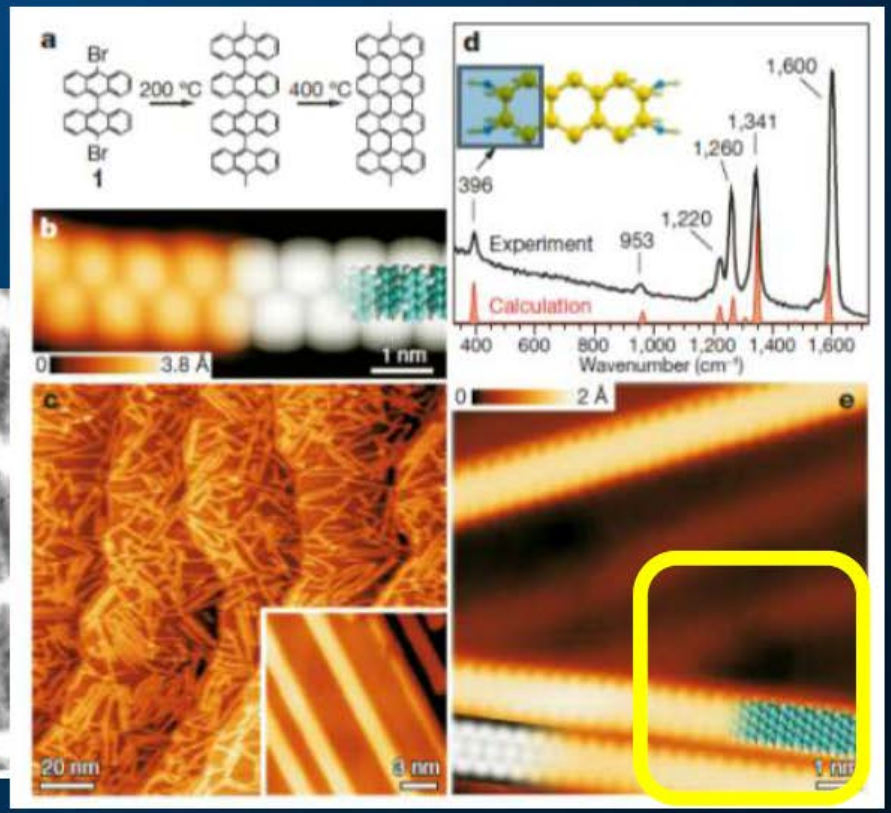
Emerging Lithography Processes

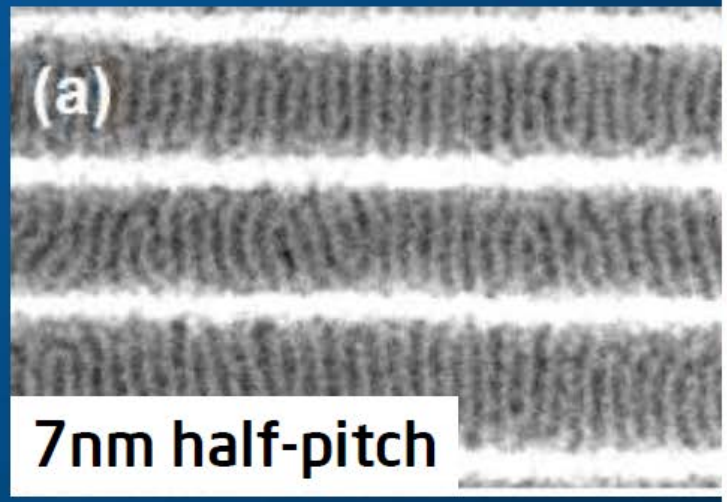
How Small Can We Fabricate and Control?

Source: Inte



"Self-Assembling Materials for Lithographic Patterning"
Bill Hinsberg et al, IBM.SPIE 2010





IBM, Park et al, Nanotech 19 2008

Cai et al, Nature July 2010

Lithography Challenges Summary

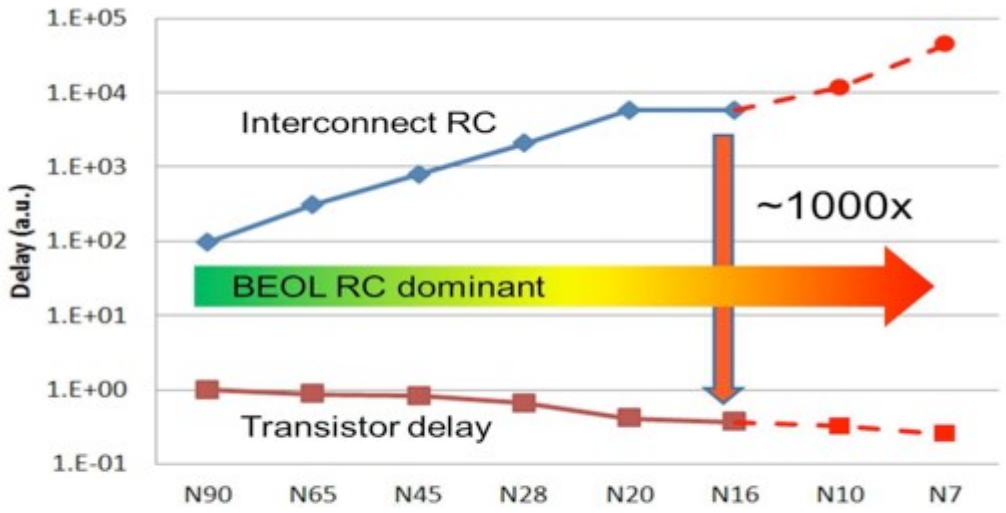
- **Feature scaling** has driven increasingly challenging requirements for:
  - **Pattern integrity** (pattern collapse, line edge roughness, etc.)
  - **Variability** control (of materials, patterns, etc.)
  - **Overlay** (especially for multi-pass patterning)

  …. and ultimately – cost-effective, high volume manufacturing ('HVM')

- **EUV** needed not just for dimensional scaling, but also for process simplification and cost

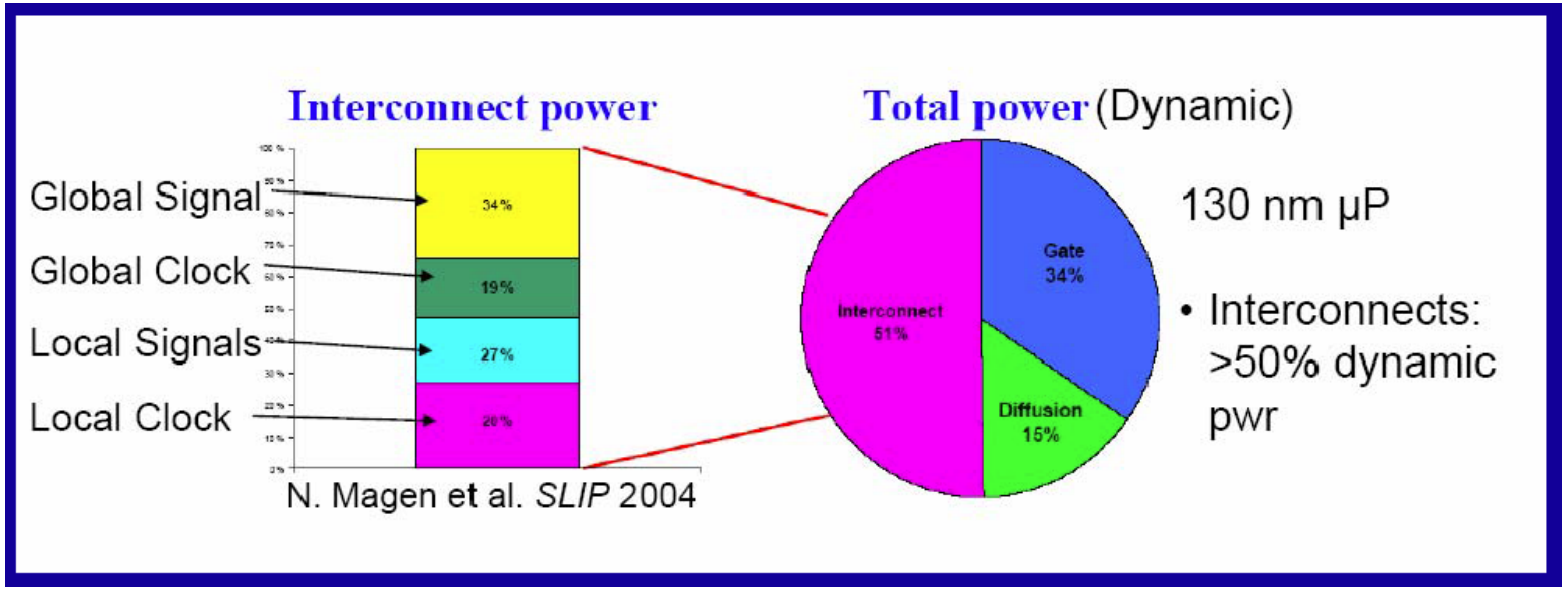
- **Emerging technologies** such as directed self-assembly, selective deposition, etc. can be used to augment and enhance patterning capabilities to extend Moore's Law, **but** only if they can be utilized cost-effectively within increasingly stringent HVM environments

Interconnect Challenge



(Yeap, Qualcomm, 2013)

Interconnects dominating chip energy and performance, not devices!



Interconnect Challenges

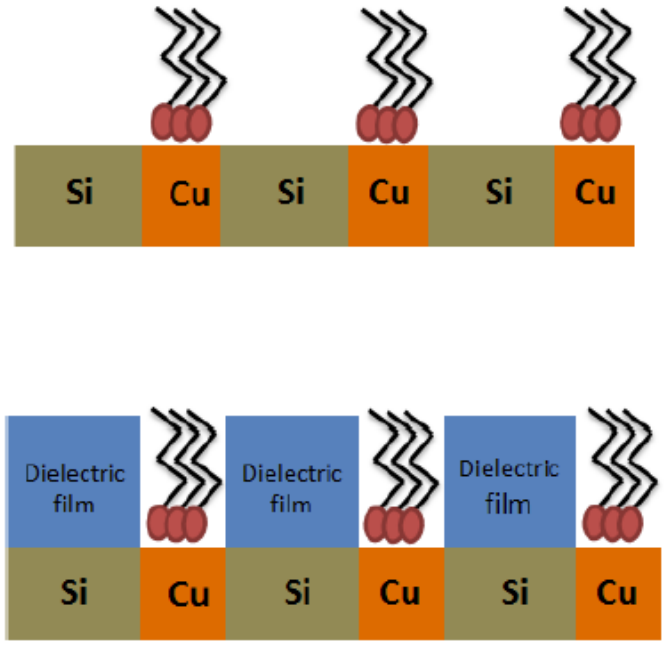
- Copper line resistance increasing exponentially with scaling, increasing dominance of circuit performance
  - Barrier metal resistance dominates at smallest dimensions
  - Sidewall and grain boundary scattering increases as a percentage with scaling
  - Uniform damascene trench filling – barrier materials and copper

- Dielectric Capacitance improvements not scaling
  - Porosity added to oxides to reduce capacitance not scalable due to mechanical robustness issues
  - Sidewall and grain boundary scattering increases as a percentage with scaling

- Reliability Challenges
  - Electromigration challenges increase with interconnect dimensional scaling
    - Current density increase
    - Cross-sectional line area decreases increasing susceptibility to failure
  - Dielectric failure (TDDB) challenges increase with scaling
    - Line spacing decreasing faster than voltage scaling
    - Alignment issues from multi-patterning create narrowed spacing at weakest points

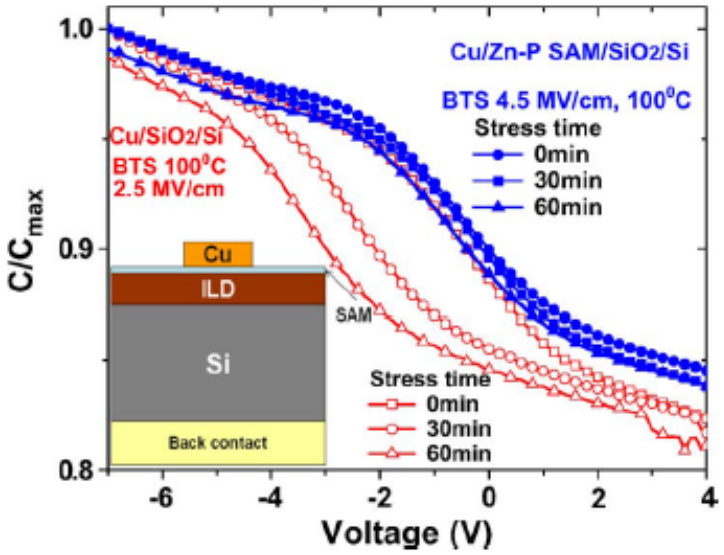
Potential Interconnect Materials Solutions - Ultra-thin Barriers, and Selective Deposition

Selective ALD deposition of dielectrics (or metals) using self-assembled monolayers

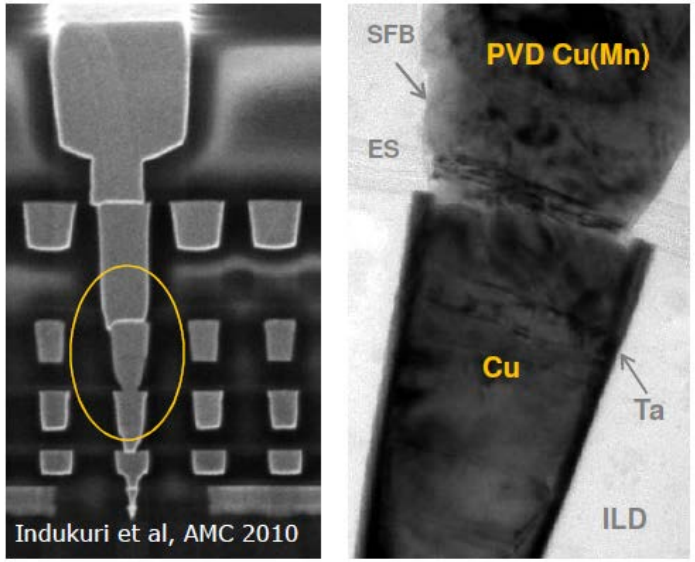


(Bent, et al, Stanford, 2014)

Ultra-thin Cu diffusion barriers using **self-assembled monolayers**



(Eisenbraun, et al, SUNY, 2013)

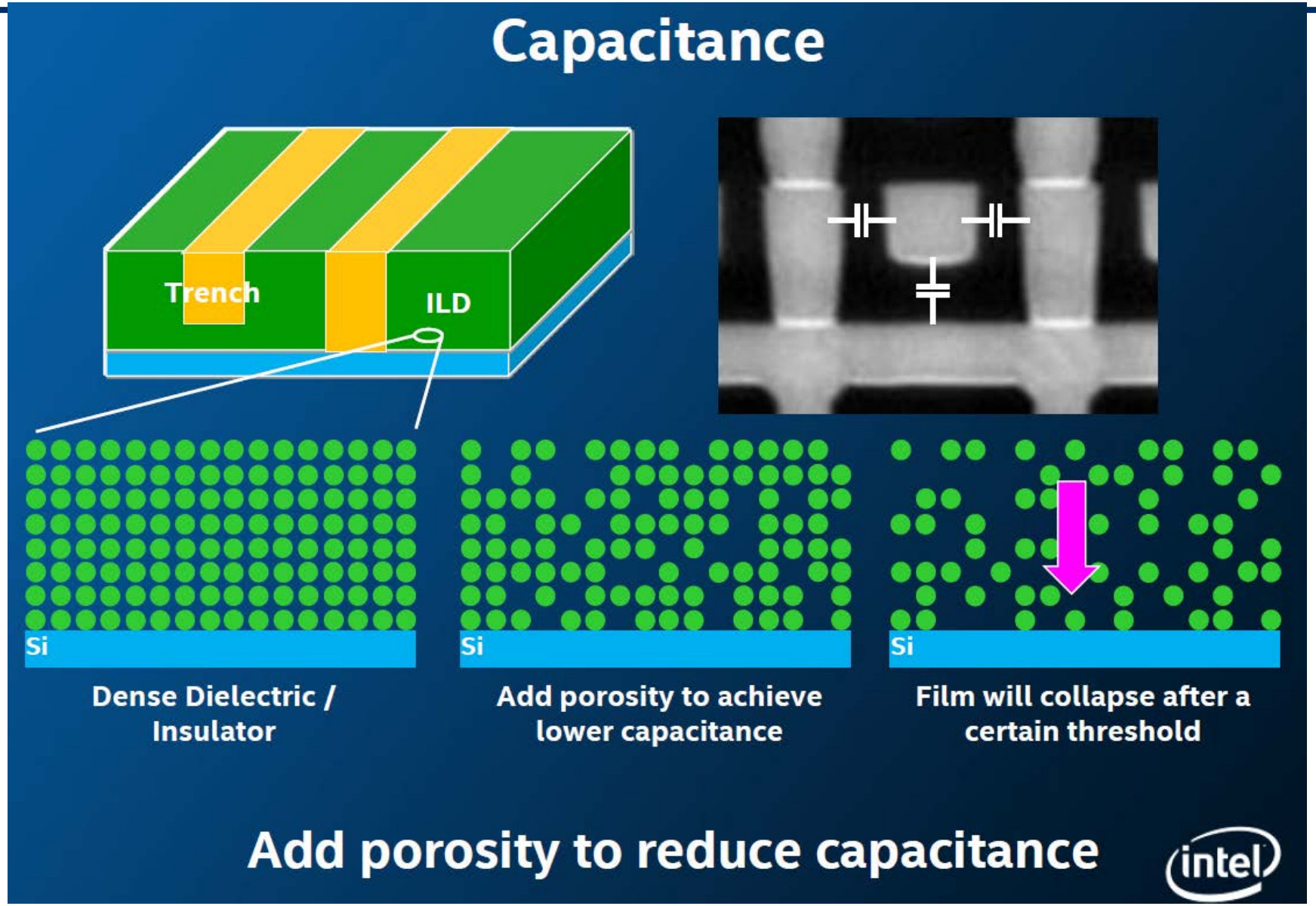


Self-forming Cu diffusion barriers

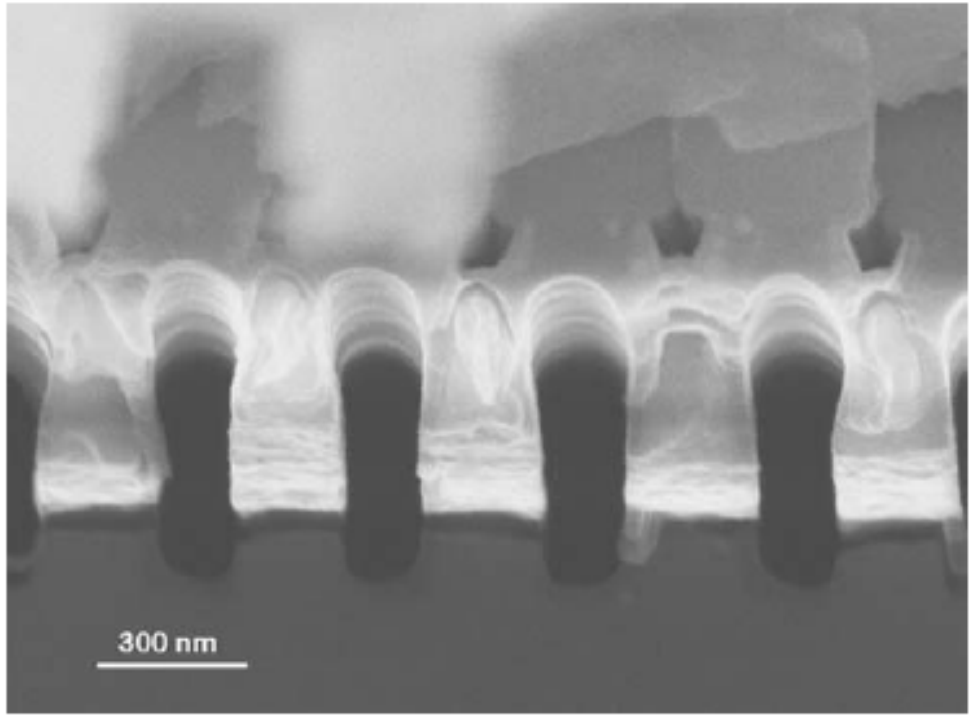
Interconnect Challenges

New Dielectric Materials Needed

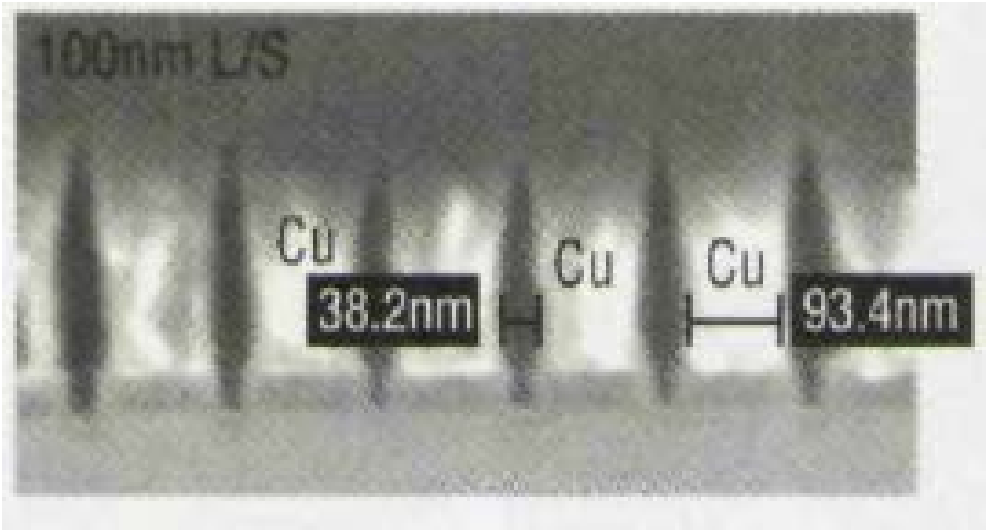
- Mechanical strength challenges



Potential Interconnect Materials Solutions - Air-gaps as Interlayer Dielectric (ILD) Material



(Kohl, et al, Georgia Tech, 2008)

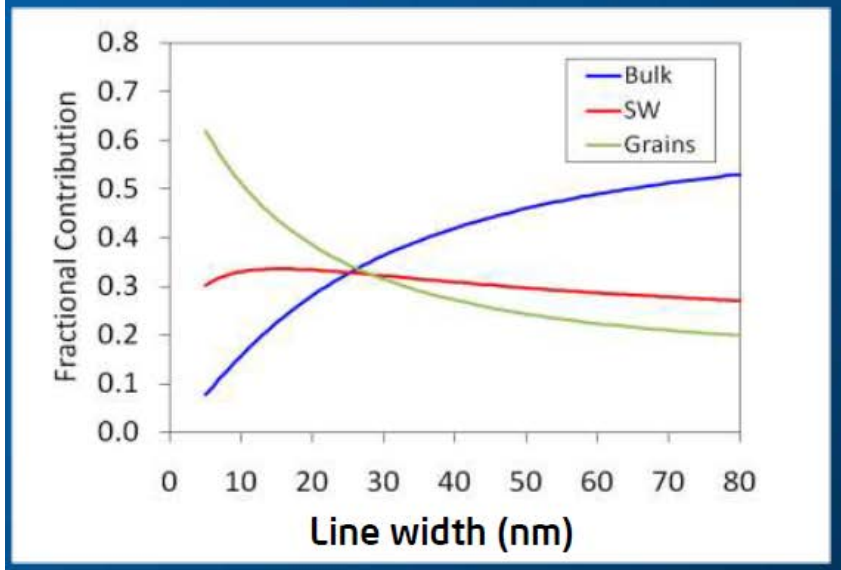


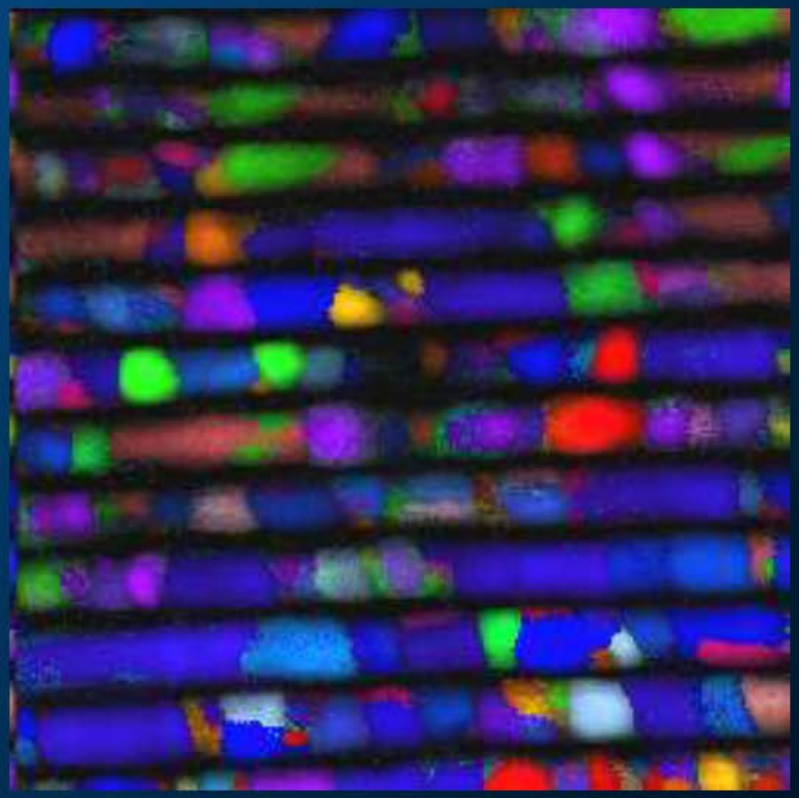
(Hoofman, et al, Philips Research,2006)

2014 IEDM Paper #3.7, "A 14nm Logic Technology Featuring 2nd-Generation FinFET Transistors, Air-Gapped Interconnects, Self-Aligned Double Patterning and a 0.0588µm2 SRAM Cell Size," S. Natarajan et al, Intel

Interconnect Challenges

Key Issue: For Small Dimensions, Scattering from Grains & Sidewall becomes Dominant



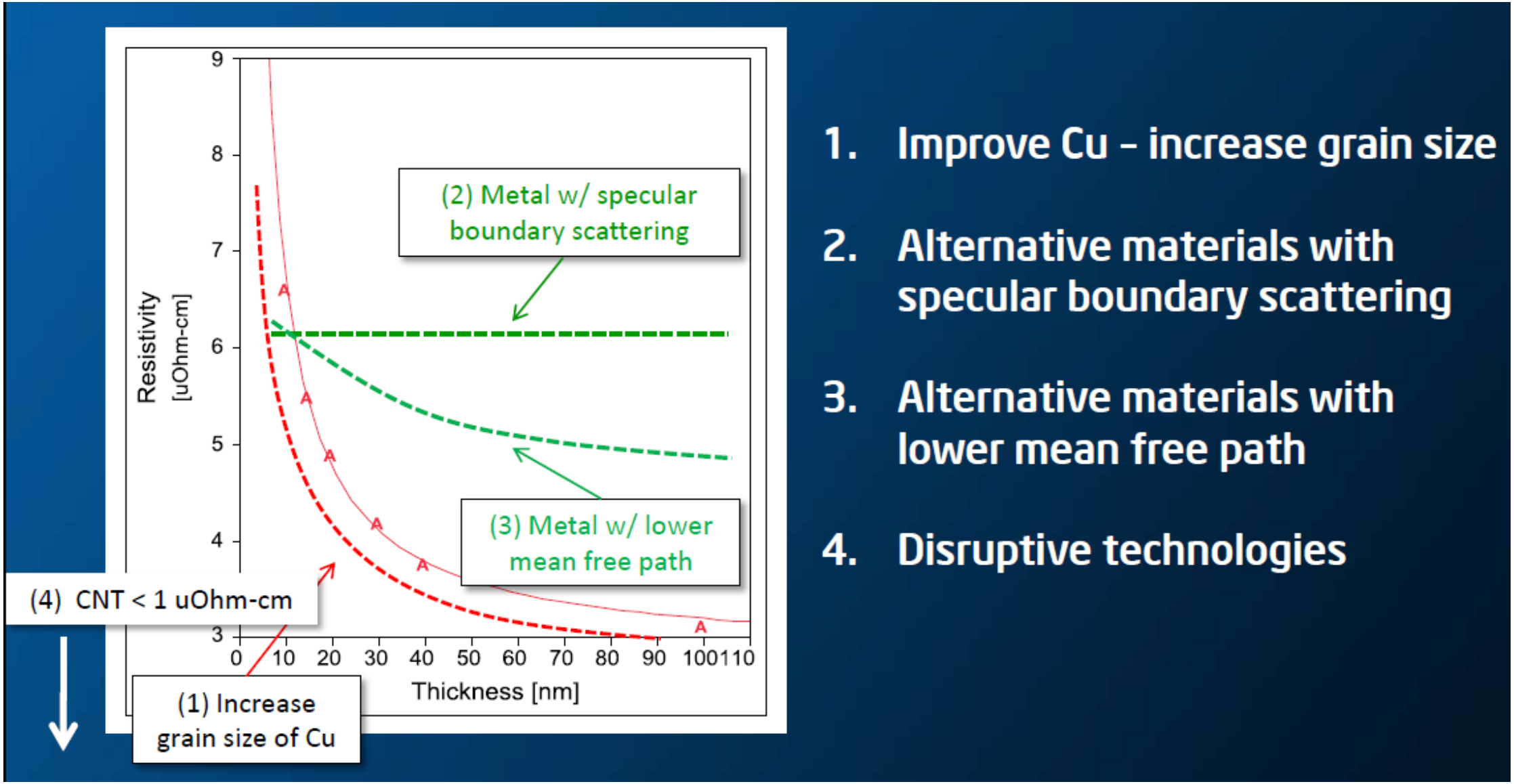


What if We Could Eliminate Scattering ?

Cu wires at 17nm drawn dimension
(colors indicate crystal orientation measured with DSTEM)

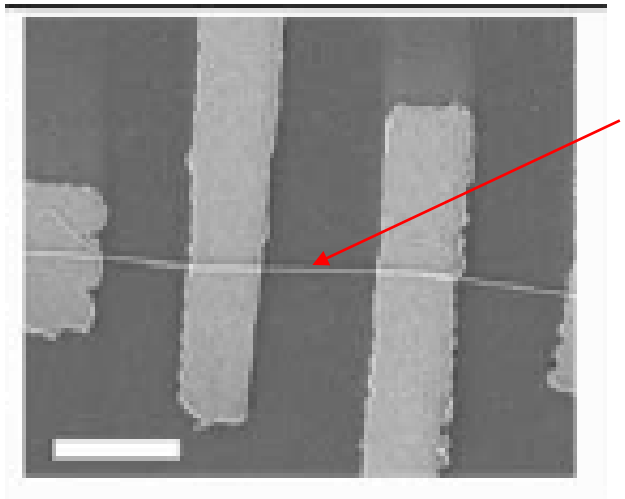
Source: Intel

Interconnect Challenges

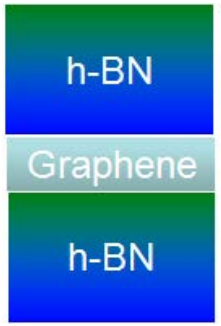


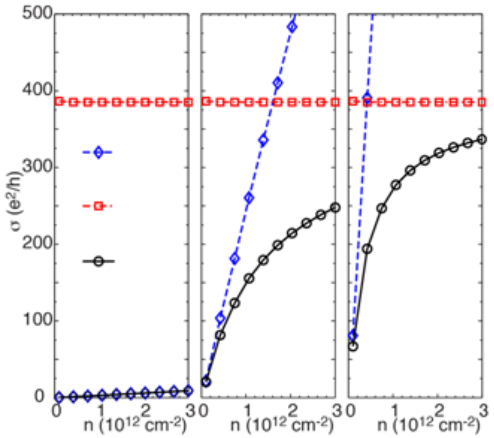
1. Improve Cu – increase grain size
2. Alternative materials with specular boundary scattering
3. Alternative materials with lower mean free path
4. Disruptive technologies

Alternative Materials

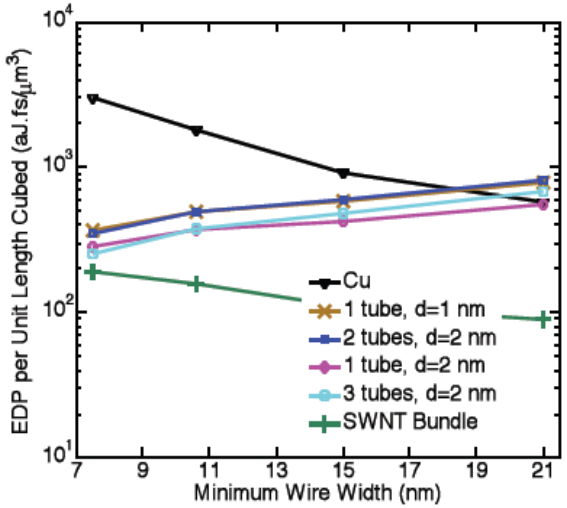


NiSi nanowires
(Wue, 2004)

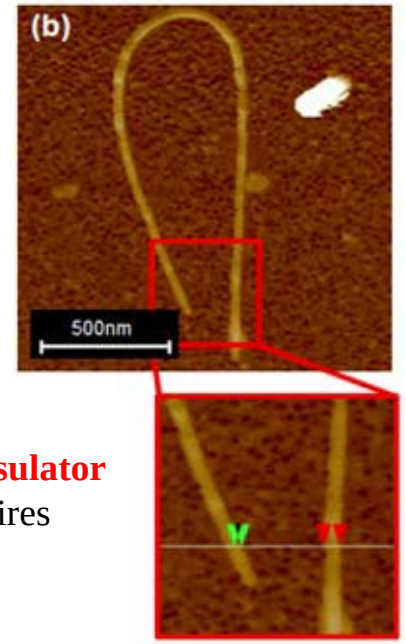




Conductivity of **GNRs** (and nanowires?) higher **on hi-K substrates** due to reduction of e-e interactions
(Nayak, 2012)



CNT's & SWNT bundles (Naeemi, 2012)

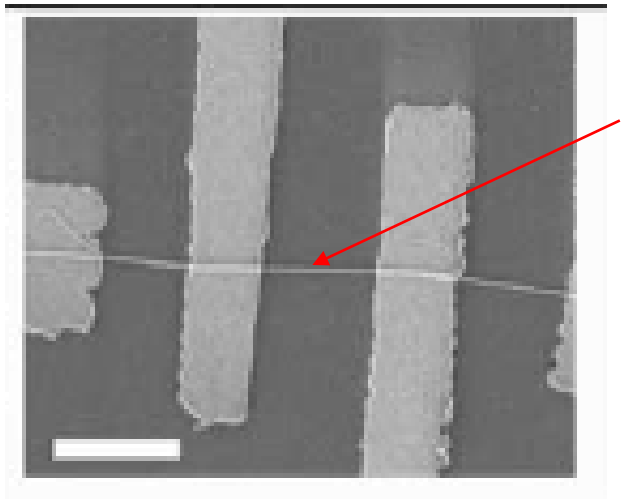


Topological Insulator
Nanoribbons/wires
(Yu, 2012)

Alternative Materials

Challenges:

- Control/Placement
- Contacts/Edges/Interfaces
- Integration



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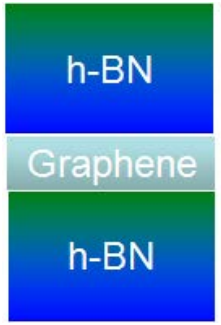

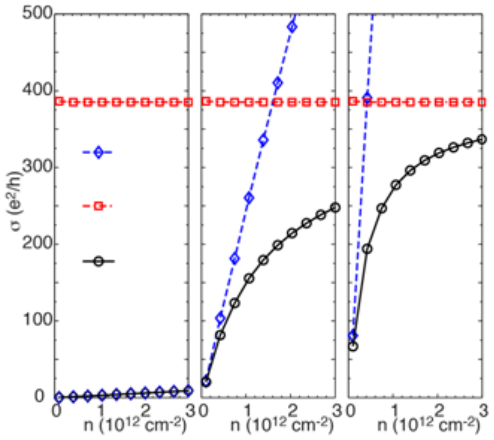

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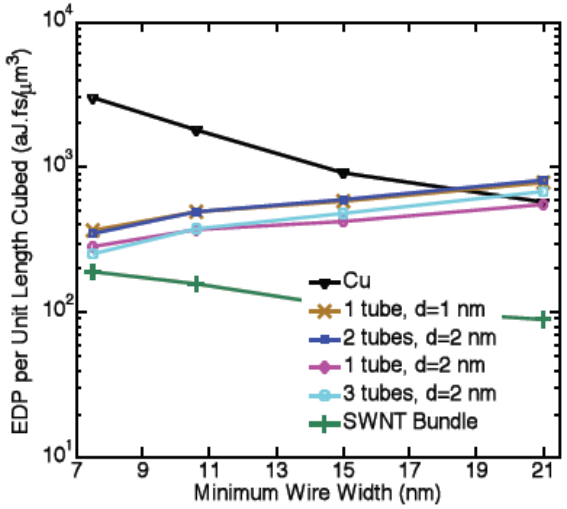

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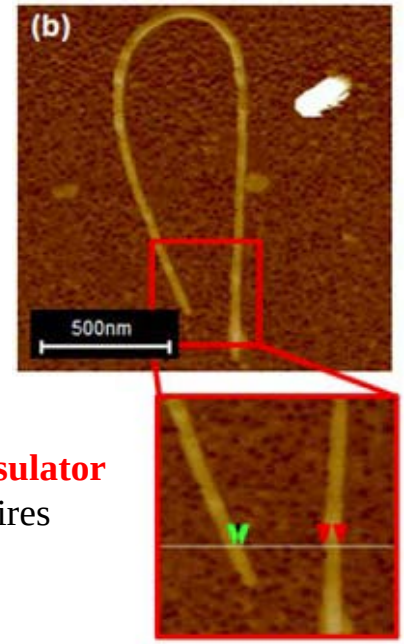

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The Future ?

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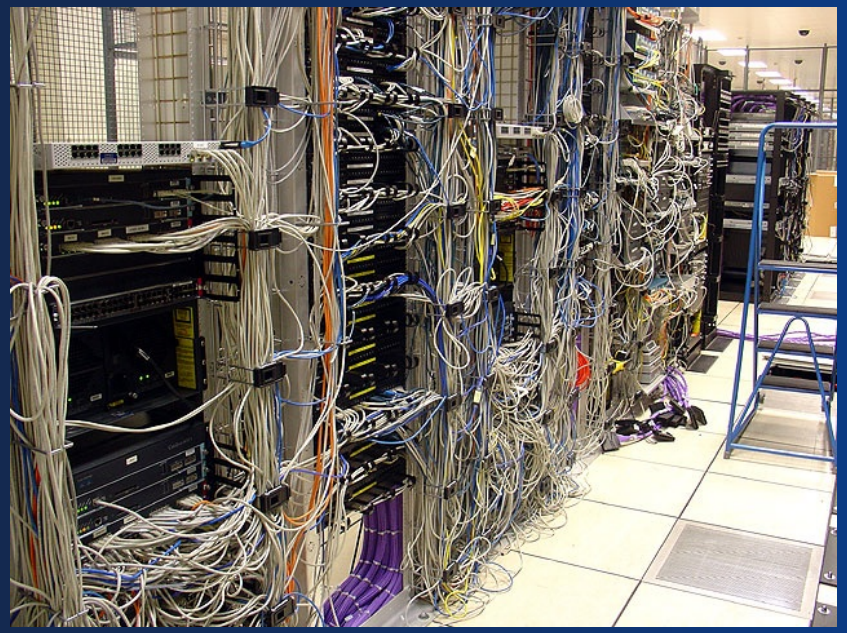
This ?



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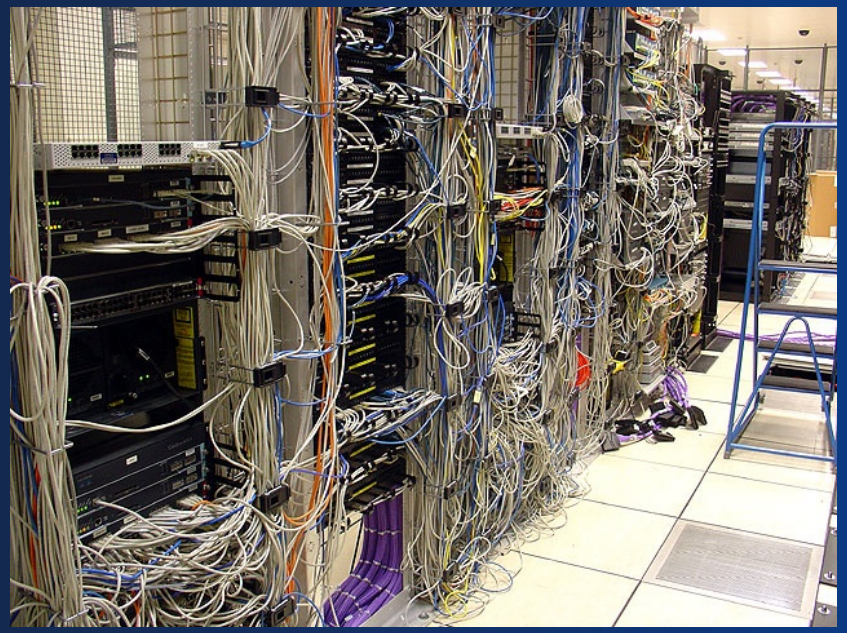
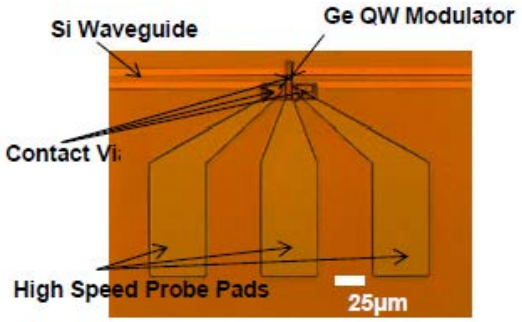


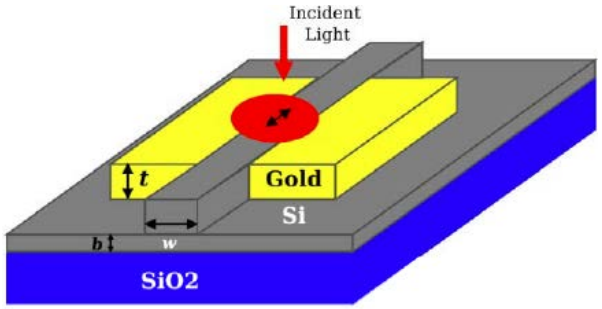
Or this ?

Alternatives?

Nanophotonics

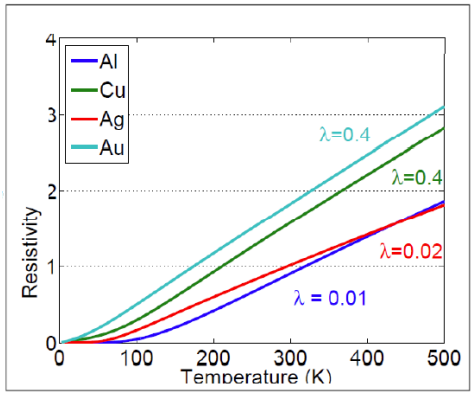


Ge quantum well **waveguide modulator**
- Dynamic energy/bit ~ 0.75 fJ
(D. Miller, 2012)

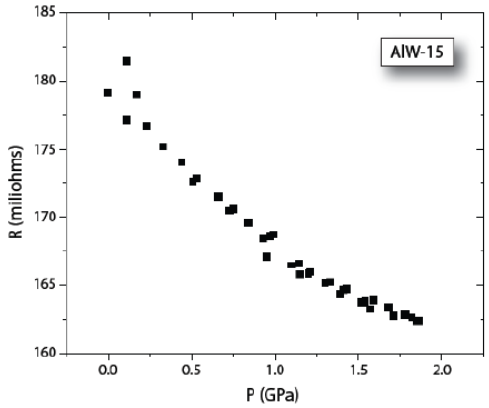


Tunable, nanoscale **resonant detector**
~ 60% absorption for 170nm thick Si
(D. Miller, 2012)

Phonon Engineering



nanowires with resistance lower than bulk values due to lower e-ph coupling



Strained Al (or other metals) to reduce electron-phonon coupling

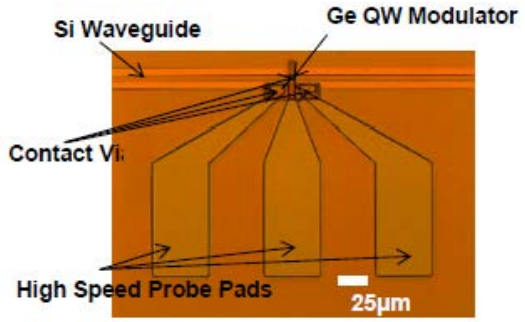
(Nayak, 2012)

Alternatives?

Nanophotonics

Challenges:

- Size
- Power
- Coupling



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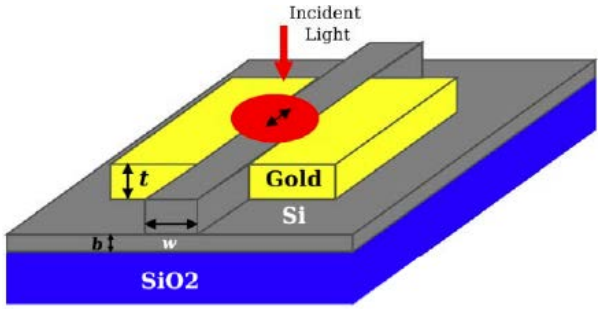

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Phonon Engineering

Challenges:

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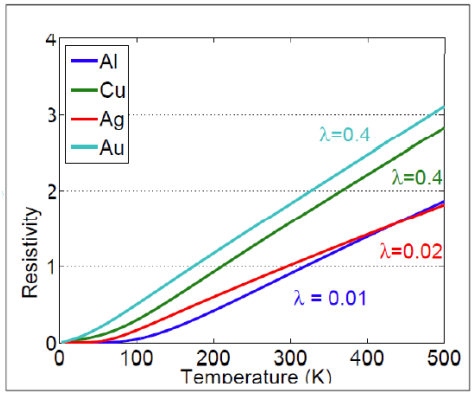
- Contacts
- Limited improvement



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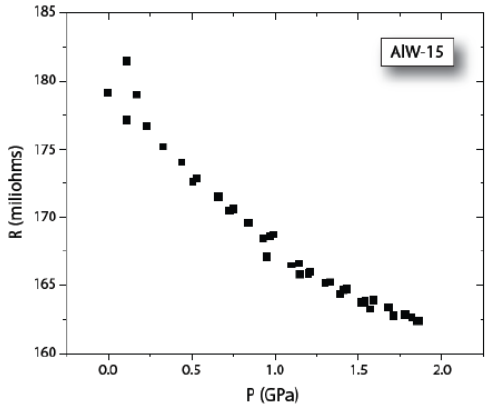

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What’s Beyond?

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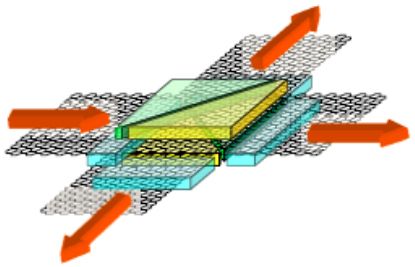
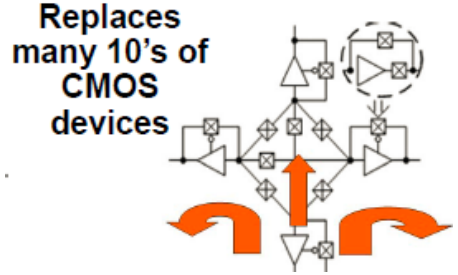
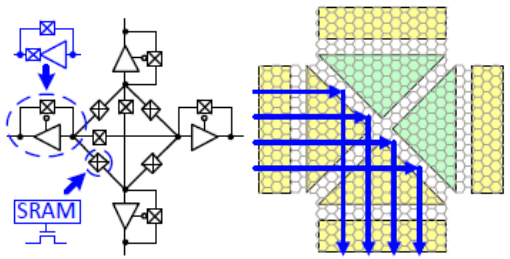
'Smart Interconnects'

Reconfigurable Graphene Nanoribbons
(Geer, Lee, et al, 2012)





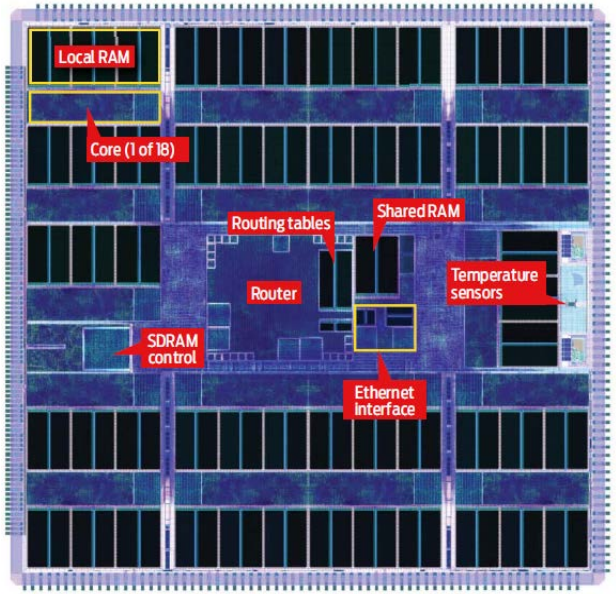


- Use with CMOS or stand-alone
- Replaces interconnect, logic & memory elements for monolithic, intelligent routers
- 8X power efficiency, 48X throughput density (simulated results to-date)

What's Beyond?

'Smart Interconnects'

'Brain-Inspired'
Reconfigurable, 'synaptic-like analog fabrics
(Furber, 2012)



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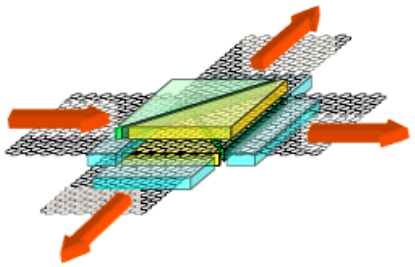

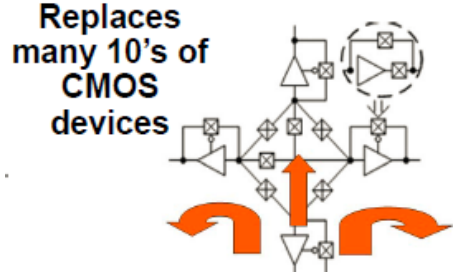

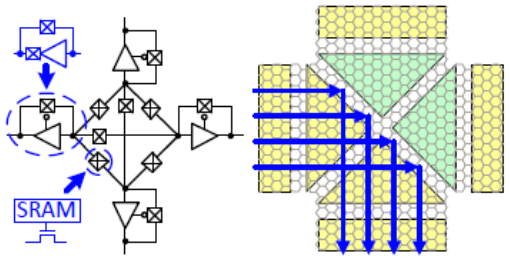

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Even Further?

Even Further?

‘No Interconnects’

Even Further?

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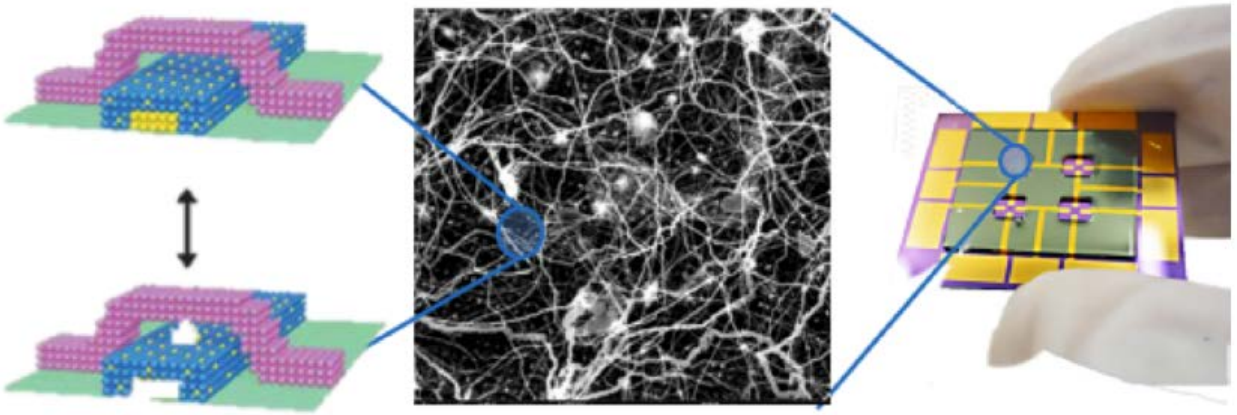
The ‘wires’ are the devices –
memory and logic

and, **they can LEARN!**

Even Further?



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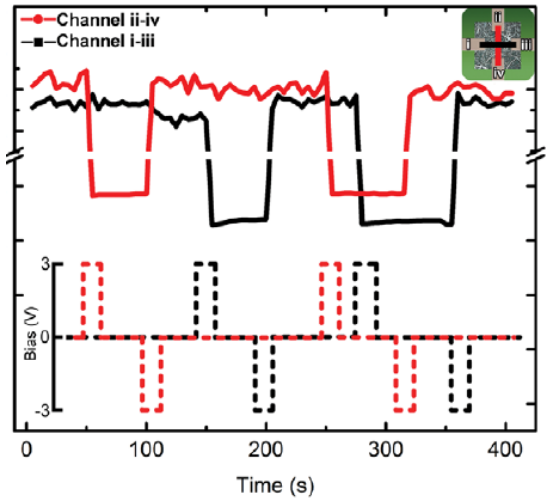

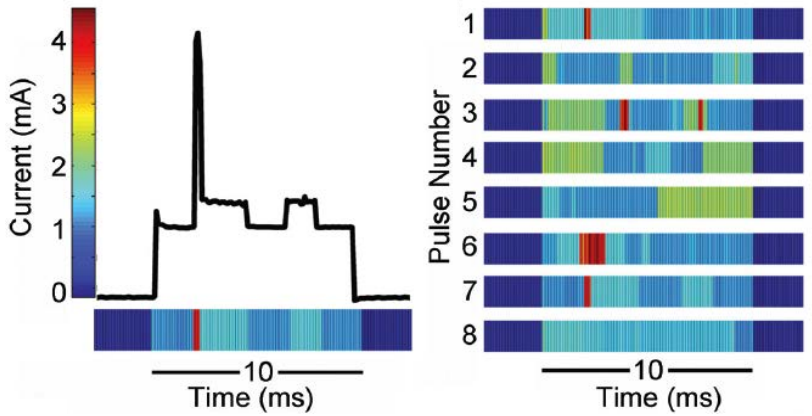

Atomic Switch Networks

(Gimzewski, Stieg, et al)

In Summary – A Call to Arms!

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- The IC industry is facing a serious and immediate challenge to its ability to continue to provide economical product advancements
- A deeper understanding of existing materials as well as the discovery of novel materials and cost-effective integration are key elements of the solution
- Atomic scale control is now essential
- Breakthroughs in any one area will not be sufficient
  - comprehensive and collaborative co-design and optimization must encompass the range from materials and devices to circuits and architectures to establish the new paradigms needed

In Summary – Hope!

“It was the best of times, it was the worst of times, it was the age of wisdom, it was the age of foolishness,
it was the epoch of belief, it was the epoch of incredulity,…”

In Summary – Hope!

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- **This is the most challenging and exciting time in at least the last 50 years to be in the scientific and engineering research community!**
- **The challenges are great, but the rewards will be greater!**

Acknowledgements

I want to thank the following individuals for contributing slides to this presentation:

Todd Younkin, James Clarke, Steve Putna, Mike Mayberry	Intel
Mehul Naik	AMAT
Alan Seabaugh	Notre Dame
Celia Merzbacher	SRC