

The Center for Power Electronics Systems – High Density Integration Research

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presented at: Packaging Review On-site Workshop



Center for Power Electronics Systems

Professors:

Fred C. Lee, Director Dushan Boroyevich, Co-Director Khai D. T. Ngo Rolando Burgos Qiang Li

Annual Research Expenditures \$4-5 million

Other:

- 1 Adjunct/Affiliate Faculty
- 6 Research Associates
- 4 Full-time Staff
- 2 Part-time Staff
- 14 Visiting Scholars
- 44 Doctoral Students
- **4 Masters Students**





What is the Future of Power Electronics?

Microelectronics



Moore's Law: "Every 1.5 years the cost of a 'bit' drops 50%."



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Power Electronics



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Electric Power



Between 1920 - 1970, every 1.5 years the cost of kWh dropped 5%. Since then it is constant.





Microelectronics vs. Power Electronics



Paradigm Shift #1: Standardization



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JRC

Paradigm Shift #2: Modularization



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Information Processing Paradigm Shift #3: Integration

Product Quality, Reliability, and Cost Factors:



- Rule-based
- Optimized macrocells
- Standard interfaces
- Hierarchical design
- Batch
 processing
 number
 of
 steps
- Small number of different materials
- Efficient use of materials

Volume Production

Cost Reduction





Power Processing #3: Integration

Product Quality, Reliability, and Cost Factors:







Integration in Power Processing !

Or Power Electronics Converter Design in the Last Century

Digital Controller – Digital Interface – Analog Interface – Sensor Interface – Power Supplies –

Gate Drives -

Power Stage





Center for Power Electronics Systems

A National Science Foundation Engineering Research Center, 1998-2008



Center for Power Electronics Systems

A National Science Foundation Engineering Research Center





Different Approaches to Integration

Integrated Load Converters:

- Low-cost, "intelligent motors"
 - motor as output filter
- Fast power delivery to microprocessors
 - minimum distance to load

• Power Distribution Converters:



Discrete converter Integrated converter

Standard-Cell IPEMs:

- Active IPEM
- Passive IPEM
- EMI Filter IPEM





Current Research Areas in CPES



CPES @ VT Achievement Highlights (1983 - 2014)

- 295 graduate degrees awarded (136 Ph.D., 159 M.S.)
- Over 3100 technical papers, theses and dissertations
- 245 invention disclosures
- 93 patents awarded
- Almost 100 government- and industry-sponsored research projects
- Over 175 CPES industry members
- 97 invention disclosures reviewed by IPPF (2002-2014)
- 65 IPPF-sponsored patent **applications** (2002 – 2014)

Current year:

- 84 industry members
- \$2.3M from industry consortium
- \$2.2M from sponsored research
- 17 research sponsors:
 - ABB
 - ARPA-E
 - Boeing
 - Department of Energy
 - **Energy Research Corporation**
 - **GE** Appliances and Light
 - **General Motors**
 - Halliburton
 - Huazhong University of Science & Tech.
 - NBF Tech
 - NSF
 - Office of Naval Research
 - Panasonic
 - Safran
 - Texas Instruments
 - Toyota Motor Engineering Mfg. NA, Inc.
 - United Technologies Aerospace Systems







CPES Industry Consortium

84 Members

40 PRINCIPAL PLUS MEMBERSHIPS (\$50 K/year)

- Same as Principal Member
- + Membership in a mini-consortium:
 - Guidance on research directions
 - Advance reporting of research results
 - Advance IP information

12 PRINCIPAL MEMBERS (\$30 K/year)

Preferential access to Intellectual Property
Seat on the Industry Advisory Board

25 ASSOCIATE MEMBERS (\$15 K/year)

- Free access to CPES publications, conference, and other information
- Representation on the Industry Advisory Board
- Industry residence and student internship programs
- Discount on short courses and other services

12 AFFILIATE MEMBERS (in-kind contributions or <\$15 K/year)

Free access to some CPES publications and conference

Limited discount on short courses and other services



Power Management Consortium

















Work Scope:

- High performance VRM/POL converters
- High efficiency power architectures for laptops, desktops and servers
- High frequency magnetics characterization and design
- Digital control
- **EMI**
- Solid state lighting
- Power management for PV system
- Power management for battery system
- High-efficiency and high power density power supplies with wide-band-gap power devices

Macroblock

NEC/TOKIN

SONOS







International





Mini-Consortium for Wide Band-Gap High-Power Converters & Systems

Newport News Shipbuilding A Division of Huntington Ingalls Industries

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VirginiaTech



VPTEnergy

Systems

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Work Scope:

DC and AC Microgrids

- Architectures and design
- Grid-, battery-, PV-, and windinterface converters
- Power management
- Modular Multi-level Converters
 - Modeling, design and control
 - Grid-interface converters
- Power Electronics for **Enhanced Grid** Performance and for Integration of Renewable **Sources and Storage Systems**

eysight

db-16

TEING

ENERGY SSC

HUAWEI

NATIONAL INSTRUMENTS

Mini-Consortium for High Density Integration



SiC Switch Comparative Characterization

Device	Continuous Current Rating (datasheet)	T _{MAX} (datasheet)	Normalized Die Area to Cree MOSFET
Cree SiC MOSFET (C2M0080120D)	31.6 A (25 °C); 20 A (100 °C)	150 °C	1.00
Rohm SiC MOSFET (SCH2080KE)	35 A (25 °C); 22 A (100 °C)	150 °C	1.21
GE SiC MOSFET (GE12N20L)	30 A (25 °C); 22.5 A (100 °C)	200 °C	0.97
Fairchild SiC BJT (FSICBH057A120)	15 A	175 °C	0.64
GeneSiC SiC SJT (GA10JT12)	6 A (25 °C)	175 °C	0.33
Infineon N-On SiC JFET (IJW120R100T1)	26 A (25 °C); 10 A (≤ 150 °C)	175 °C	1.29
SemiSouth N-Off SiC JFET (SJEP120R100)	17 A (100 °C); 10 A (150 °C)	150 °C	0.43





SiC Switch Comparative Characterization

Specific On-Resistance vs. Temperature



Conclusions:

- All devices have much smaller conduction loss than Si MOSFETs with similar ratings.
- All devices have much smaller switching loss than Si IGBTs with similar ratings.
- All devices operate satisfactorily at temperatures of 200 °C and higher.





E)

SiC Device Characterization and Modeling





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Design of a 0 Ω Gate Drive for 1.2 kV SiC JFET





Vds: 100 x Probe, 2500 V, P5100 Vgs: 10 x Probe, 300 V, P6139A Ids: 0.1 Ω Coaxial Shunt SDN-10









Turn-on/off at different temperatures 600 V – 10 A





Generations of GaN POL Power Module





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Advanced Research Proje



PCB Embedded Inductor Substrate

for 3D Integrated POL Module



Multi-layers PCB substrate with

embedded magnetic layer

$$f_s = 1^2 MHz, V_{in} = 12V, V_{out} = 1.2V, I_{out} = 20A$$





Module Design and Manufacture on 4-layer PCB



Open loop evaluation motherboard





Power Density Achievement



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Demands for High-Power-Density Converters



Planar Packaging









250°C Embedded Power



Sintered Bonds





Solder-Free Package



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Bi-directional Battery Charger for PHEV with MHz GaN Converter

3.3 kW, 500 kHz, GaN-based, Bidirectional Battery Charger





500 kHz hardware test result



High-Power-Density, 10 kW Motor Drive with High-Temperature Modules



Passive cooling with air at 70°C

Objective:

- Reduce weight through integration and high-temperature operation
- **Targets & Desired Features**
 - Specific power: > 2 kVA/lb
 - Device junction temperature 200-300°C with SiC devices
 - Advanced topologies
 - Reduced filter size



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High-Power-Density, 10 kW Motor Drive with High-Temperature Modules







DEING

High-Power-Density, 10 kW Motor Drive with High-Temperature Modules

- High-temperature SiC modules
- Sensorless control
- Soft start

Power Density

High-temperatu

1.27 kW/lb

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Low

• Fan load application



Atemperature

175 °C Converte







250°C Converter



DEING



Interleaved High Power Density AFE Converter



Reliability of Direct-Bond-Copper (DBC) Substrate

Reliability of DBC substrate in thermal cycling between -55°C and 200°C



• DBC substrate fails in

< 20 cycles







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Reliability of Direct-Bond-Copper (DBC) Substrate

Reliability of DBC substrate in thermal cycling between -55°C and 200°C









Targets:

- > Junction temperature up to 250°C.
- > Ambient temperature over 150°C.







Modified Hybrid Packaging Structure







Multiple chip Hybrid Power Module



Power module thermal test





Integration of High-Temperature Three-Phase Rectifier





Converter Thermal Testing





Ambient temperature test point: -50°C, -25°C, 0°C, 25°C, 50°C, 75°C, 100°C, 125°C, 150°C

Test Picture for 150° C Ambient Temperature

Electrical and thermal performance met design targets. Ceramic capacitors and their attach to PCB exhibited early failures.



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High-Temperature 3-Phase AC-DC Converter for Embedded Generators in MEA





- High-temperature and high-power-density
- Ambient temperature: 200 250 °C
- Switching frequency: 70 kHz





Need a power module capable of both high-temperature & high-frequency operations!





High-Temperature Packaging Materials Used





High-temperature capability of the material; Suitable combinations of materials to achieve higher reliability





1200 V, 60 A SiC Phase-Leg Module Design



Improved substrate layout to minimize loop inductances



Fast & clean switching



Hard switching w/ $R_G = 0 \Omega$ Fast di/dt & dv/dt with small V_{DS} overshoot

Fabricated module with DC decoupling capacitors



Switching Loss is 10-20% of an equivalent IGBT





200 °C, 1200 V, 60 A SiC Phase-Leg Module: Continuous Operation at 200 °C





Test results at 560 V & 100 kHz







200 °C, 1200 V, 120 A SiC Phase-Leg Module: Module Design







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11 12

cm 1____

9 10

10



System Design

ROLLS



Converter Layout









Converter Layout





Cooling terminals

DC terminals





Converter Testing





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Utilization of 10 kV SiC Devices for Grid-scale Applications



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 Low-inductance interconnection achieved using molybdenum bumps and DBC.









 Low-inductance interconnection achieved using molybdenum bumps and DBC.





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V_{DC}

Om

- Low-inductance interconnection achieved using molybdenum bumps and DBC.
- Embedded decoupling capacitors shorten the commutation loop.





20 mm

-V

= 3 nH



• Stacking DBC substrates can help to reduce the peak electric field.







Stacking DBC substrates can help to reduce the peak electric field.



1. High-Density → Thermal & Electric Field





Each MOSFET pair has its own gate and power loops.







The <u>system interface</u> must be carefully designed to prevent partial discharge.







Surrounding pins with an <u>elliptical conductive</u> <u>shield</u> minimizes the peak electric field.







Conclusion

 The goal of standardized "Integrated Power Circuits" that enable high-density integration has not been achieved.

There are too many different functions:

- Electrical switching,
- Electrical conduction,
- Thermal conduction,
- Electrical insulation,
- Electrostatic energy storage,
- Magnetic energy storage,

that require too many different heterogeneous materials.

- New semiconductor materials and devices impose new challenges on packaging:
 - Reduced layout and interconnect designs for reduced parasitics that enable high frequency operation;
 - New high temperature materials with better matched CTEs for hightemperature operation;
 - New high-voltage materials and designs for eliminating "air" as insulator.



