Possible Needs for Automotive: Mechanically Flexible Interconnects and Advanced Cooling

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Mechanically Flexible Interconnects in Extreme Condition Applications

- Interconnects in extreme condition (temperature, vibration, impact, and etc.)

- We need reliable interconnects under vibration and extreme temperature

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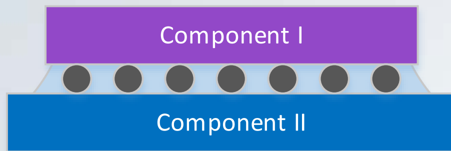
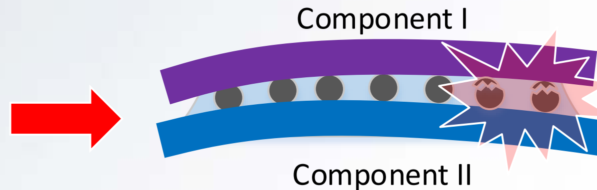
Mechanically Flexible Interconnects in Extreme Condition Applications

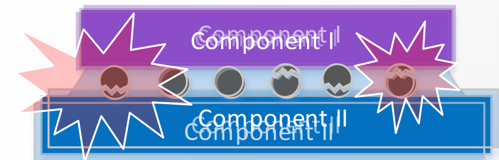
Conventional solder based interconnects



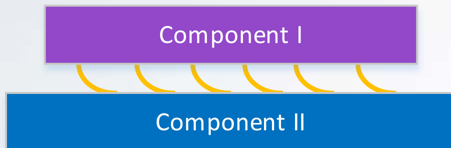
Extreme temperature variation



Vibration or impact



Mechanically Flexible Interconnects



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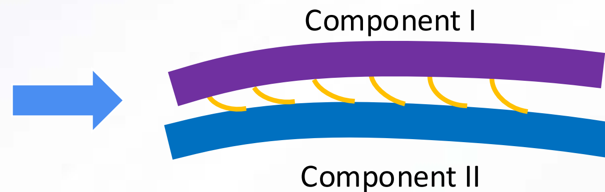
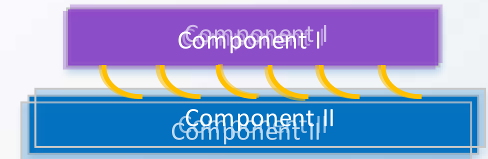
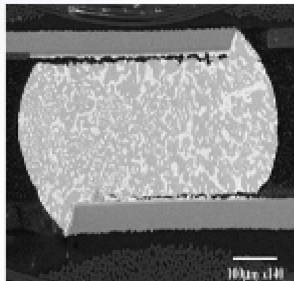


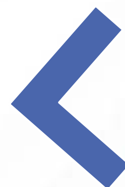
-. Flexibility can compensate any warpage in components

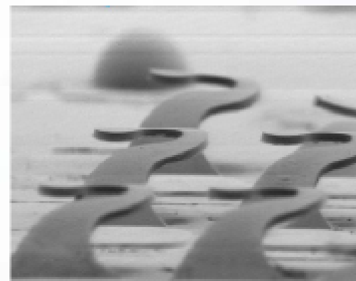
Vibration or impact



-. Flexible interconnect and pressure based contact can maintain good connection between components







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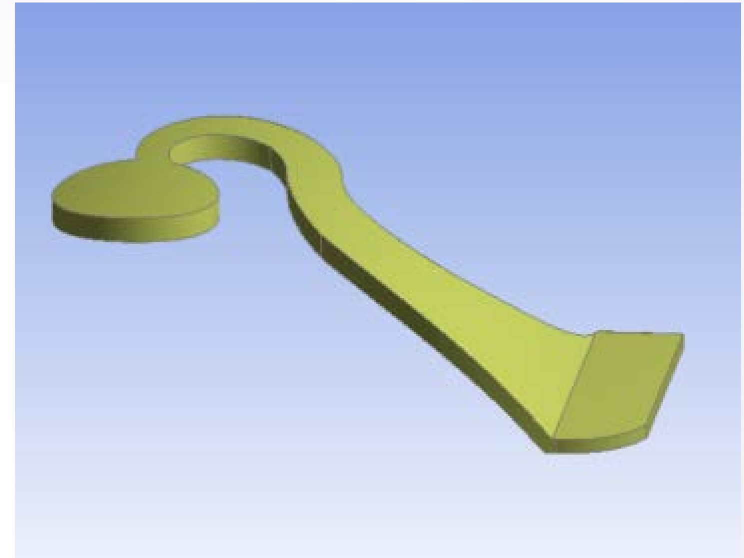
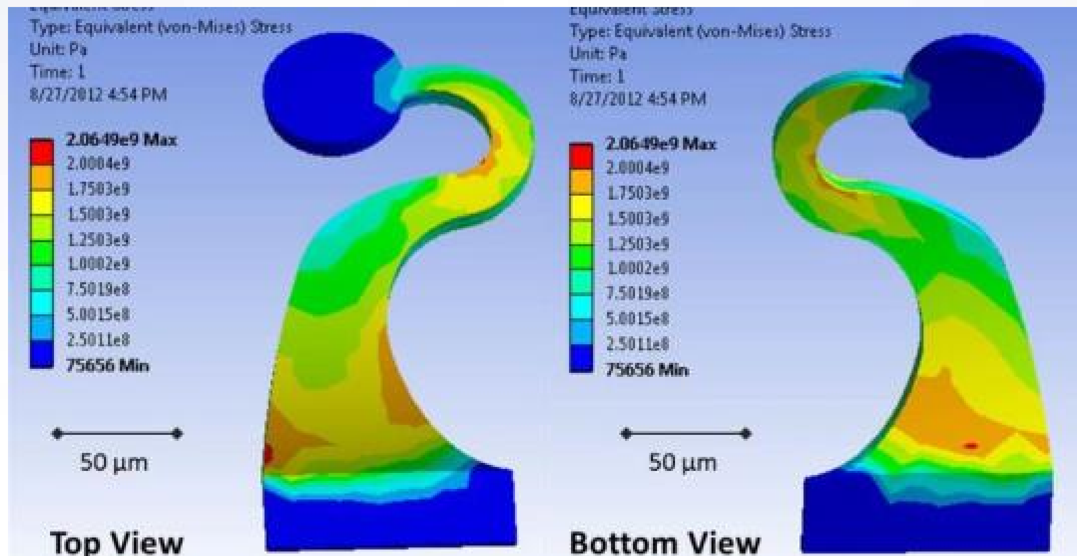
Mechanically Flexible Interconnects: Design and FEM Analysis

- Design Strategy
  - Material
    - High yield strength: NiW
  - Geometry
    - Uniform inner stress:
      3D tapered and curved design





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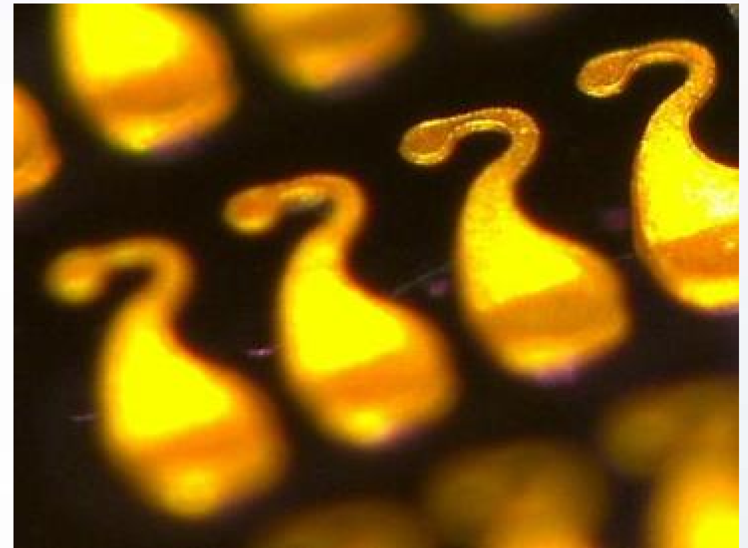
Design and FEM Analysis

- Design Strategy
  - Material
    - High yield strength: NiW
  - Geometry
    - Uniform inner stress:

      3D tapered and curved design
  - Finishing
    - Enhanced life-time:

      Electroless gold passivation layer



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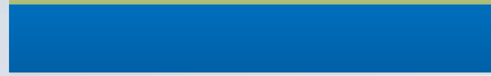
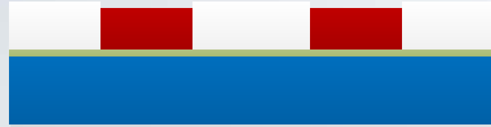
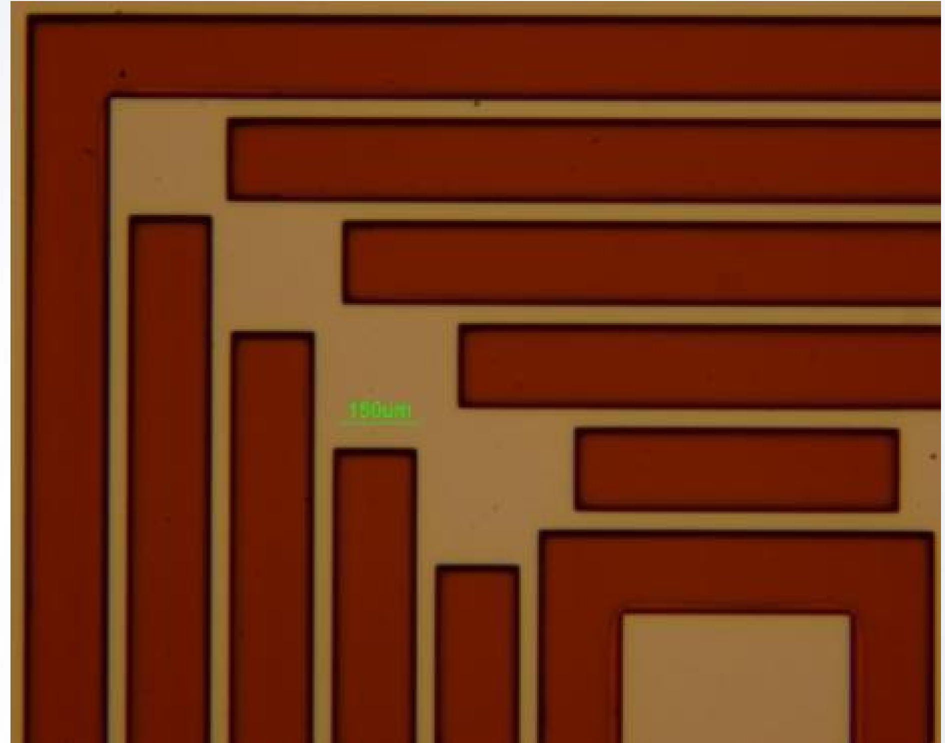
Fabrication of MFIs



A. Wafer Clean and surface passivation



B. Sacrificial Dome Patterning



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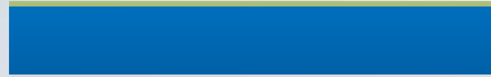

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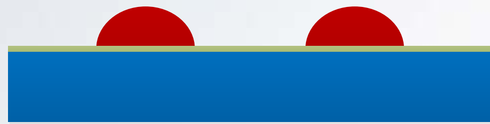
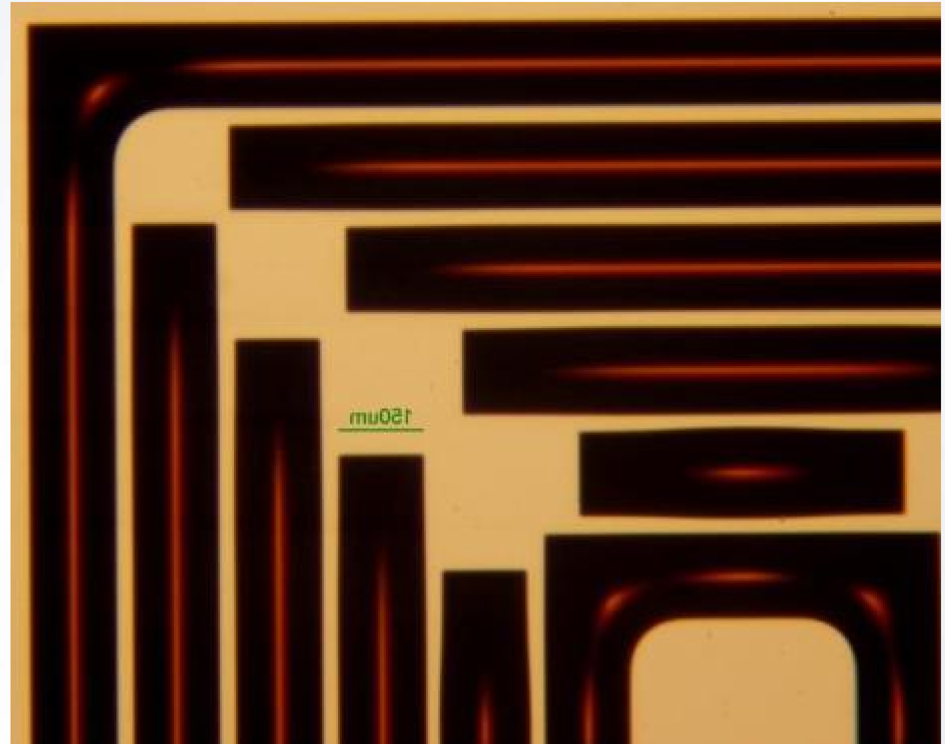


C. Sacrificial Dome Reflow



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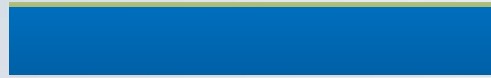

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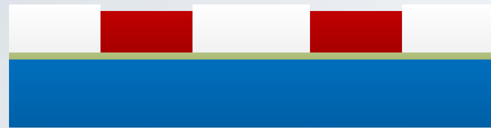

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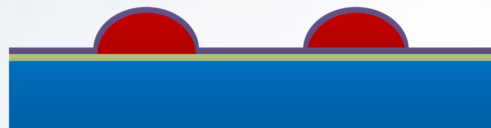
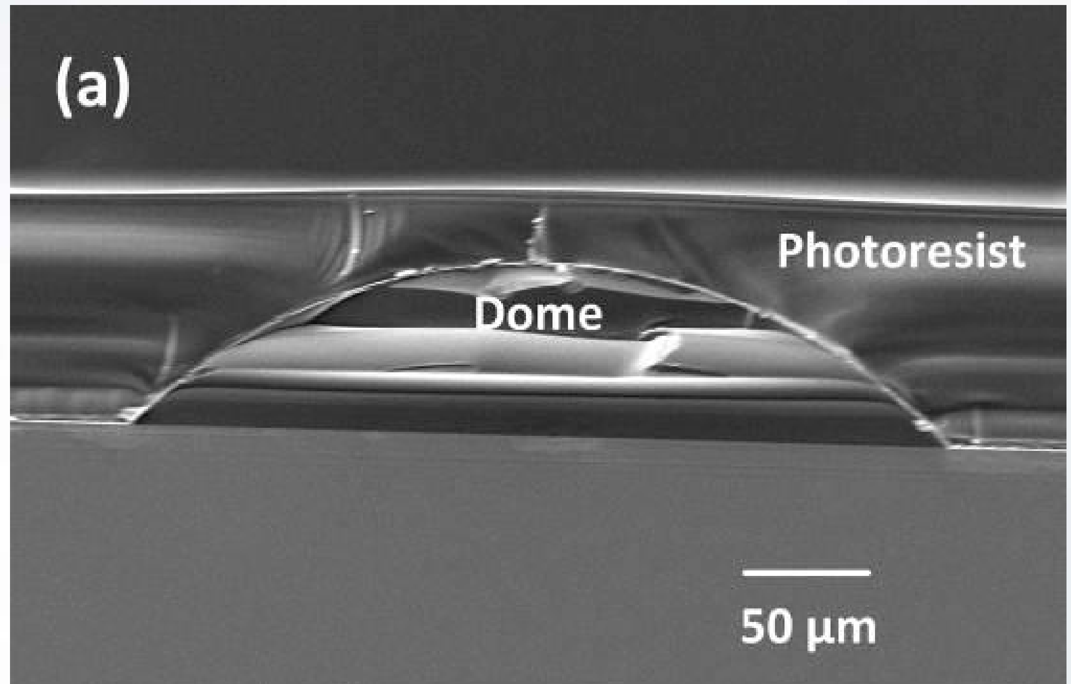
C. Sacrificial Dome Reflow



D. Electroplating Seed Layer Deposition

E. Photoresist Spin-coating for Electroplating Mold Formation



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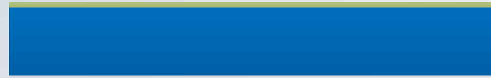

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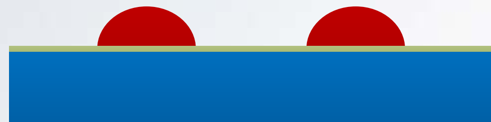

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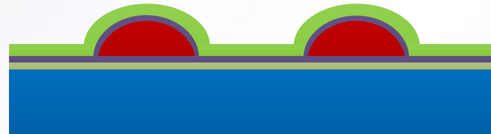
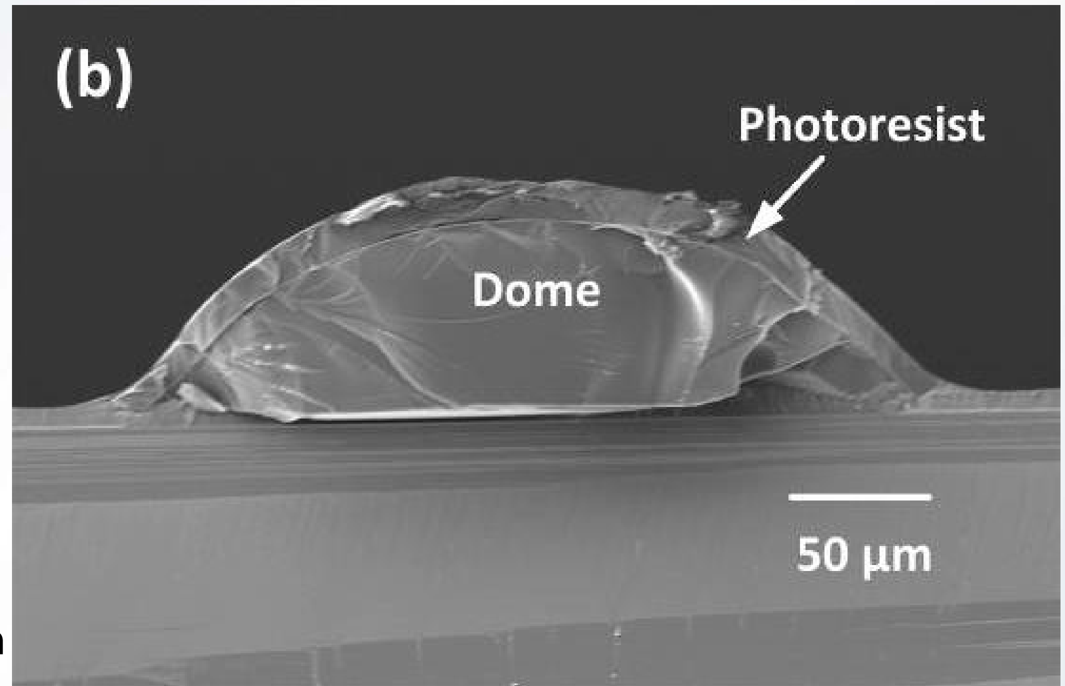


E. Photoresist Spray-coating for Electroplating Mold Formation



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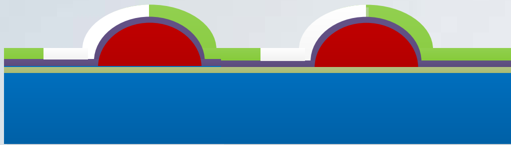

F. Electroplating Mold Patterning

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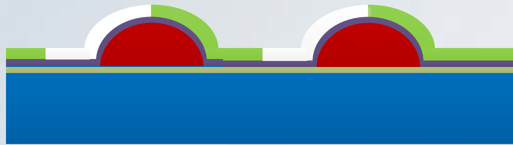

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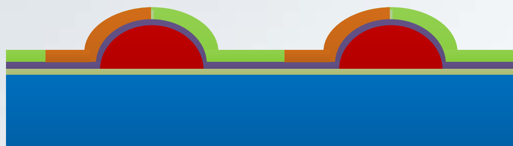
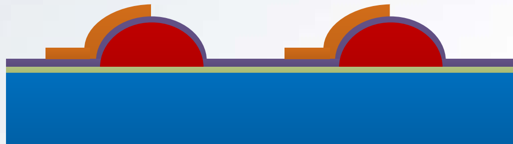


G. MFIs Formation Using NiW Electroplating



H. Electroplating Mold Removal

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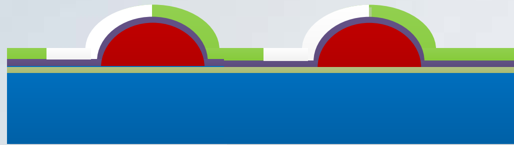

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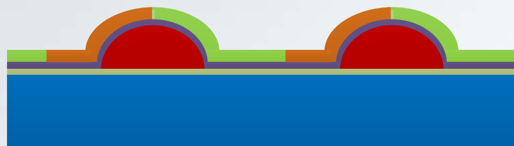

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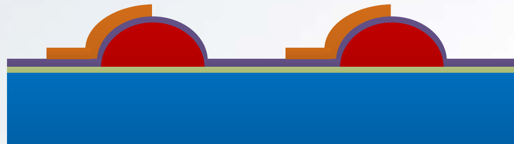

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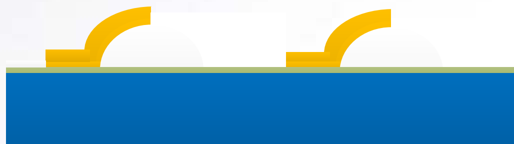
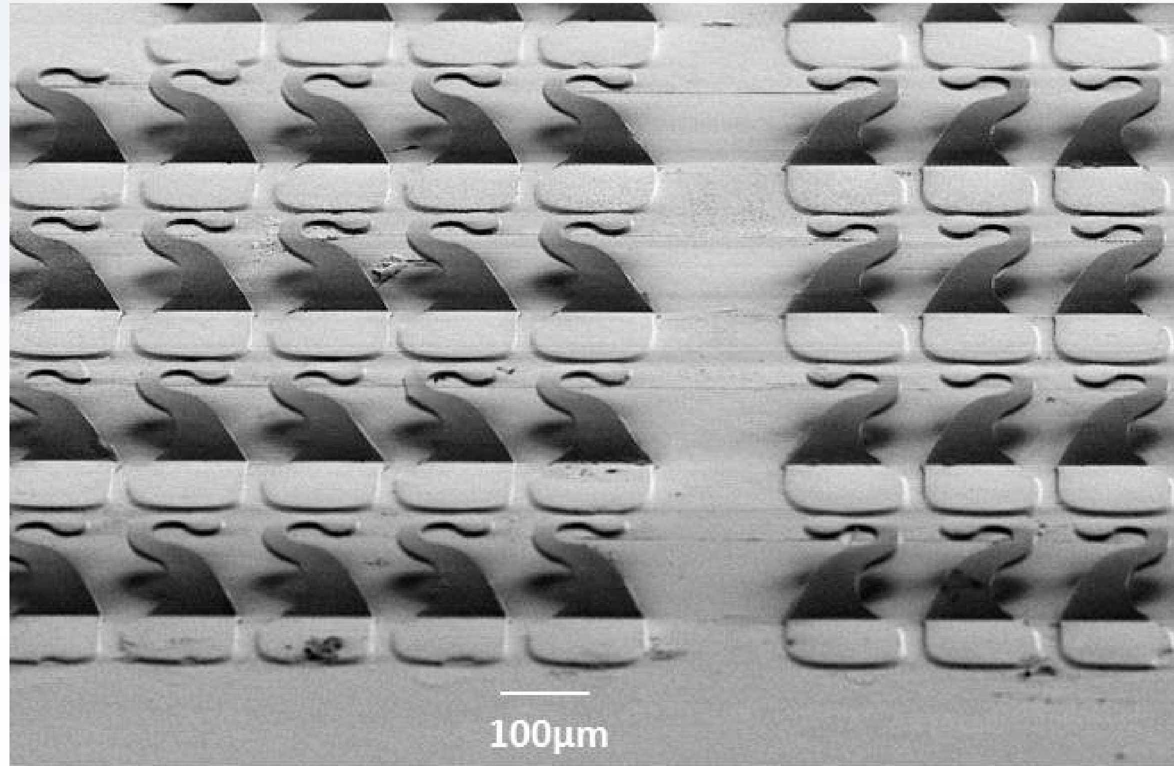


I. MFIs Releasing and Gold Passivation



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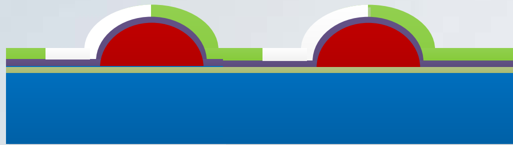

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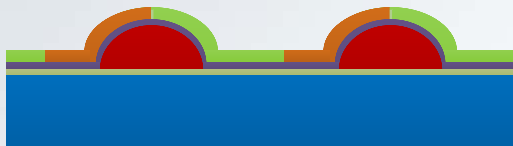

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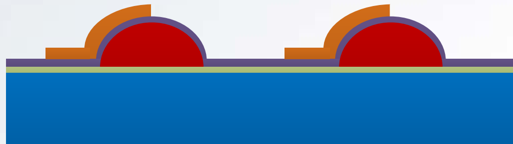

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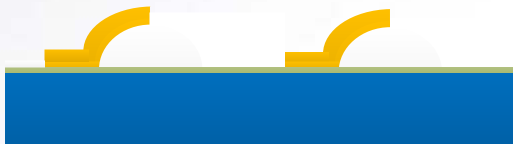

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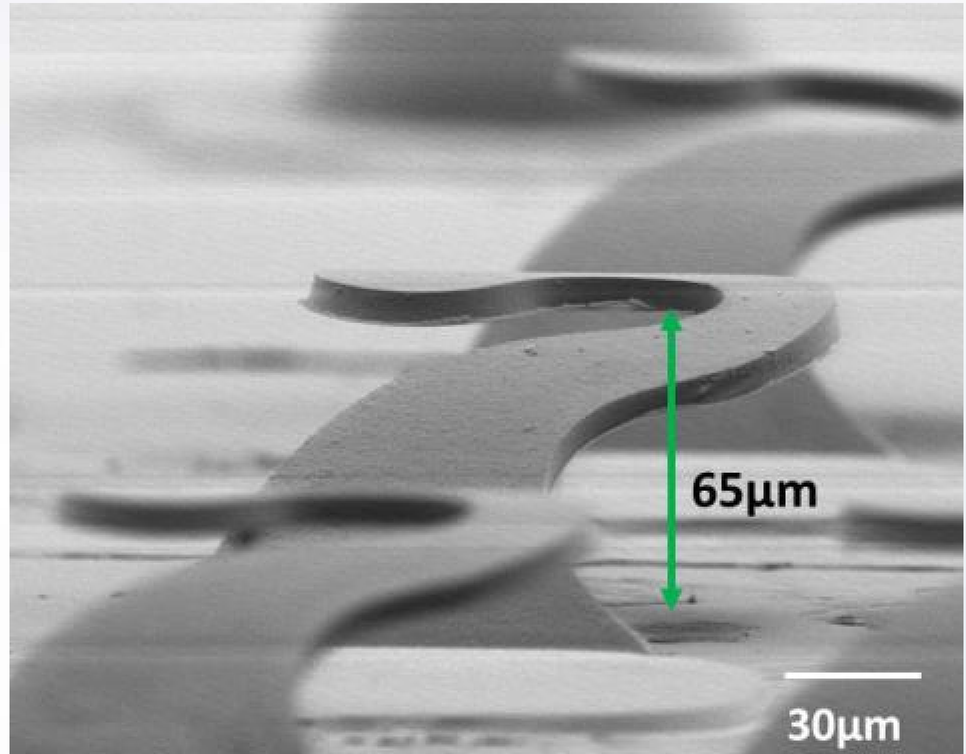

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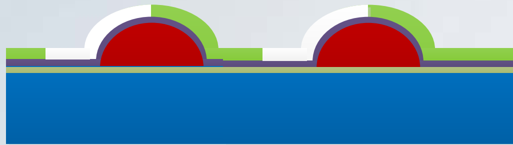

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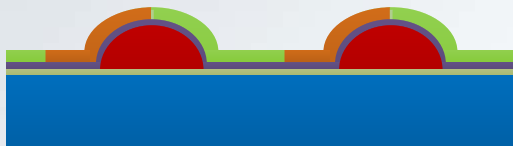

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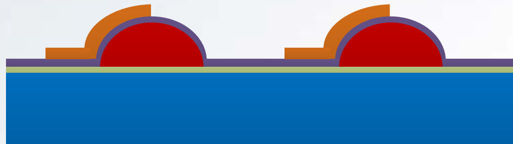

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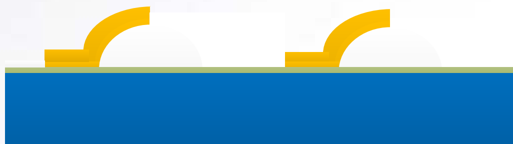

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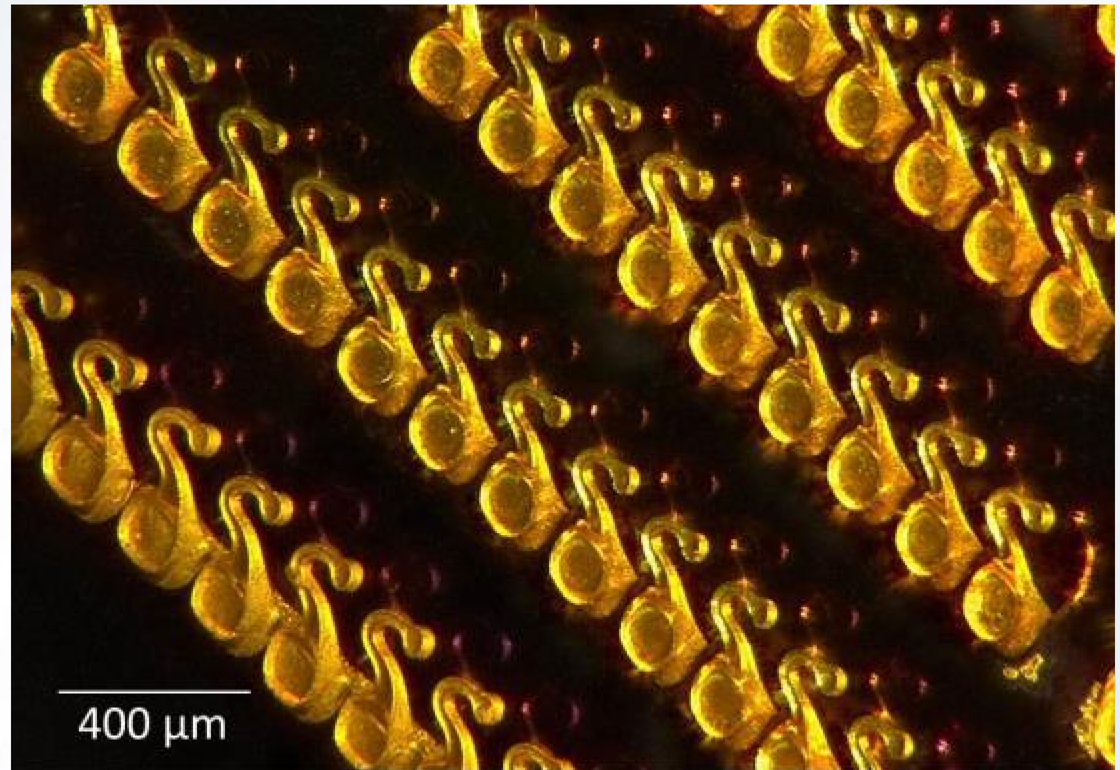

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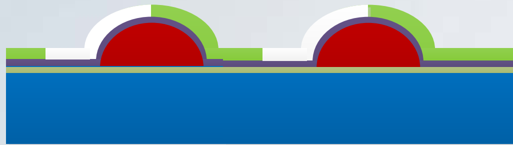

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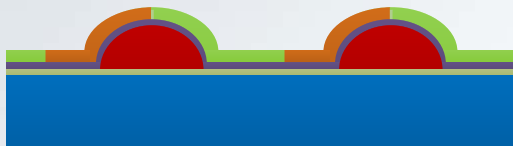

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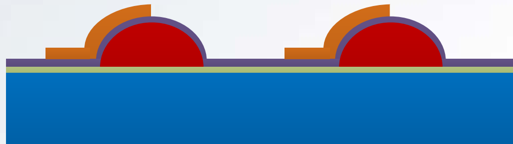

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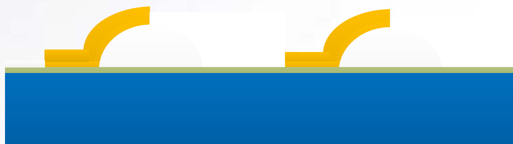

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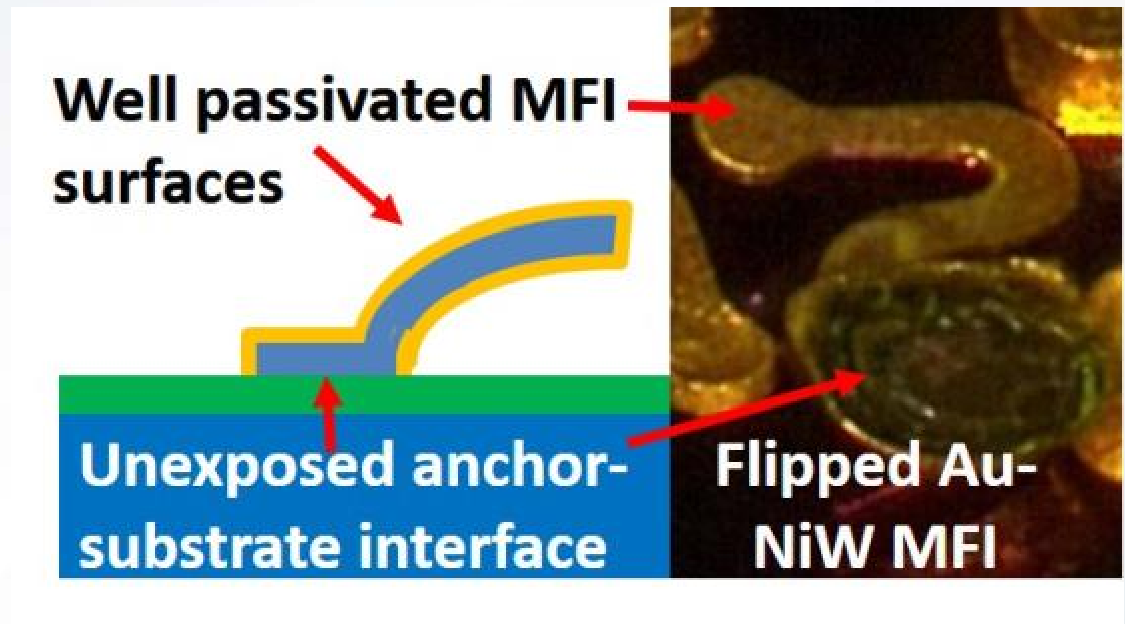

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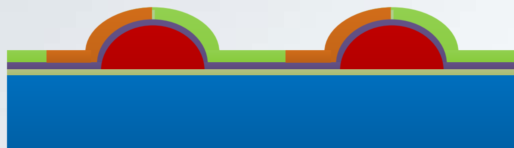
MFIs with Highly Scalable Pitch

F. Electroplating Mold Patterning



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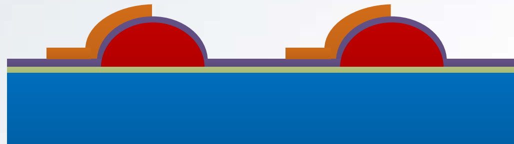

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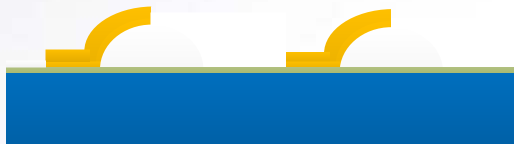

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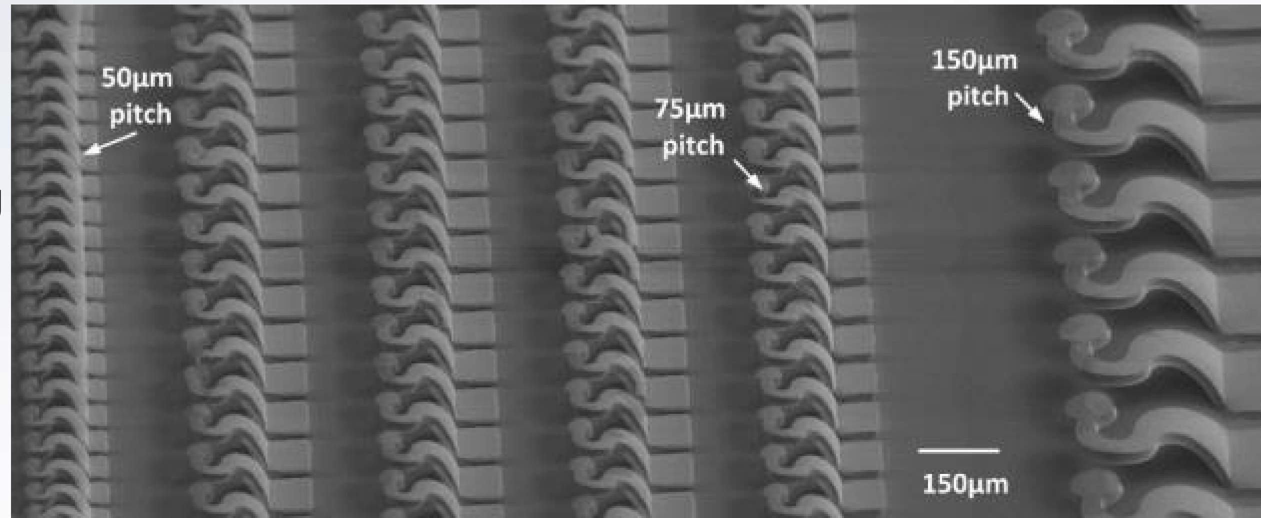

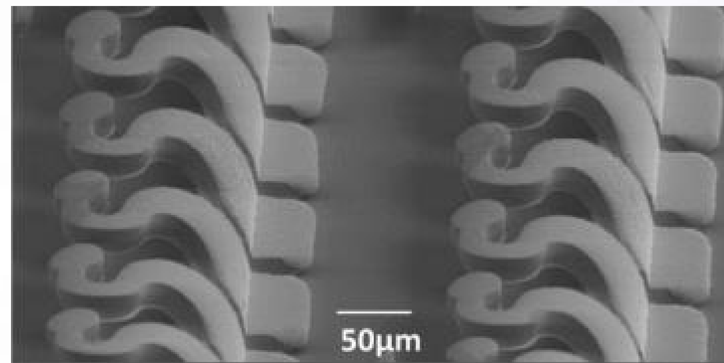

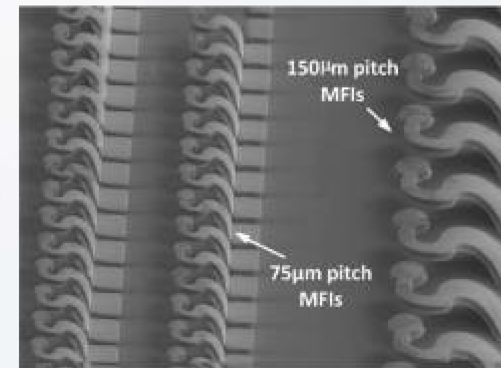

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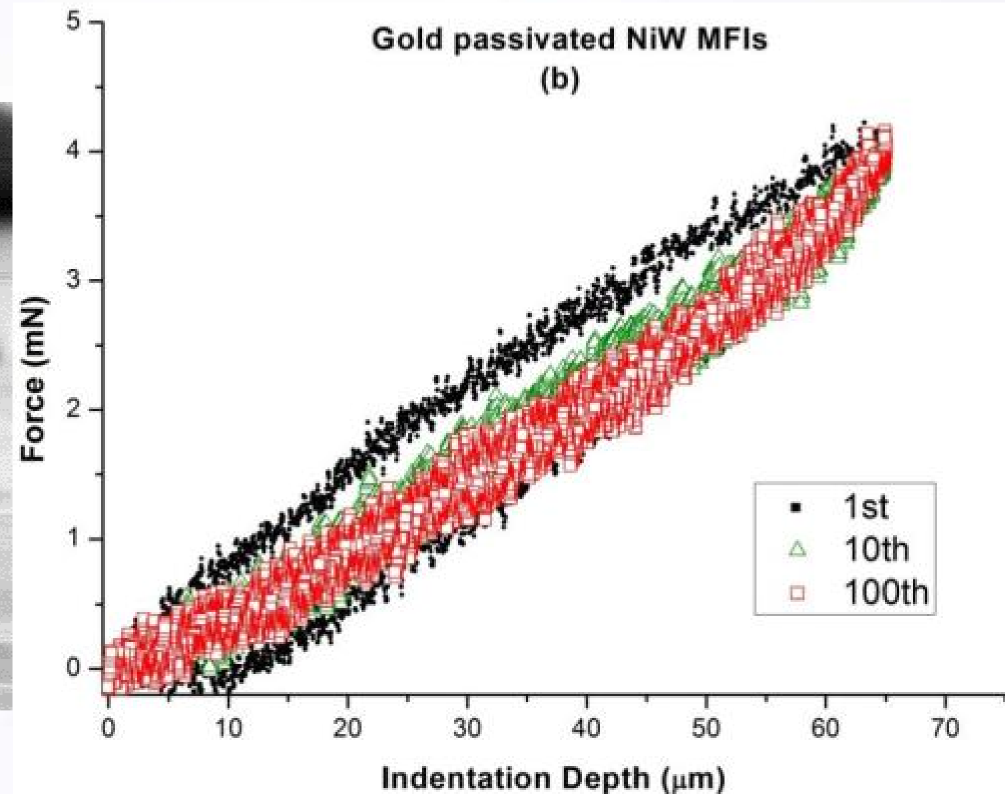
Mechanical Characterization

- Indentation test results show the Au-NiW MFIs have up to 65 µm vertical range of motion



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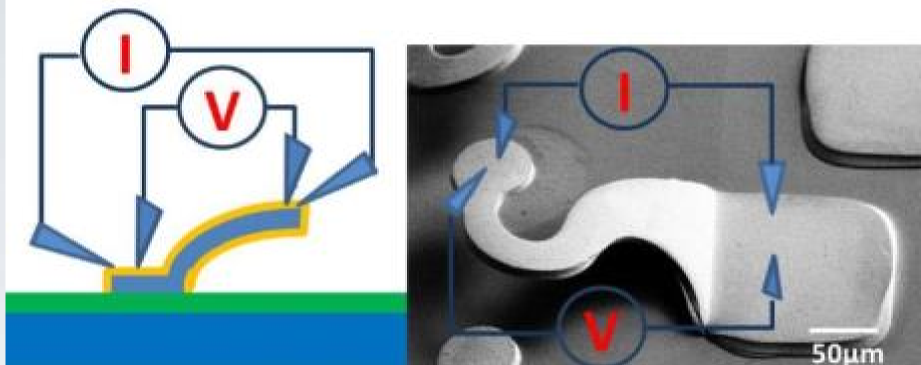
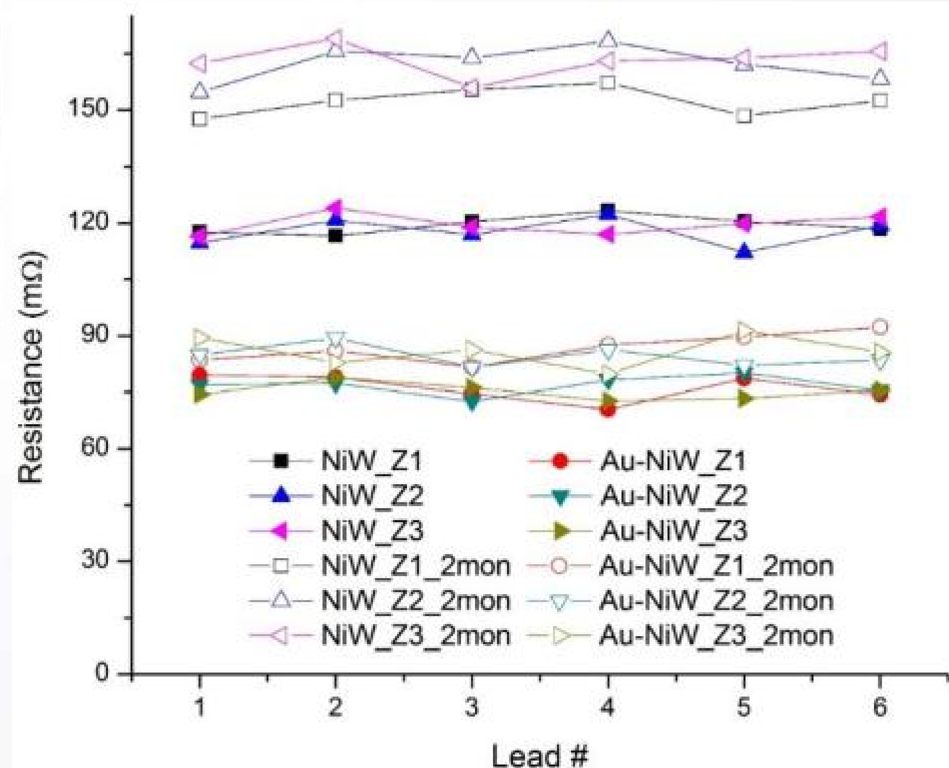
Electrical Characterization

- Four-point resistance of Au-NiW MFIs was performed on probing station
- The electrical property of Au-NiW MFIs is maintained by the gold passivation layer.

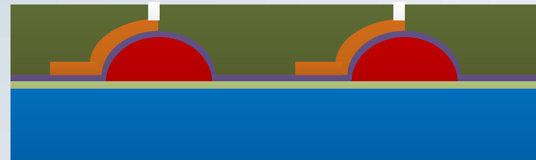


ELECTRICAL RESISTANCE MEASUREMENT FOR NIW MFIS

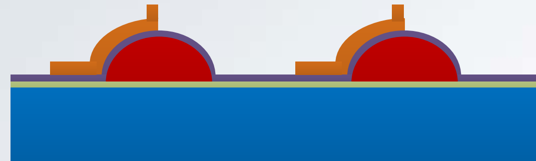
	Zone1(mΩ)		Zone 2(mΩ)		Zone 3(mΩ)	
	No Au	Au	No Au	Au	No Au	Au
t=0	119.5	76.1	117.7	76.7	119.6	75.2
t=2 months	152.3	86.7	162.2	84.6	163.3	85.8



MFIs with Truncated Cone Tip

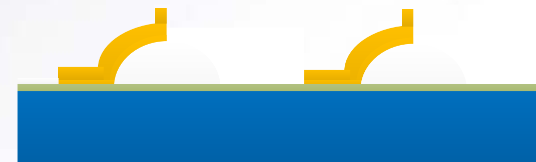


H. Tip Mold Patterning

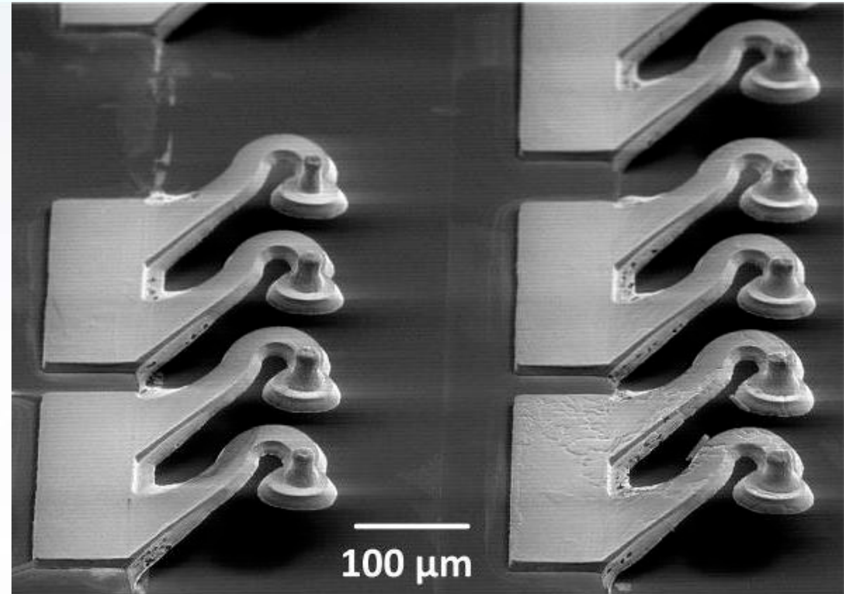


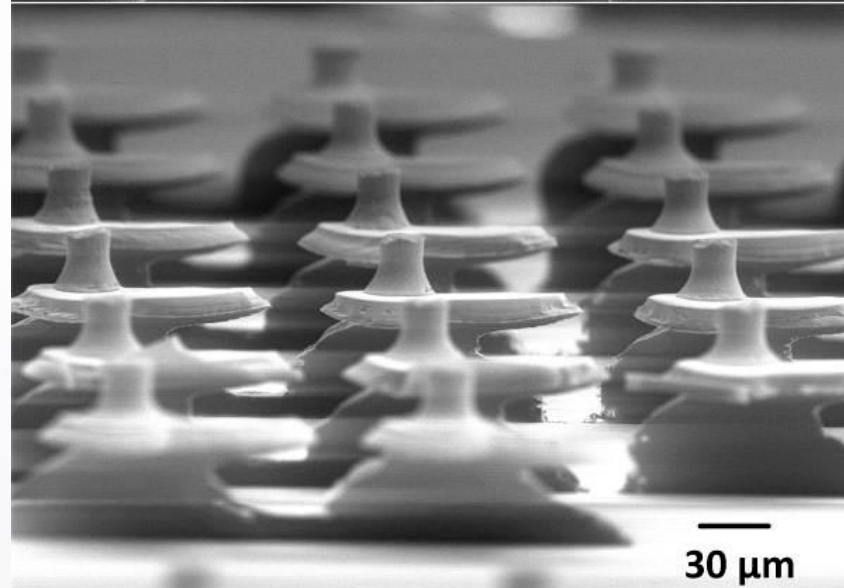
I. Tip Formation

J. MFI releasing



K. Gold Passivation

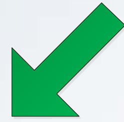


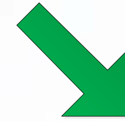


MFIs Assisted Temporary Assembly

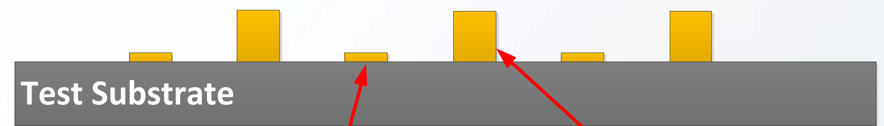
Chip/Interposer with MFIs

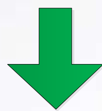
Rematable assembly on planar surface

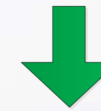




Robust assembly on non-planar surface







Chip/Interposer with MFIs

Test Substrate

Chip/Interposer with MFIs

Test Substrate

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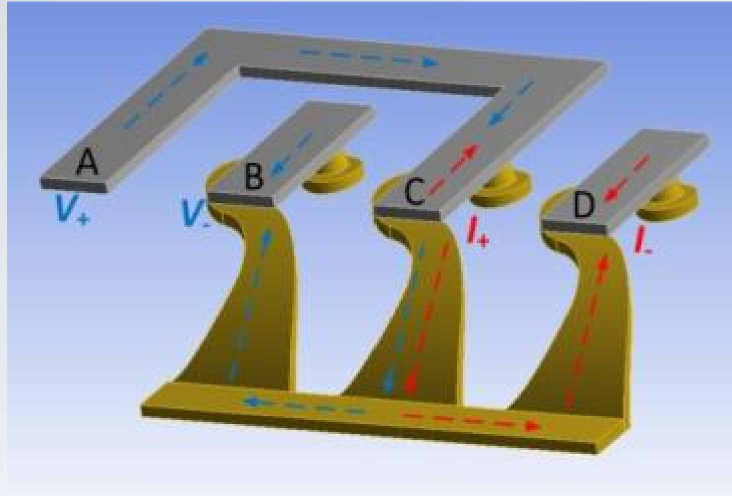
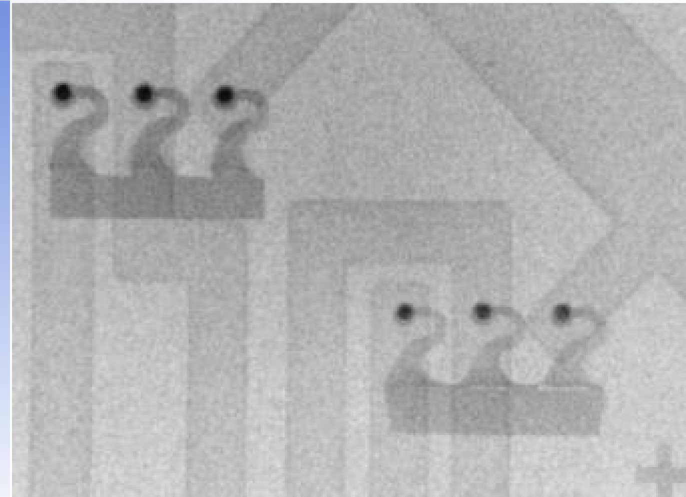
Four-Point Resistance Measurement



Four-point resistance test structure



X-ray imaging is used for alignment check

RESISTANCE CHARACTERIZATION FOR REMATABLE ASSEMBLY

	Average Resistance (mΩ)	Standard Deviation (mΩ)
After 1st assembly	103.21	4.06
After 10th assembly	105.99	4.40

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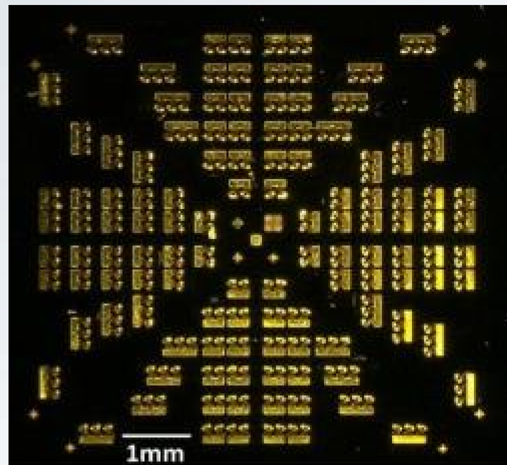
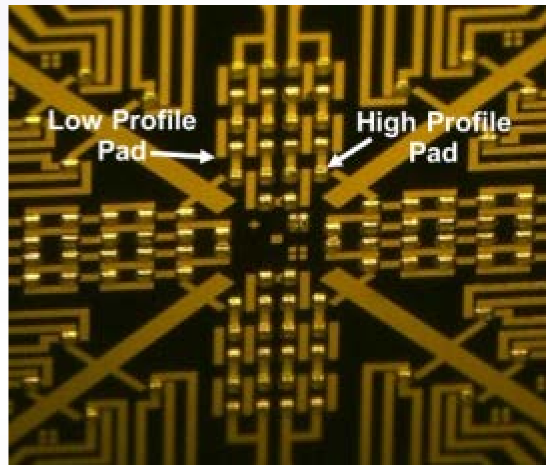
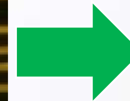
Assembled on Non-planar Substrate

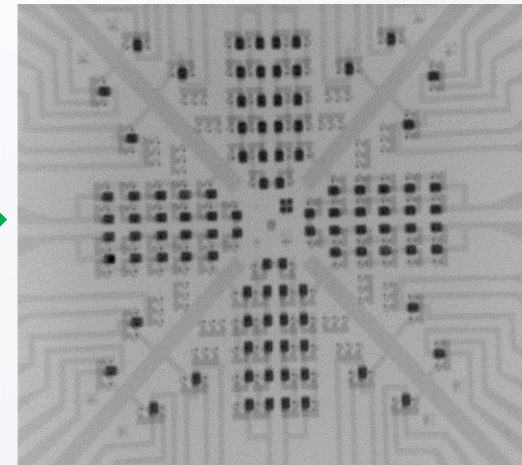
Chip/Interposer with MFIs

Test Substrate









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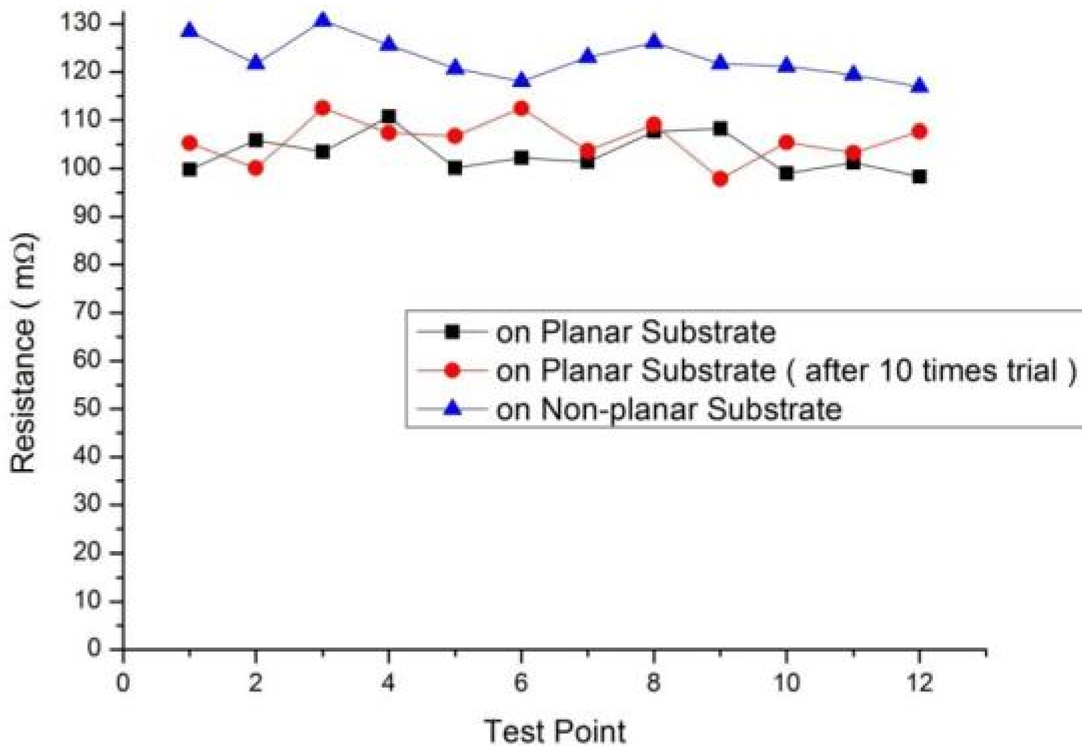
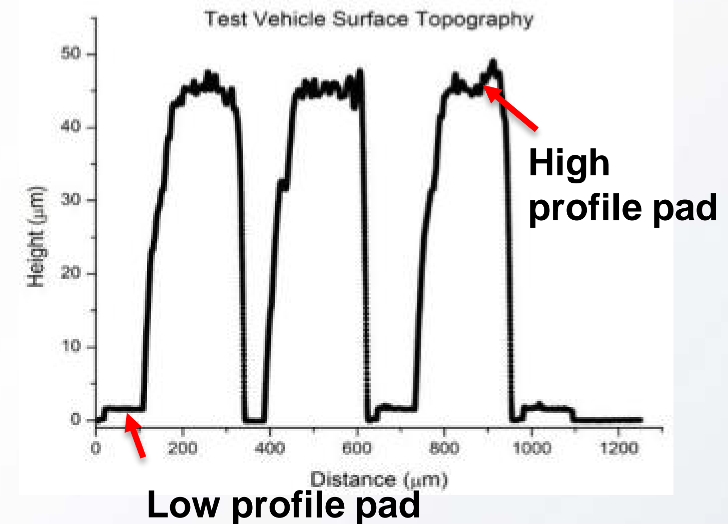
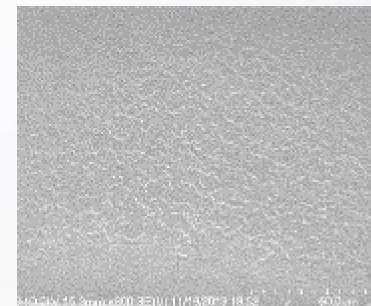
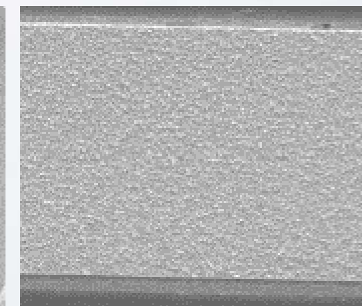
Assembled on Non-planar Substrate









High profile pad

Low profile pad

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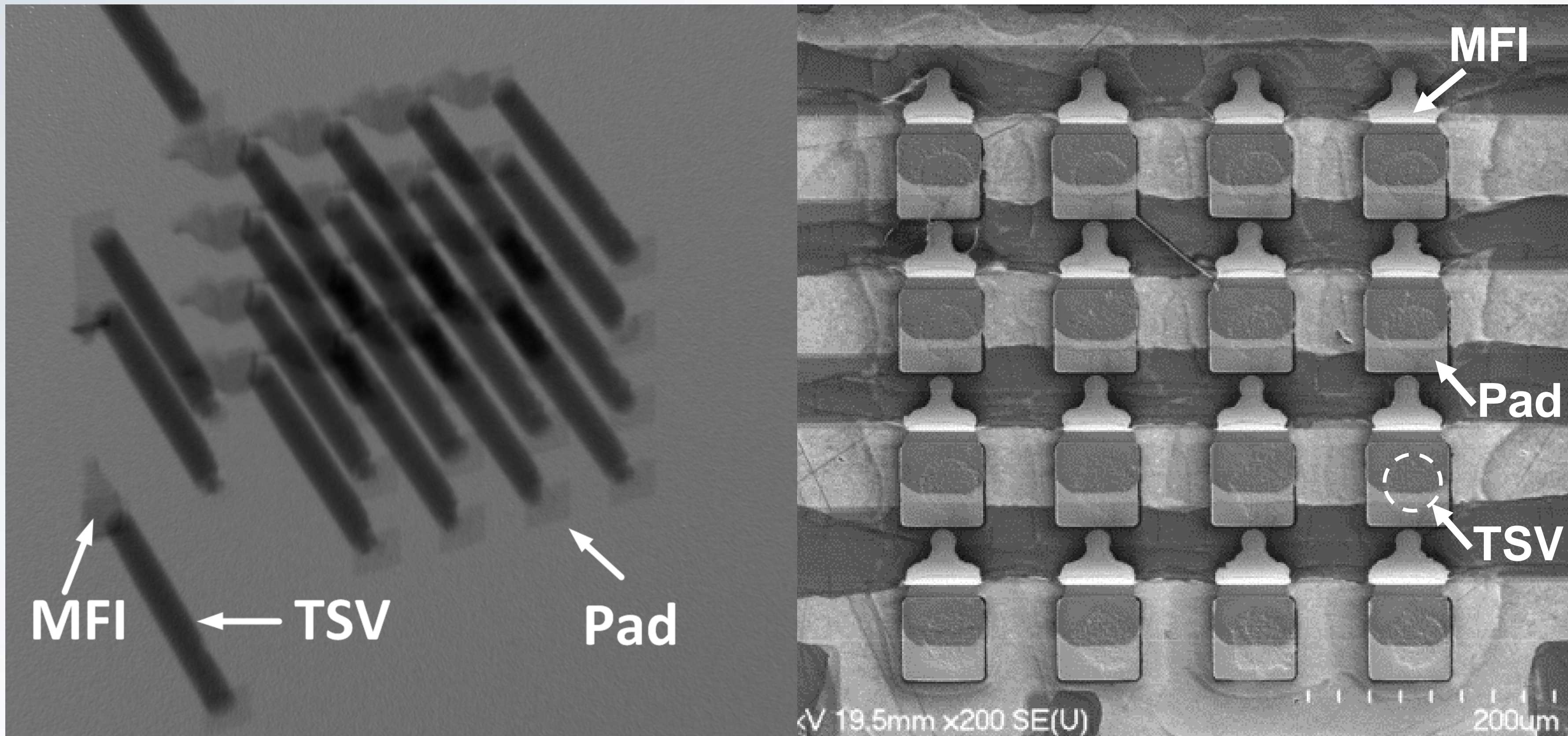
MFI/TSV Integration



MFI/TSV Integration

- DC Measurement
  - $Resistance_{MFI+TSV} = 76\ m\Omega$

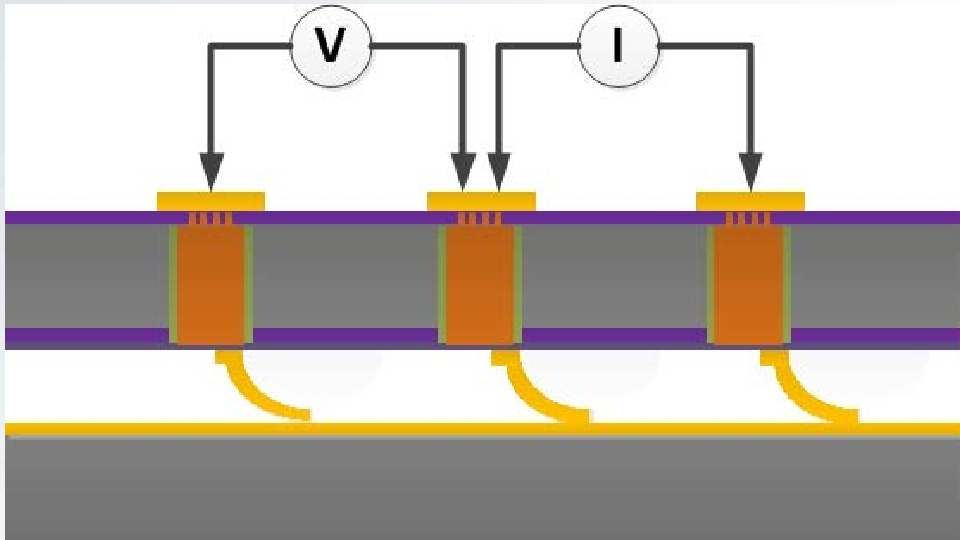


Table 12: Dimensions of TSV/MFI array

	Demension	Value (μm)
TSV	Diameter	50
	Height	300
	Pitch	100
MFI	Vertical height	30
	Thickness	5
	Pitch	100

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Advanced Cooling

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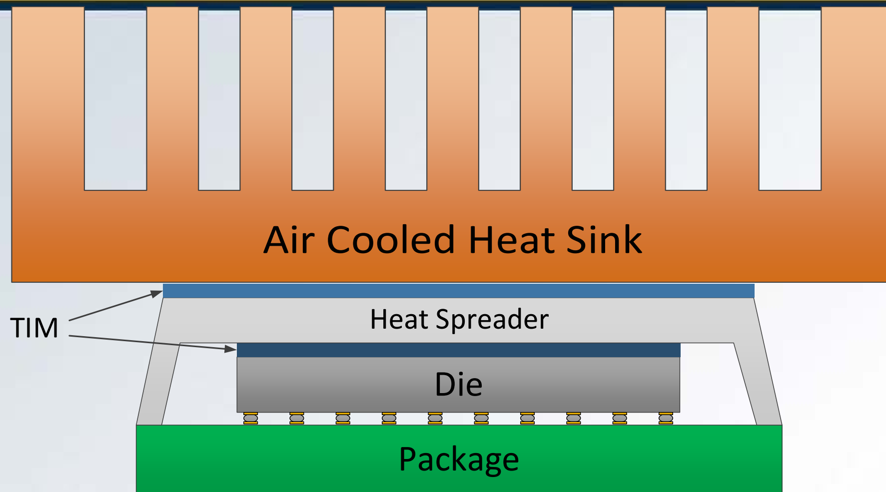
Microelectronic Cooling



- Power limit ~100W/cm^2
- Large Footprint
- Incompatible with high power 3DIC

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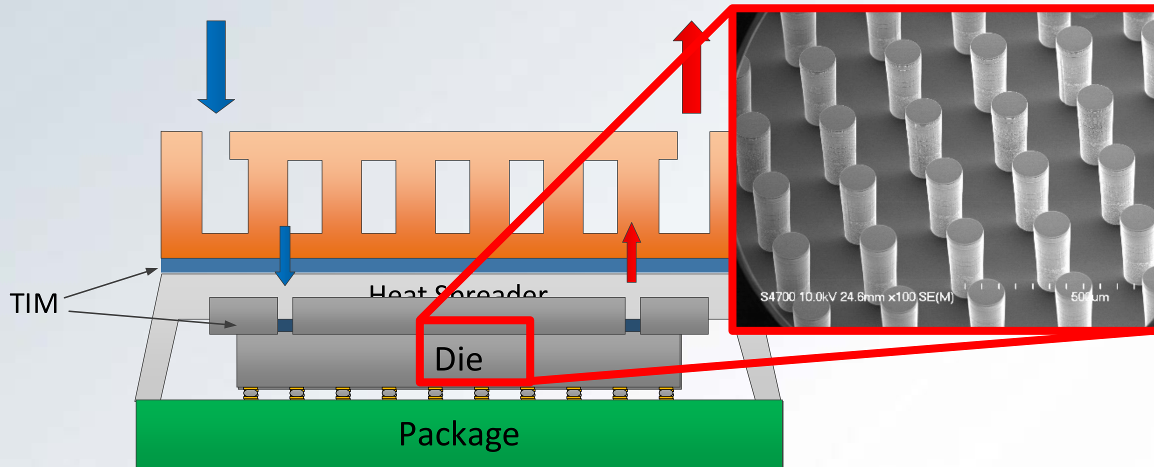
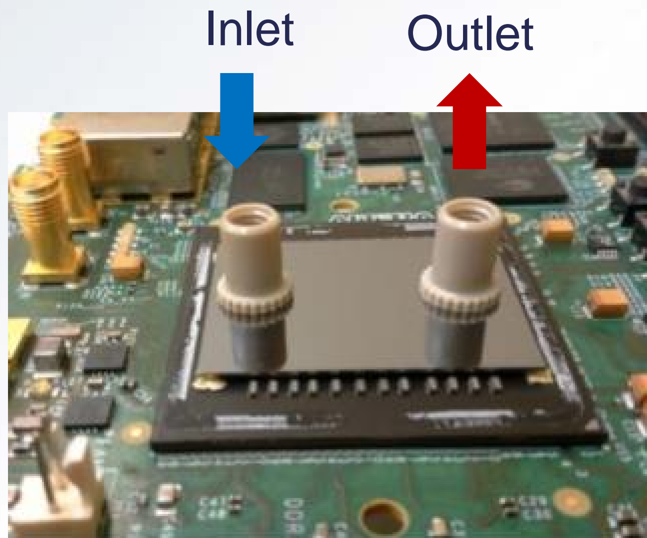
Monolithic Microfluidic Heat Sink in IC



Etched FPGA Backside

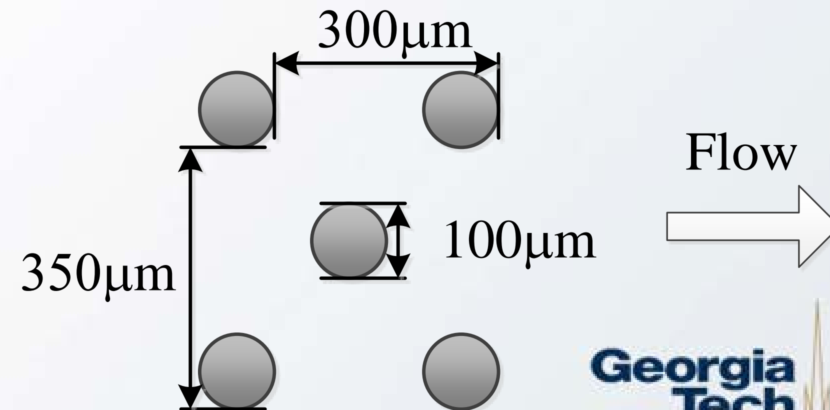
Inlet

Outlet



Assembled Microfluidic-cooled FPGA

Micropin-fin Dimensions



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Demo with Pulse Compression Core

- **A functional design for Stratix V DSP kit**
  - Multiple independent Pulse Compression test units. The number of active cores to be enabled is run time configurable
- **Design optimized for streaming data and low latency**

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Microfluidic Cooled FPGA Performance

Baseline Design

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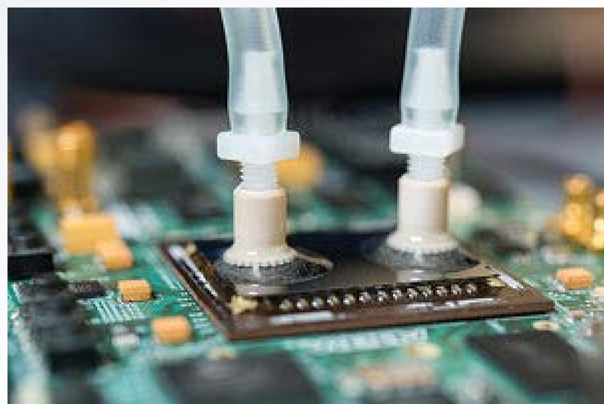


Cores	Fluidic FPGA Power (W)	Air FPGA Power (W)	Fluidic FPGA Temp (°C)	Air FPGA Temp (°C)	Throughput GOP/s
0	13.2	13.7	21-22	43	0
1	15.4	16.0	21-23	46	104
2	17.6	18.3	22-23	49	208
3	19.8	20.5	22-23	51	311
4	21.9	22.8	22-23	53	415
5	24.0	25.1	22-23	59	519
6	26.2	27.5	22-23	59	623
7	28.3	29.8	22-24	61*	727
8	30.4	--	22-24	--	830
9	32.4	--	22-24	--	934

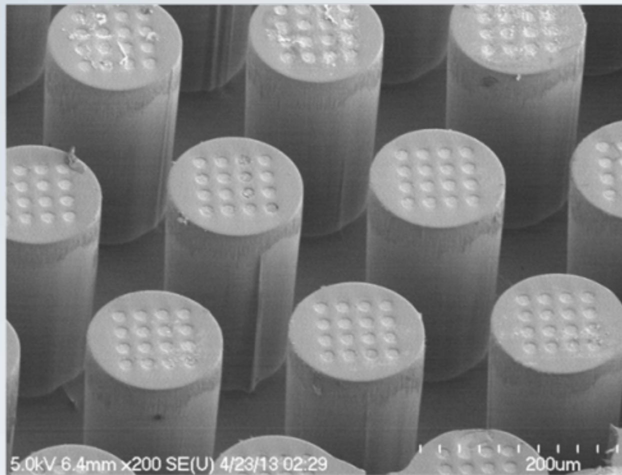
1.5x of Baseline Compute Capability

Power	Flow Rate	Die Temp
29W	147mL/min	**24°C**

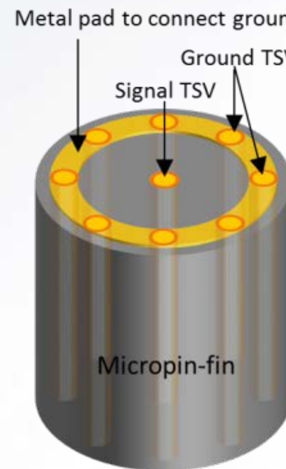
Junction-to-ambient R_{th} ≈ 0.08°C/W

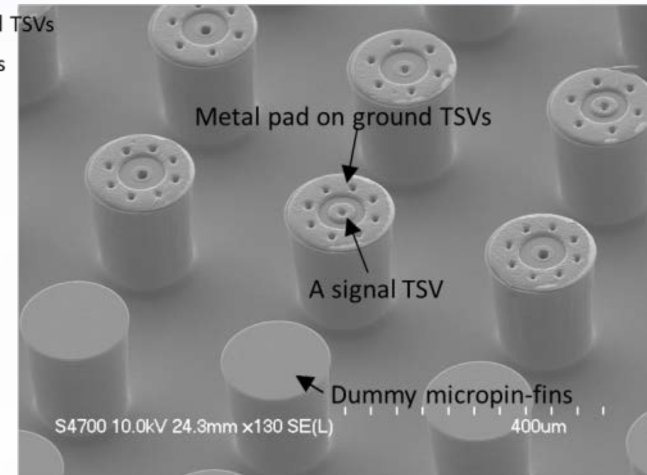
High-Aspect Ratio TSVs Integrated Within a Micropin-fin Heat Sink (TSV AR = 23:1)

Multiple TSVs in a micropinfin heat sink



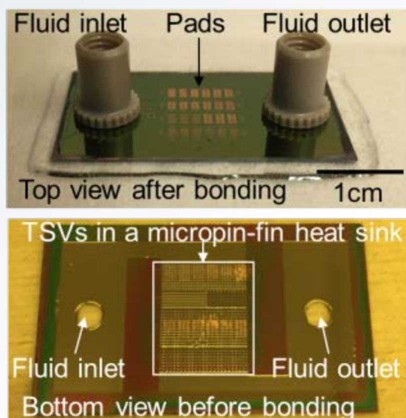
Coaxial TSVs in a micropinfin heat sink

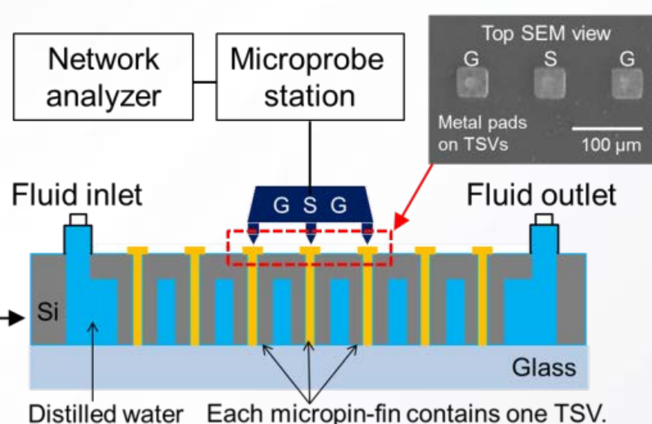




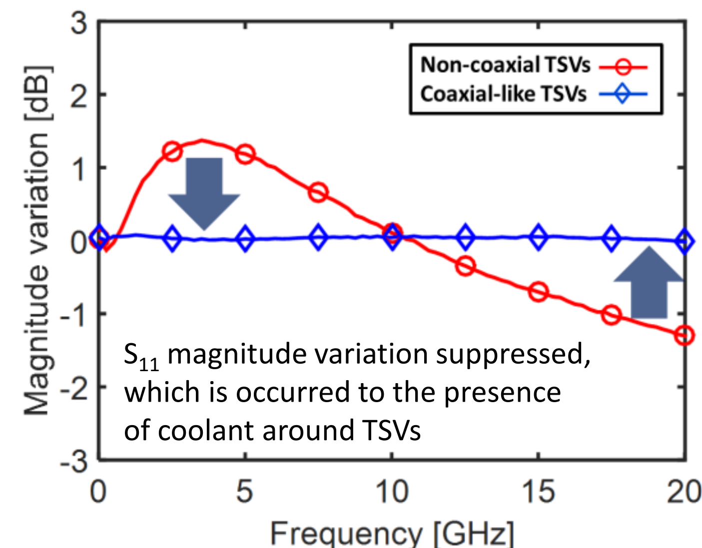
RF measurements setup with the testbed

Fabricated & assembled testbed





RF measurement results



Thank you!

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