Georgia Tech Packaging Research Center
College of Engineering

System Scaling
for
New Era of Automotive Electronics: A Large-scale Industry Consortium at Georgia Tech
in Partnership with
Global Supply-Chain Mfg and OEMs

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Outline

- System Scaling as a Microelectronics Technology Frontier
- New Era of Automotive Electronics (NAE)
- Industry Consortium at GT
  - Faculty
  - Industry Partners
  - Facilities
  - Technical Programs
    - Computing and Communication Electronics
    - Sensing Electronics
    - High Power and High Temperature Electronics
- Summary

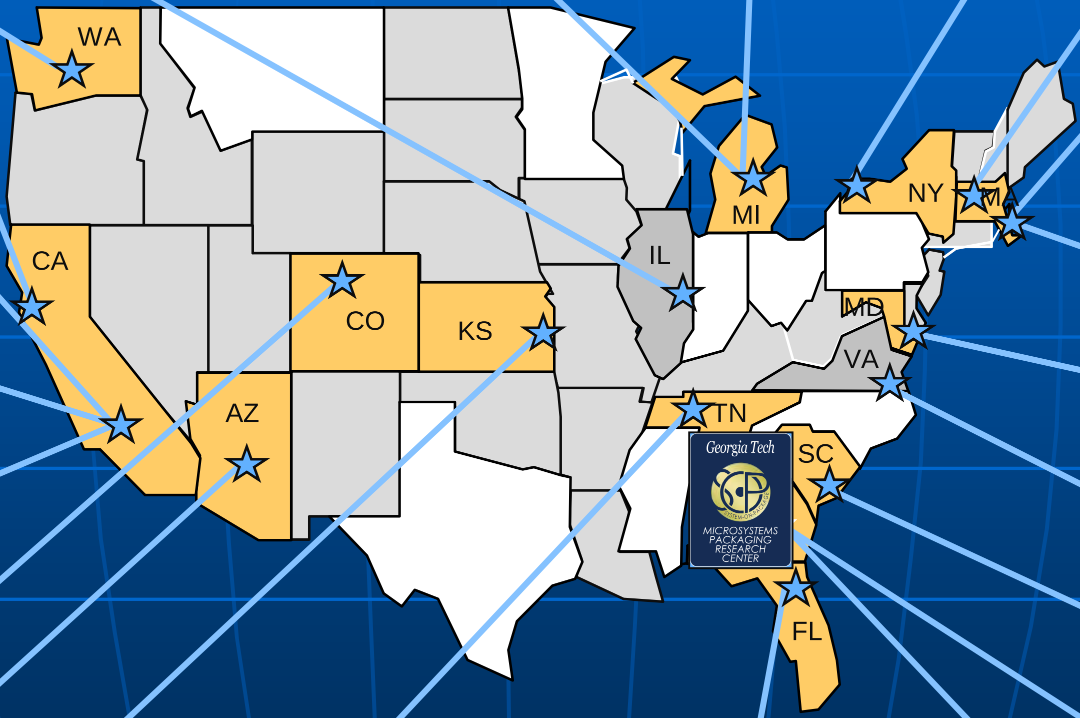
SYSTEM SCALING AS A MICROELECTRONICS SYSTEMS TECHNOLOGY FRONTIER

Georgia Tech PRC Center started with a Vision For Digital Convergence by SOP Concept in 1993

Digital + Analog + RF + Optical + Sensors

- Computing/Internet
- Digital Audio
- Digital Imaging/Video
- Cellular/Wireless
- GPS/Satellite
- Sensors
- And, of course, timekeeping!

GT PRC Started with the 1st NSF ERC in US in System Scaling and Integration (SSI)



Univ. of Illinois
Mid-America Earthquake Center

Univ. of Michigan
Reconfigurable Manufacturing Systems

Univ. of Michigan
Wireless Integrated MicroSystems

SUNY Buffalo
Multidisciplinary Center for Earthquake Eng. Research

Univ. of Washington
Engineered Biomaterials

UC, Berkeley
Pacific Earthquake Engineering Research Center

Univ. of Southern California
Biomimetic MicroElectronic Systems

California Inst. of Technology
Neuromorphic Systems Engineering

Univ. of Southern California
Integrated Media Systems

Colorado State Univ.
ERC for Extreme Ultraviolet Science & Technology

Univ. of Arizona
Environmentally Benign Semiconductor Manufacturing

Univ. of Massachusetts
Collaborative Adaptive Sensing of the Atmosphere

MIT
Biotechnology Process Engineering Center

Northeastern University
Subsurface Sensing & Imaging Systems

Johns Hopkins University
Computer-Integrated Surgical Systems & Technology

Virginia Polytechnic Institute
Power Electronic Systems

Clemson University
Adv. Engineering of Fibers & Films

Georgia Inst. of Technology
Packaging Research Center

Univ. of Kansas
Center for Environmentally Beneficial Catalysis

Vanderbilt University
Bioengineering Educational Technology

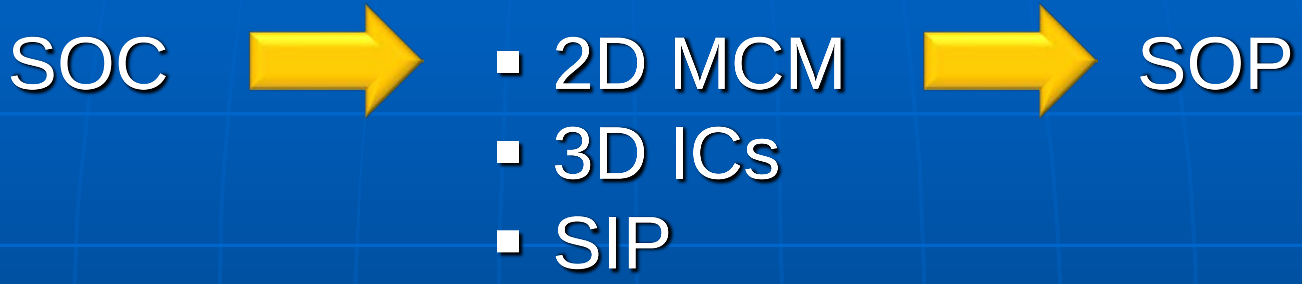
Univ. of Florida
Particle Science & Technology

Georgia Inst. of Technology
Center for the Engineering of Living Tissue

SOP @ PRC
“Package is the System”

System: Convergent Computing, Communication, Consumer & Biomedical

IC-Package Trend



SOC

- 2D MCM
- 3D ICs
- SIP

SOP

Outcomes of Georgia Tech's NSF ERC & Model

Research & Infrastructure

- System Scaling for Smart phones
- 2000 ground-breaking publications
- 20 Faculty and 150 grad students
- 100 Best Paper Awards
- $40M SOA Laboratories

Education

- Interdisciplinary Engineers
    - Ph.D ~500,MS ~570,BS ~340
- Created 20 new courses
- 1st undergrad & 1st Grad. book

Disruptive Technology: System Scaling

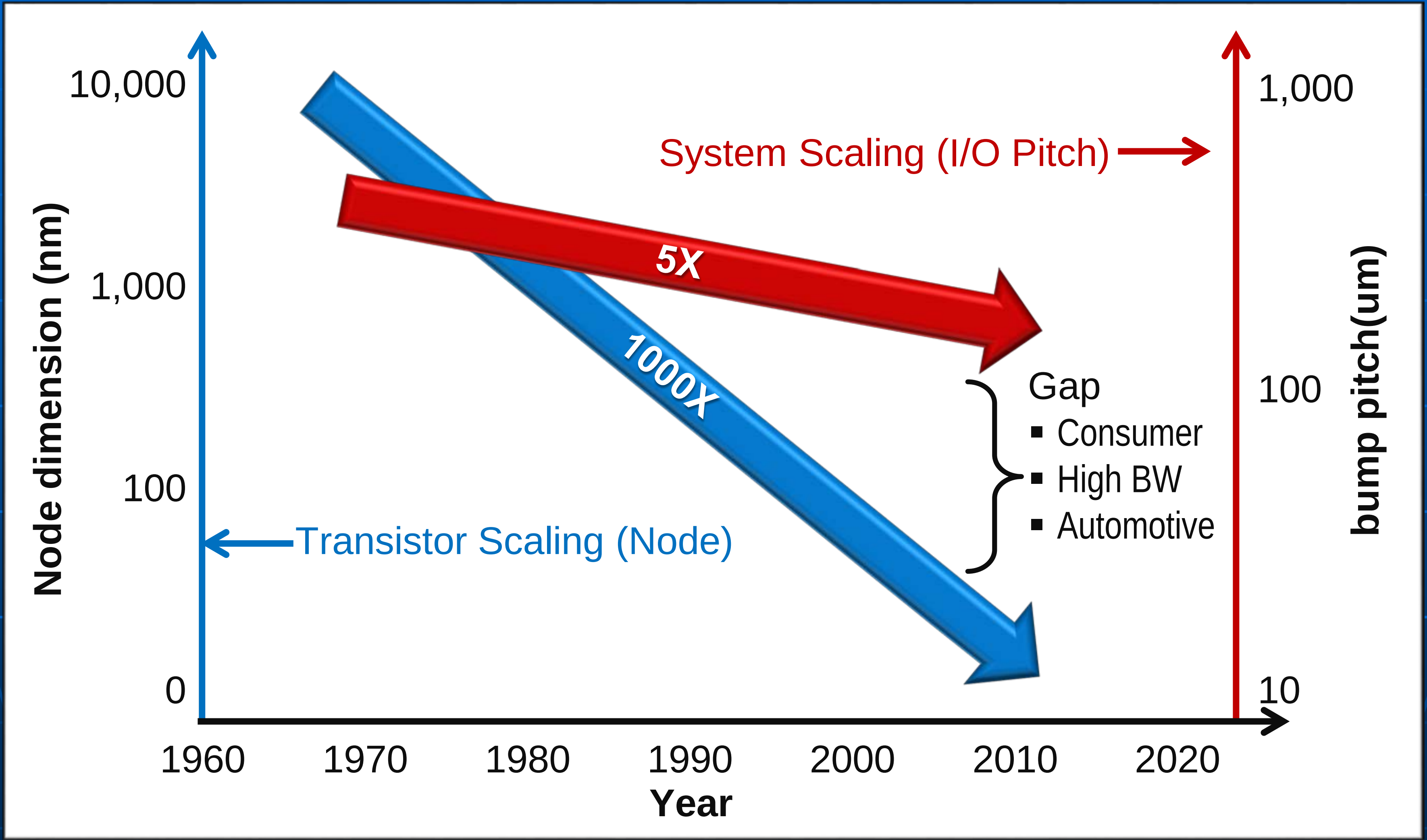
Global Industry Collaborations

- 150 US, 25 Jap., 10 Eu, 10 Korean
- 10 Spin-off and spin-in companies
- 70 Patents, and 166 IP licenses
- 97 Technology transfers

Funds Raised Economic Development

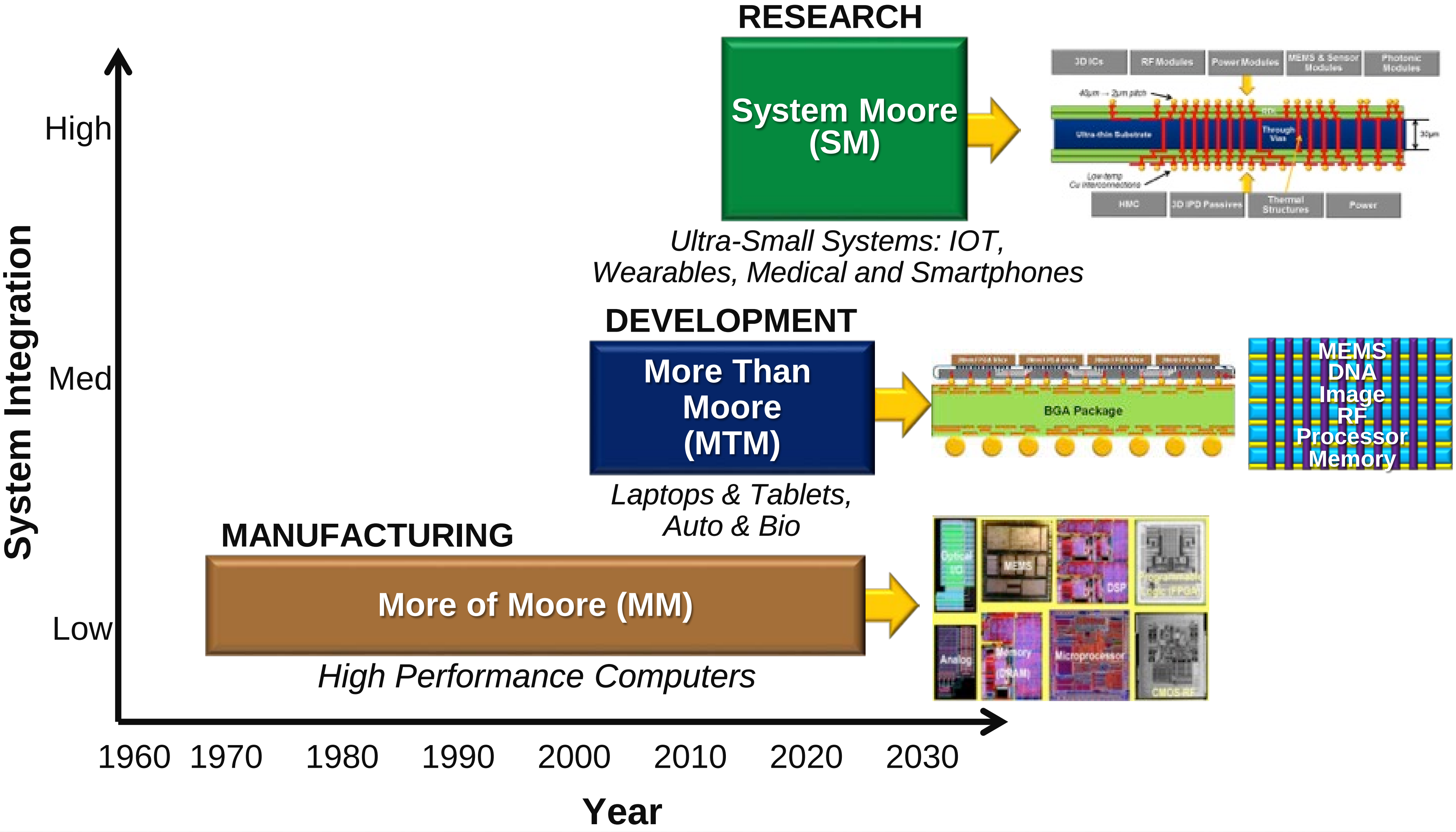
- Raised $250M for research
- $350M to State of Georgia economy

An Example of System Scaling vs. Transistor Scaling



Courtesy: S.S. Iyer, IBM

Basis of System Scaling



RESEARCH

System Moore (SM)

Ultra-Small Systems: IOT, Wearables, Medical and Smartphones

DEVELOPMENT

More Than Moore (MTM)

Laptops & Tablets, Auto & Bio

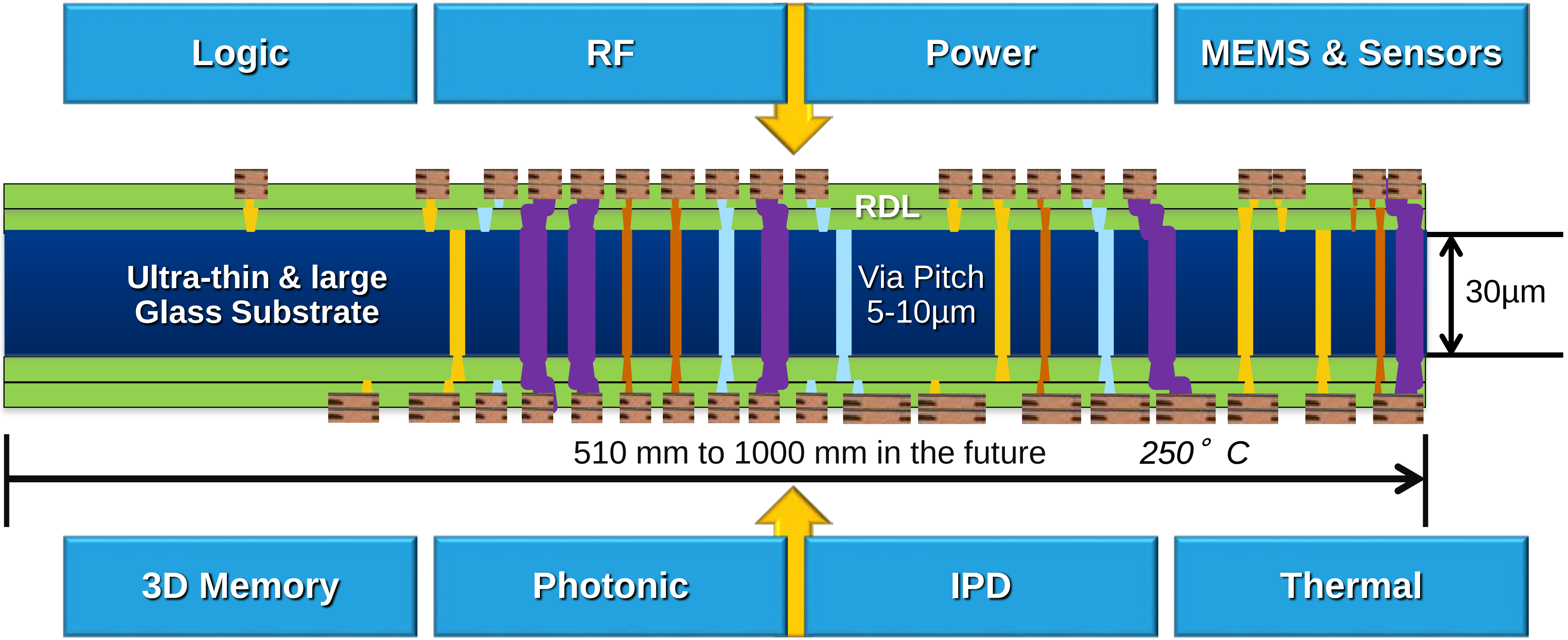
MANUFACTURING

More of Moore (MM)

High Performance Computers

3D System Package – A Fundamental Concept

1. Ultra-thin, Large, Low CTE, HT Substrates
2. Ultra-short TSV-like System Interconnects
    - Signal vias, power vias, photonic vias and Large Thermal Vias
3. Ultra Low-loss Materials & Interconnects
4. Balanced Fine-pitch RDL for Min. Warpage
5. High-temp & High-power Cu-Cu Interconnects
6. High-throughput Panel Mfg and Panel Assembly



NEW ERA OF AUTOMOTIVE ELECTRONICS (NAE)

NAE: Most Complex Electronics System

- Wireless Electronics
- Sensor Electronics
- Camera Electronics
- 4G LTE
- Digital Electronics
- MEMS and Sensors
- Power Electronics

+

- Sensing Electronics for Autonomous Driving
  - Radar, LiDAR, Cameras
- High-power and High-temp for Electric Cars
  - GaN, SiC devices
  - Metal-insulators
- Healthcare Electronics
- Etc …

New Era of Automotive Electronics (NAE)
is the Most Complex Electronic System

Global Challenges in New Era of Electronics

- New Technologies
- Educated Workforce
- Global Manufacturing Supply-chain
- Component Integration
- System Assembly
- Roadmaps
- Standards

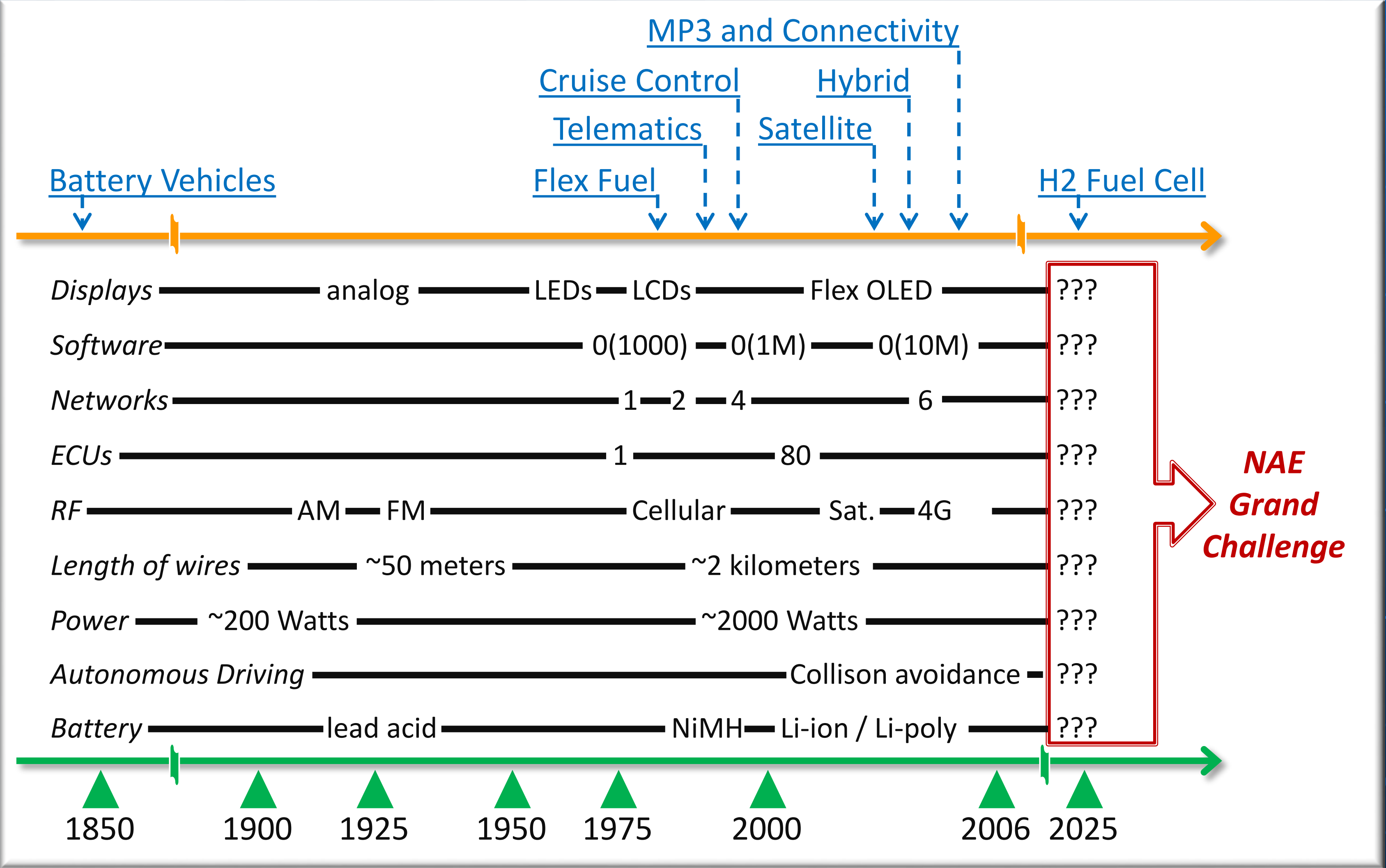
3 Main Reasons for NAE

1. Reducing Human Fatalities
    - 94% of 33,000 Deaths in the U.S., and 1.3M globally due to human error
2. Improving Driving – Energy Efficiency
3. Improving Human Productivity

Many, Many more

Mercedes-Benz F 015 Luxury in Motion Research

Grand Challenges in Automotive Electronics (Ford)



MP3 and Connectivity
Cruise Control
Hybrid
Telematics
Satellite
Battery Vehicles
Flex Fuel
H2 Fuel Cell

Displays — analog — LEDs — LCDs — Flex OLED — ???
Software — 0(1000) — 0(1M) — 0(10M) — ???
Networks — 1 — 2 — 4 — 6 — ???
ECUs — 1 — 80 — ???
RF — AM — FM — Cellular — Sat. — 4G — ???
Length of wires — ~50 meters — ~2 kilometers — ???
Power — ~200 Watts — ~2000 Watts — ???
Autonomous Driving — Collison avoidance — ???
Battery — lead acid — NiMH — Li-ion / Li-poly — ???

NAE Grand Challenge

NAE: Ultimate Electronic System Opportunity

Computing & Communication Electronics

- 5G
- High Bandwidth
  - Electronics
  - Photonics

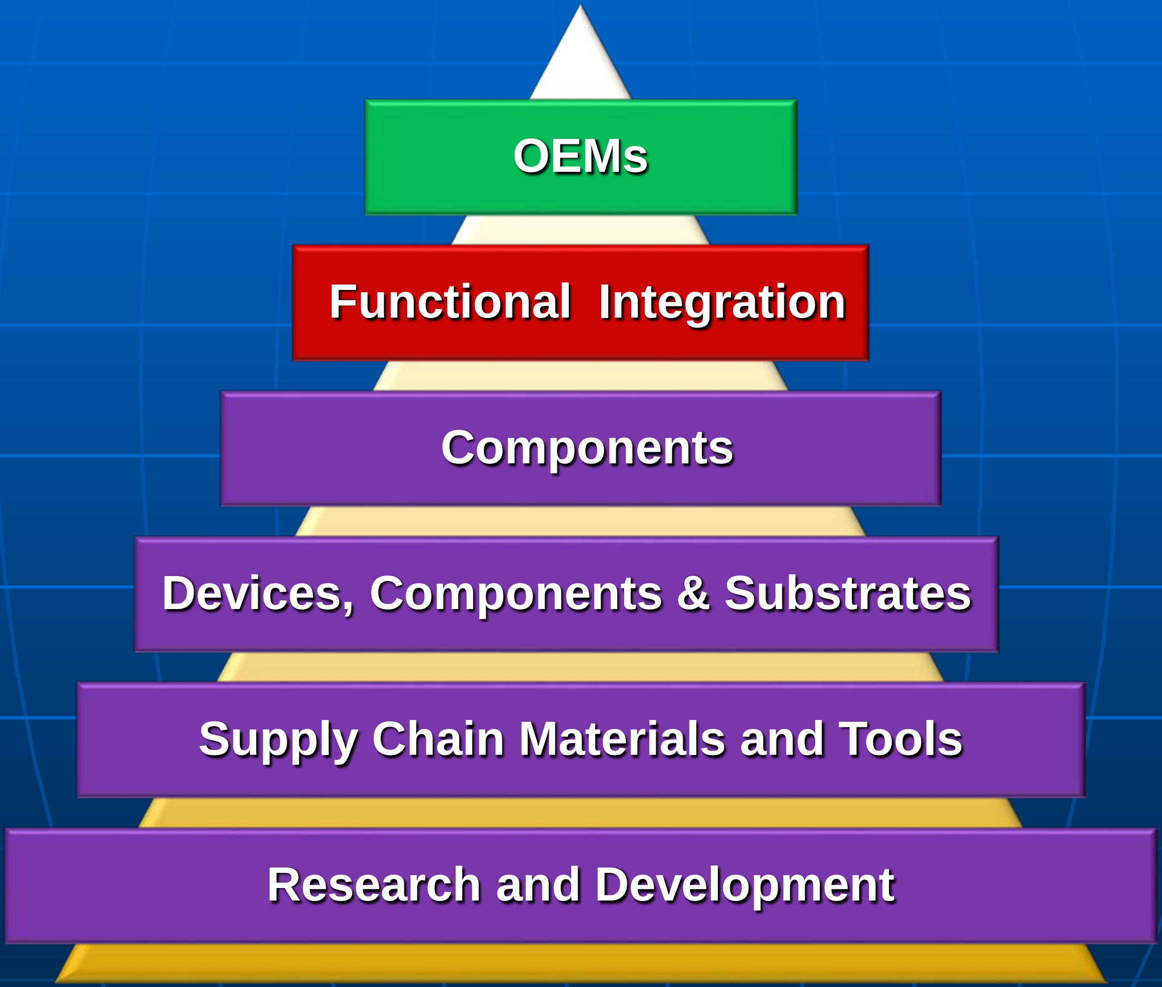
Sensing Electronics

- Radar
- Lidar
- Cameras

High Power & High Temp Electronics

- Batteries
- Drive Train
- Power Distribution &
- Power Conversion

Global Ecosystem for NAE – From R&D to System Integration



OEMs

Functional Integration

Components

Devices, Components & Substrates

Supply Chain Materials and Tools

Research and Development

INDUSTRY CONSORTIUM AT GT

Georgia Tech Industry Consortium

Uniqueness of GT PRC

Technical Strategy

Faculty Expertise

300mm Cleanroom Pilot Facility

Industry Partnership

State of Micro-electronics

Georgia Tech
SYSTEM-ON-PACKAGE
MICROSYSTEMS PACKAGING RESEARCH CENTER

Automotive Programs in the South East

Organization	Emphasis
NTRC – National Transportation Research Center, Oak Ridge, TN	Improving fuel economy, reducing emissions and addressing transportation systems issues
CTR – Center for Transportation Research, Univ. of Tennessee, Knoxville	Conduct research; develop expertise; serve transportation research, service and training needs
CU-ICAR – Clemson Univ. - International Center for Automotive Research	Campus is an automotive ecosystem that helps companies make connections and build relationships
CAVE-3 – Center for Advanced Vehicle and Extreme Environmental Electronics, Auburn Univ.	New technologies for packaging electronics with emphasis on cost, harsh environment and reliability
CAVT – Center for Advanced Vehicle Technologies, Univ. of Alabama, Tuscaloosa	Powertrains, energy storage, materials and manufacturing and other automotive electronics
CAVS – Center for Advance Vehicular Systems, Mississippi St. Univ., Starkville	Engineering solutions for design, technology, production, and infrastructure for sustainable mobility
ATDC – Advanced Technology Development Center, EI2, Georgia Tech	Startup incubator that helps technology entrepreneurs in Georgia launch and grow successful companies
Venture Lab, EI2, Georgia Tech	Ranked #2 University based incubator in the world
NCTSPM – National Center for Transportation Systems Productivity and Management; Ga Tech, FL International Univ, Univ. Central FL, Univ. Alabama Birmingham	Tier 1 University Transportation Center (UTC) that conducts transportation related research in the areas of safety, state-of-good-repair, and economic competitiveness

Uniqueness of GT Consortium

- Leading-edge, precompetitive, 100 global researchers, developers, manufacturers and OEMS
- Co-development by all 50+ companies
- Device-Package synergy and system integration
- Basic research by Ph.D and MS students
- Integration and prototype research by GRAs, company engineers and GT research faculty
- Long-term roadmap with 2 year deliverables

Georgia Tech Faculty Expertise

Design


Prof. Graham
Thermal


Prof. Joshi
Thermal


Prof. Sitaraman
Mechanical


Prof. Chang
Optical


Prof. Tentzeris
RF 5G

Devices: SiGe, GaN, MEMS and Sensors


Prof. Cressler
SiGe


Prof. Dupuis
GaN


Prof. Shen
GaN


Prof. Hesketh
Sensors

Materials


Prof. Losego
Dielectrics


Prof. Wong
Encapsulants

Substrates


Dr. Sundaram
Glass

Passives


Dr. Raj
RF & Power

I&A


Prof. Antoniou
Sintered Cu


Dr. Smet
Non-solder

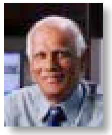
Lidar


Dr. Tuell
Modeling & Design

Camera


Prof. Wolter
Fabrication

System Integration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Technology Integration

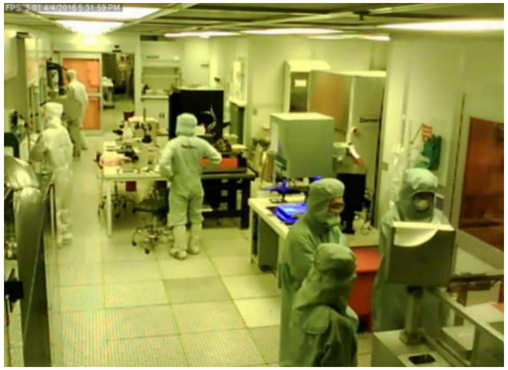
Software


Dr. Christensen
Software

300mm Cleanroom Pilot Facility and Labs

Plating Facility

Substrate Cleanroom



Assembly Facility

Environmental Testing

Shared User Labs

Partnership with Tool Companies

Disco Dicing Saw and Planer

XYZTEC Bond Tester

Ushio Projection Lithography

ESI Cornerstone Laser

MKS Ozone Cleaner

K&S APAMA Bonder

Global Industry Co-development Consortium at GT PRC

UNITED STATES

- 🟩 Brewer Sci - Polymers
- 🟩 Corning – Glass
- 🟫 Applied Materials – PVD, CVD Tools
- 🟫 Coherent – Laser
- 🟫 ESI – Laser
- 🟫 K&S – TCB Bonder
- 🟫 MKS – Plasma Etching
- 🟫 Tango – PVD Tools
- 🟫 Veeco - Cleaning
- 🟥 QualiTau – Assembly
- 🟦 AVX – Passives
- 🟦 Ciena – Opto
- 🟦 Global Foundries
- 🟦 Intel – Digital
- 🟦 Qualcomm – All
- 🟦 TE – Opto
- 🟦 TI – Passives

EUROPE

- 🟩 HC Starck – Capacitors
- 🟩 Schott – Glass
- 🟫 Atotech – Plating
- 🟫 Suss – Laser Via
- 🟫 Xyztec – Assembly
- 🟦 TDK-Epcos – RF

ASIA

- 🟫 Orbotech – Metrology

CHINA

- 🟥 JCET – Bumping

KOREA

- 🟦 Gigalane – RF

TAIWAN

- 🟪 Unimicron – 2.5D
- 🟥 ASE – Assembly
- 🟦 TSMC – User

JAPAN

- 🟩 Ajinomoto – Dry Film
- 🟩 Asahi Glass – Glass
- 🟩 MGC – Laminates
- 🟩 TOK – Photopolymer
- 🟫 Asahi Glass – TPV
- 🟫 Disco – Dicing
- 🟫 Mitsubishi Electric – Laser
- 🟫 Ushio – Lithography
- 🟪 NGK/NTK – 2.5D
- 🟪 Shinko – 2.5D
- 🟥 Namics – Underfill

🟩 *Materials*	🟫 *Tools*	🟪 *Substrates*	🟥 *Assembly*	🟦 *Users*

Additional Recent Industry Interest

UNITED STATES	EUROPE	KOREA	JAPAN
AMD	Audi	Samsung	FujiFilm
Dow	Bosch		Ibiden
Finisar	Continental		Nitto Denko
IDT	Hella		Renesas
Linear	Heraeus		Rohm
On-Semi	Infineon		WALTS
Rodgers	Thales		
Rudolph	Valeo		
Savansys	Volkswagen		
Stellar			
USCI			
Veeco			

GT PRC 2016 Industry Consortia Members

Fundamental Challenges & Trends in Electronics

ICs

- IC < 14nm: no cost
- Front end: leakage
- Back end: RC delay
- Split SOC inevitable

***Trend*:**

- 2.5D Si Interposer
- 2.5D Glass BGA (GT)

Device Packaging

- Digital: Organic, Si
- RF: LTCC & laminate
- Power: embedded fanout
- Bulky and expensive

***Trend*:**

- WLFO
- PFO: Glass by GT

Systems Packaging

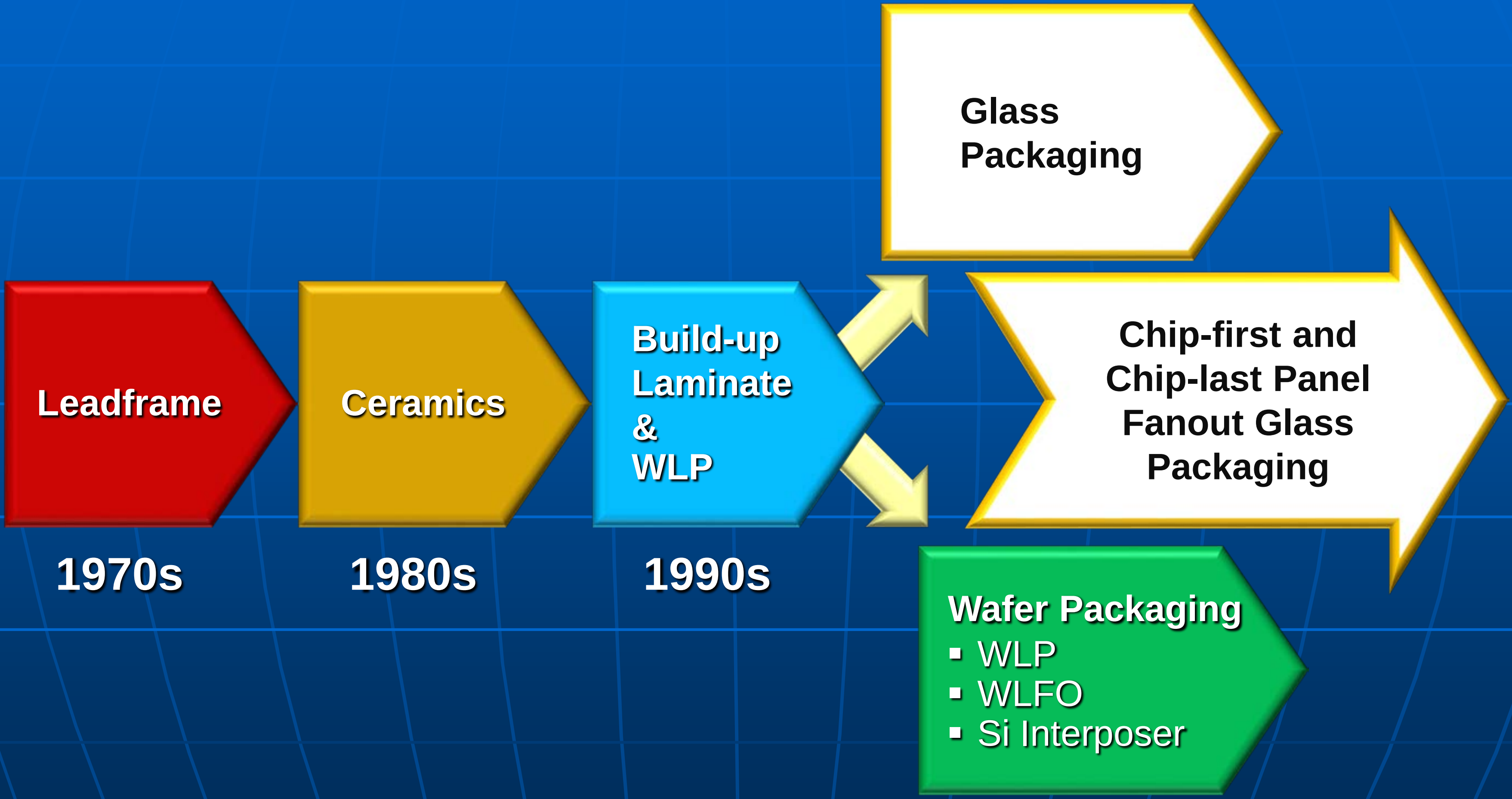
- SIP
- MCM
- 2.5D Interposers with 3D ICs

***Trend*:**

System on Board

- 3D System Architecture (GT)

Packaging Evolution to Glass Pkg, & Wafer Fanout



Glass Packaging

Leadframe

Ceramics

Build-up Laminate & WLP

Chip-first and Chip-last Panel Fanout Glass Packaging

1970s

1980s

1990s

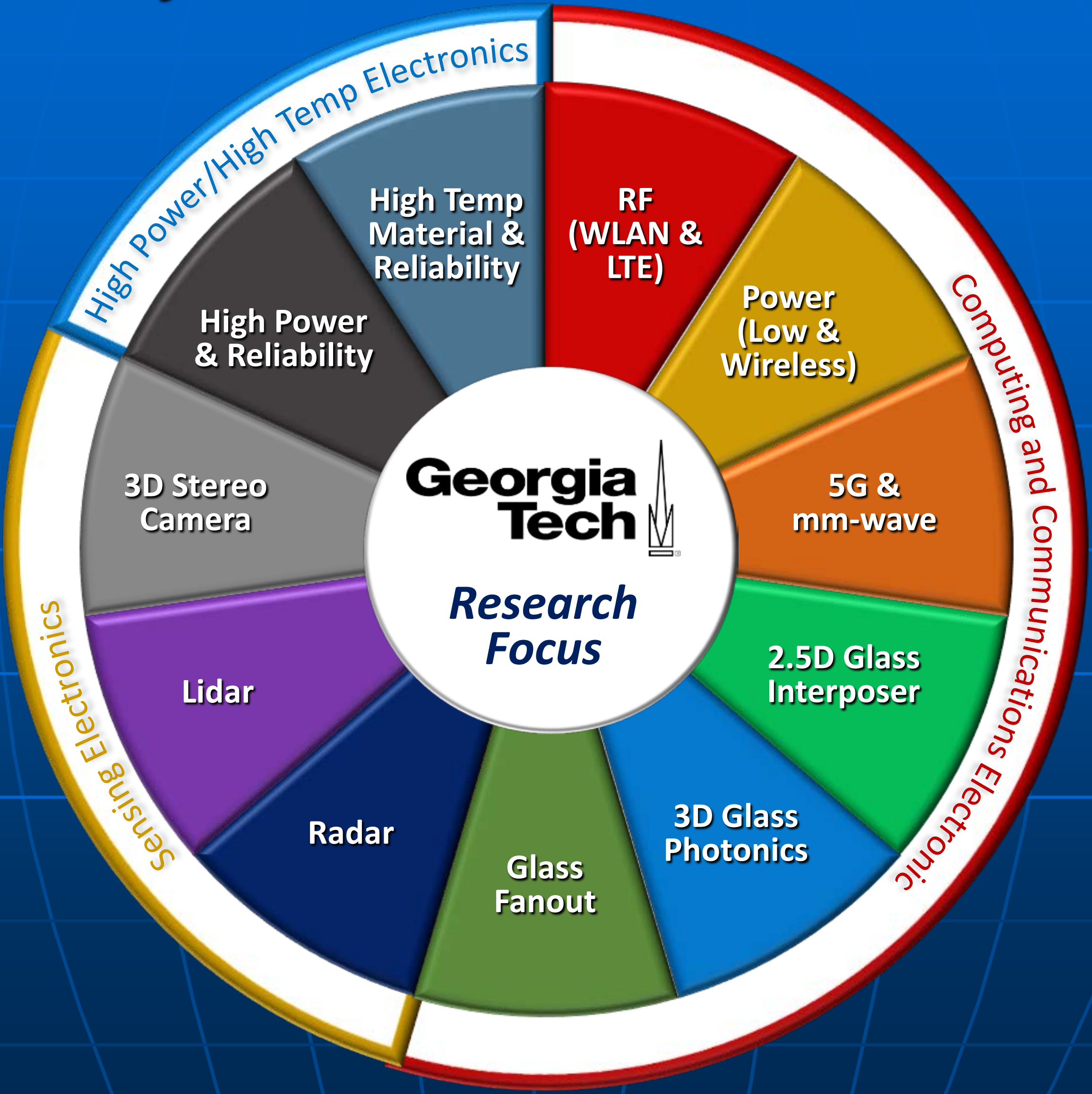
Wafer Packaging
- WLP
- WLFO
- Si Interposer

Wafer vs. Panel Fanout

- Wafer FO: Promise of Ultimate I/O Density
  - Reality: Limited by materials and processes
  - Limited to 300 mm so limited to small size packages
  - High cost for large multi-chip or SIP
  - Reliability and lithography limited by molding materials
  - One-stop shop for IC and package
- Panel FO: Promise of Ultimate Low Cost
  - Reality: Low cost
  - Limited in I/O density
  - Limited by polymer materials
  - Limited by large area sub-micron tools
  - Limited by large panel foundry investments

Future: Ultimate I/O Density and Ultimate Low Cost!

GT Industry Consortium Technical Strategy



Basic & Design & Demonstration Research (2016-'18)

D&D Test Vehicles

1. Computing & Communications Electronics
    - A. RF (WLAN & LTE)
    - B. Power (Low & Wireless
    - C. 5G and mm-wave
    - D. 2.5D Glass Interposer
    - E. 3D Glass Photonics
    - F. Glass Fanout
2. Sensing Electronics
    - A. Radar
    - B. Lidar
    - C. Camera
3. High-power & High-temp Electronics
    - A. High-power
    - B. High-temperature

1. Design

- Electrical: signal & power integrity
- Mechanical: warpage & reliability
- Thermal: Cu TPVs, evaporation and condensation

2. Electronic Substrates

- High-temp TPVs
- 1µm RDLs
- TPV & RDL reliability

3. Photonic Substrates

- Single and multi-mode
- Optical vias
- WG and turning structures
- Fiber coupling

4. Components

- Capacitors
- Inductors
- EMI shields
- PA thermal
- Diplexers
- Antennas
- Wireless power

5. Interconnects & Assembly

- SLID bonding
- Low-temp Cu-Cu interconnects
- High-throughput TCB
- Direct-SMT of Glass BGA
- Pre-applied underfill

6. Devices

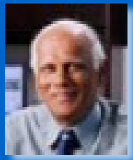
- GaN,SiC, SiGe, MEMS and Sensors
- OEIC, RF ICs, and Digital ICs

7. High-power/High-speed

- Switch and Gate Driver
- Metal Insulator substrates
- Embedded power chips & passives
- Sintered-Cu interconnection

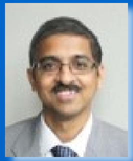
8. High-temp Electronic Materials

- High-temp polymers
- High-temp passives
- High-temp interconnections
- High-temp encapsulants



Prof. Tummala

Si-like I/Os with Glass Packaging



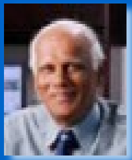
Dr. Sundaram

Parameter	Prior to 2014	2014-2016	2016-2018
TPV			
• Glass Thickness	180 µm	100µm	30-50µm
• TPV Pitch	150-200µm	100-120µm	50µm
RDL			
• Line- Space- Via	5-5-15µm	3-3-8µm	1.5-1.5-2µm
• Layer Count	2 + 2	3 + 3	4 + 4

What is a System Scaling Platform?
Ultra-thin Panel Glass with Ultra-fine Pitch TPV & RDL

Characteristic	**Materials**						
	Ideal Properties	**Glass**	**SC Si**	**Poly Si**	**Organic**	**Metal**	**Ceramic**
Electrical	▪ High resistivity ▪ Low loss and low k	🟩	🟥	🟨	🟩	🟥	🟩
Physical	▪ Smooth surface finish ▪ Large area availability ▪ Ultra thin	🟩	🟨	🟩	🟨	🟨	🟨
Thermal	▪ High Conductivity	🟨	🟩	🟩	🟥	🟩	🟨
Mechanical	▪ High strength & modulus ▪ Low warpage	🟨	🟨	🟨	🟥	🟩	🟨
Chemical	▪ Resistance to process chemicals	🟩	🟨	🟨	🟨	🟥	🟨
TPV and RDL Cost	▪ Low cost Via formation and metallization	🟨	🟥	🟨	🟨	🟥	🟥
Reliability	▪ CTE matched to Si and PWB	🟩	🟩	🟩	🟨	🟥	🟨
Cost/mm^2	▪ At 25µm I/O pitch	🟩	🟥	🟨	🟥	🟥	🟥

🟩 Good 🟨 Fair 🟥 Poor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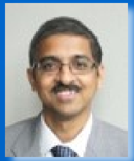
Leading Advances in Glass Packaging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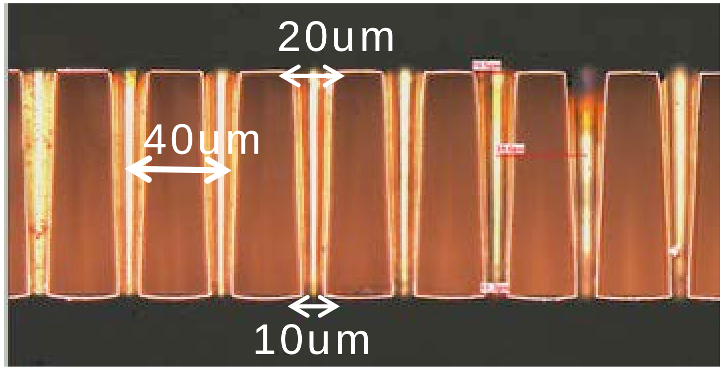
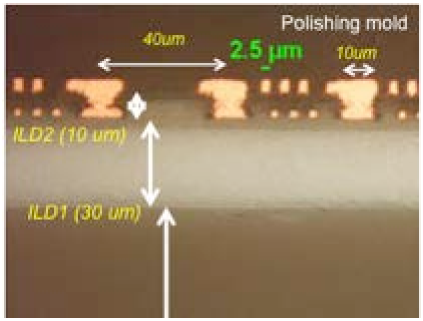
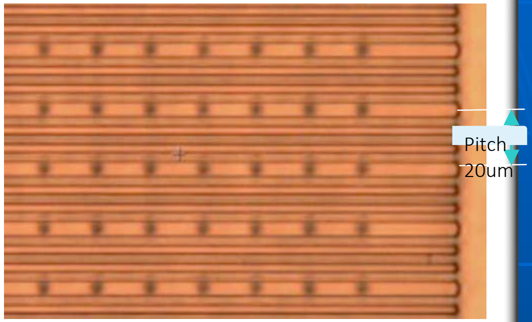
TPVs in Glass @ TSV Pitch



2um RDL @ 20-40um Pitch

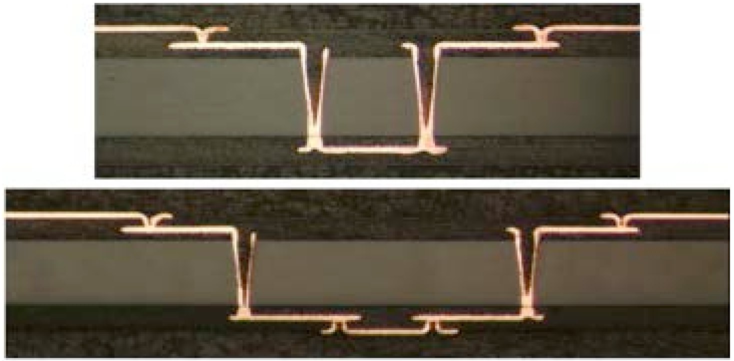


2.5D with 40um Pitch

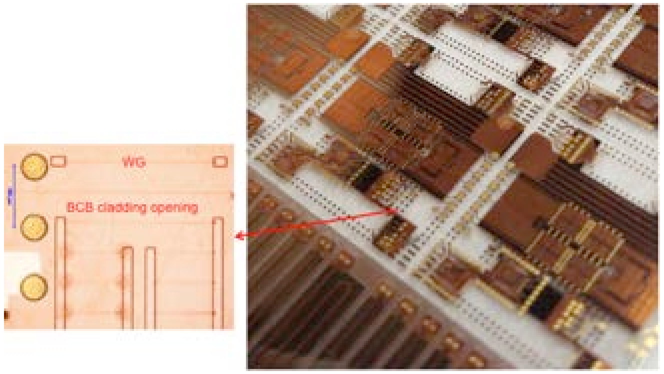


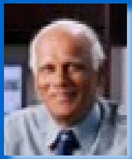
1st Demo at 20um Pitch

Multilayer Glass Substrate POR



Single Mode Photonics Integration





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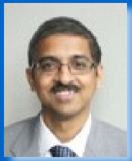
Si-like RDL on Glass Panels for Low Cost



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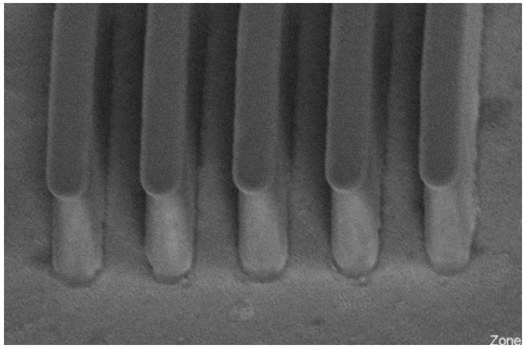
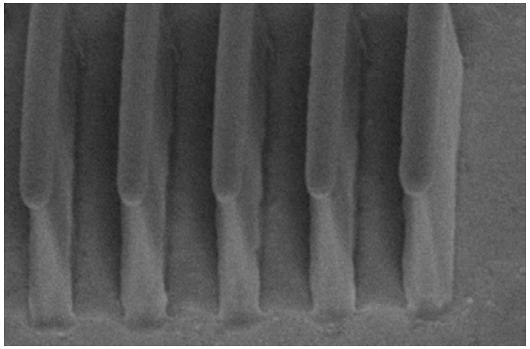
Dry film resist
wet processing

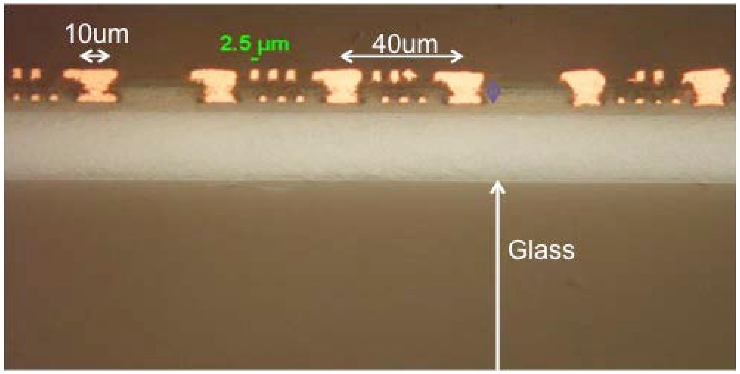
2.0 µm L/S



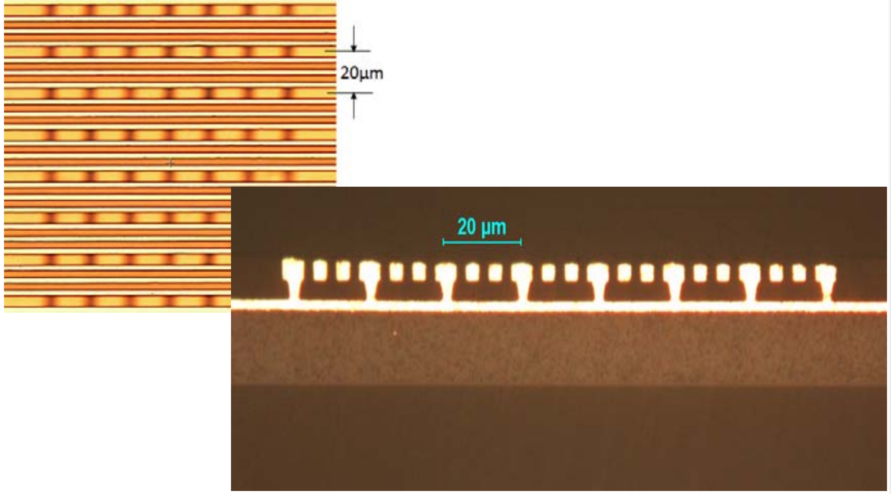
1.5 µm L/S



Extending SAP to 40 µm Pitch & Beyond Enabled by Glass

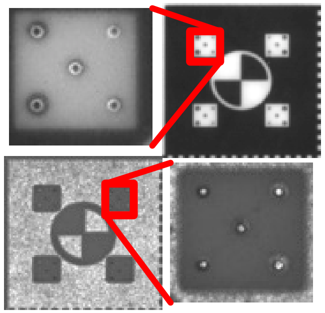


Via in Line at 20 µm Pitch Multilayer RDL - 1st time on Panel



Georgia Tech Glass Embedded Fanout
Si-like I/Os, Laminate-like Cost

Reduced Die Shift

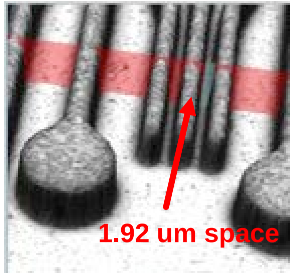


+/-1um Registration

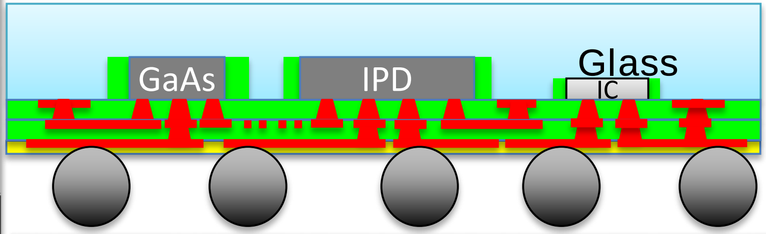
Ultra-fine Pitch I/Os

Same Cost as Laminate Panel

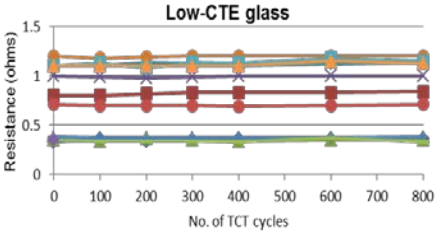
Silicon-like RDL



2µm lines and vias



Direct Attach to Board with Reliability

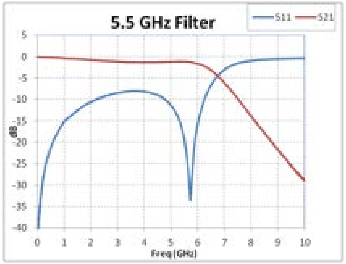


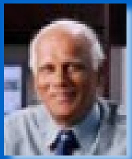
Hermetics

Ultra-thin

No Molding Compound

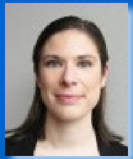
Ultra-low Loss up to mm-wave



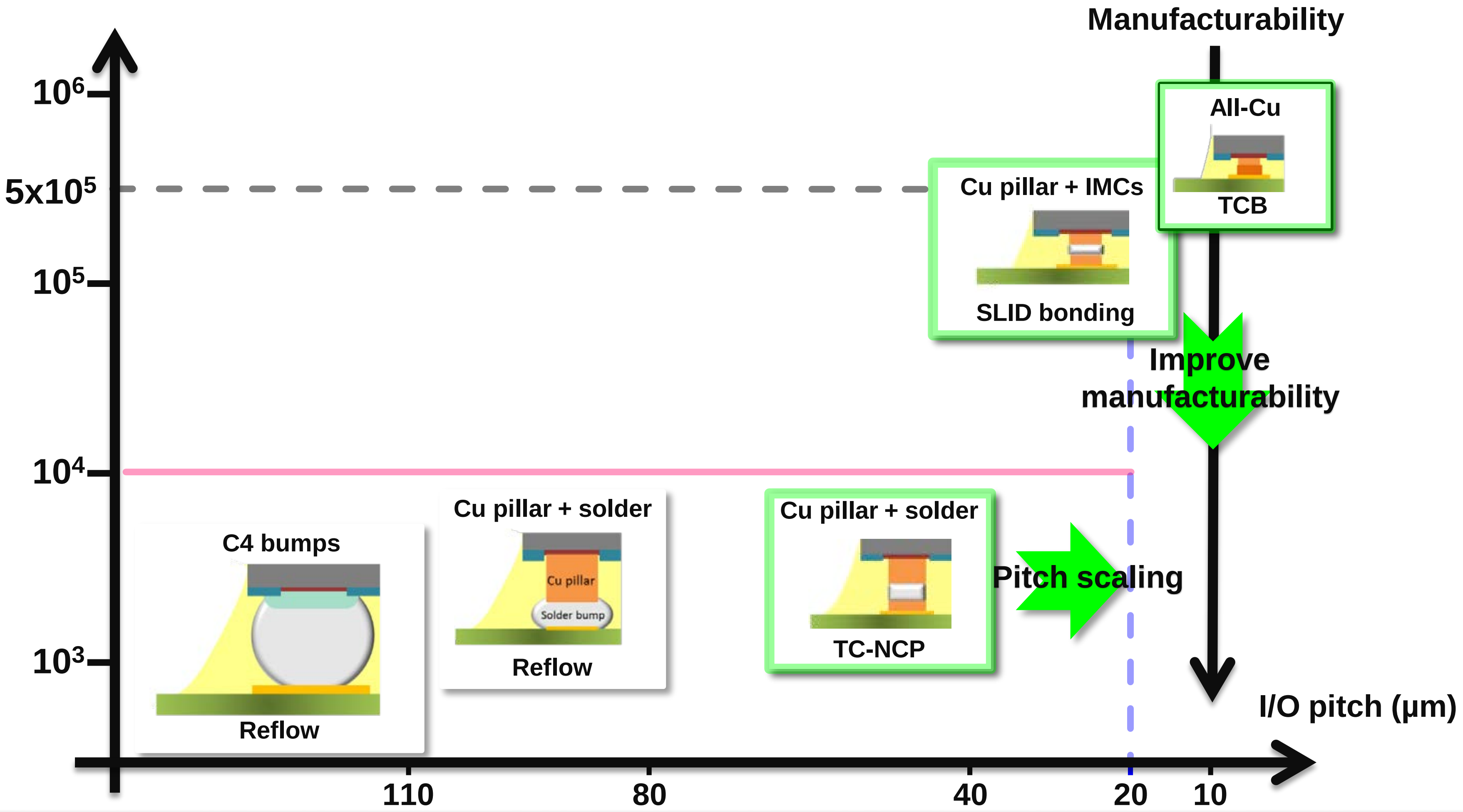


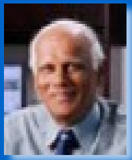
Prof. Tummala

Interconnections & Assembly Research



Dr. Smet



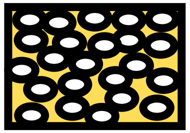


Prof. Tummala

RF Components & Modules Research

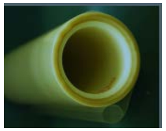
Dr. Raj

Materials design and synthesis for better properties



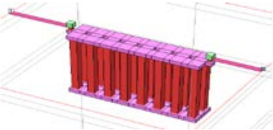
Nanoparticles

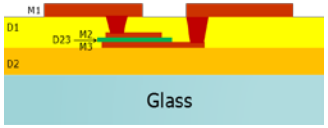
Nanofilms



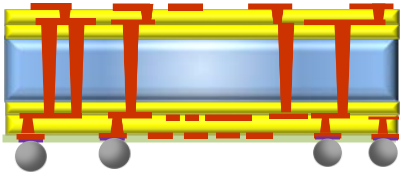
Polymer films

Thinfilm components with better performance & precision

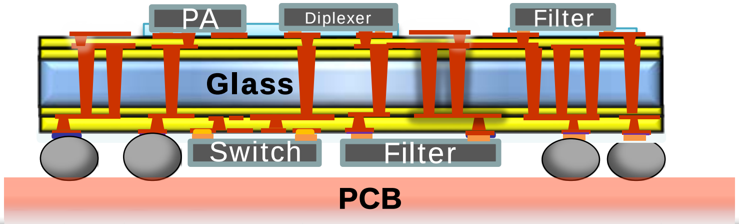


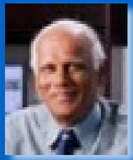


Passive integration on substrates



Passive with Actives to form modules





Prof. Tummala

Power Module Research

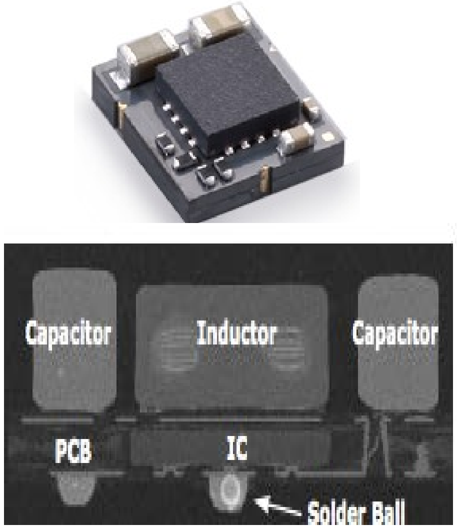
Dr. Sharma

Dr. Raj

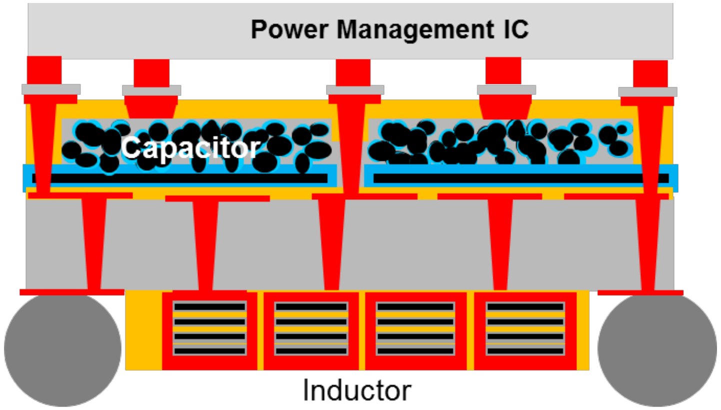
- Design and demonstrate low power module for consumer electronics with following attributes

Miniaturized → **High Power Handling** → **Low Cost**

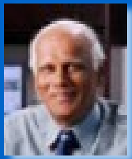
State-of-the-art power module



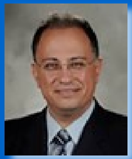
PRC's proposed power module



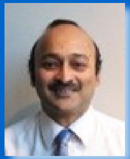
5G Research



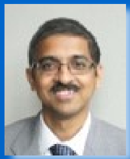
Prof. Tummala



Prof. Tentzeris

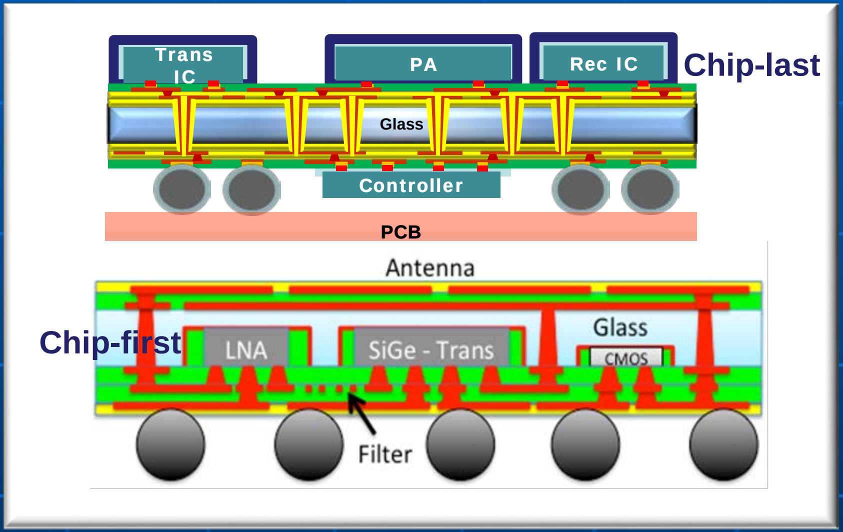


Dr. Raj



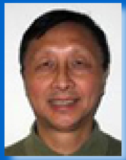
Dr. Sundaram

- Explore novel designs, materials, processes and 3D packaging structures and RF components to build 5G-enabled modules that accommodate V2X applications with superiority over LTCC and organic packages in terms of:
  1. Performance
  2. Miniaturization
  3. Reliability
  4. Cost
  5. Integrability (e.g.transparent)
  6. IoT compatibility
  7. Broadband/multiband (e.g. 5.9GHz/mmW) operability

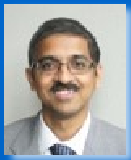


Prof. Chang

3D Glass
Photonics Research

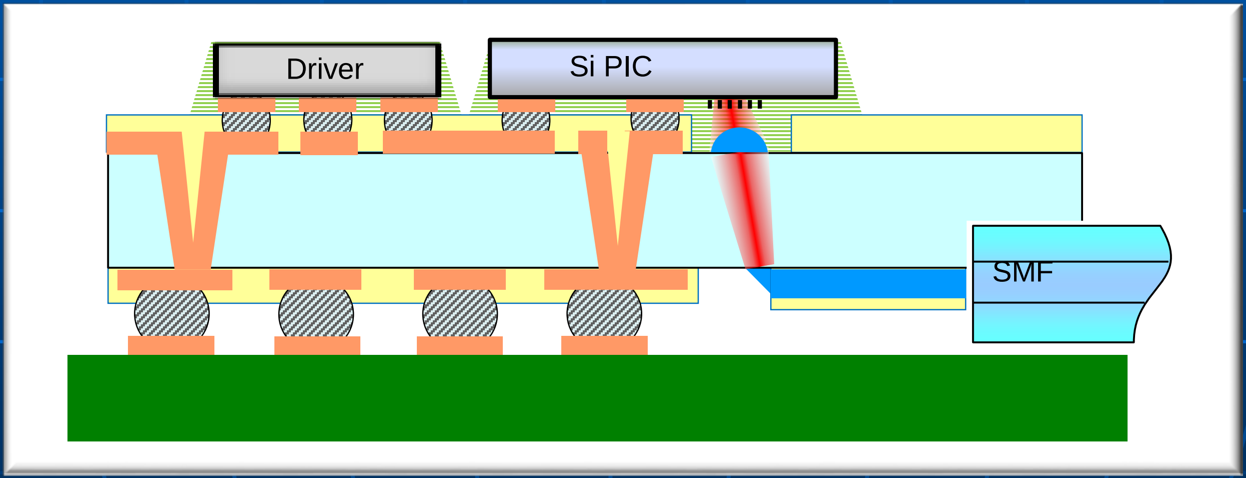


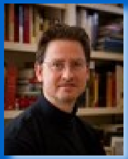
Dr. Liu

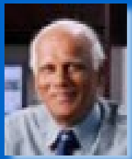


Dr. Sundaram

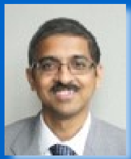
- Demonstration of low loss optical interconnects integrated with high speed electronics in 3D Glass Photonics (3DGP) interposer for optimum Energy Efficiency, Density, and Cost



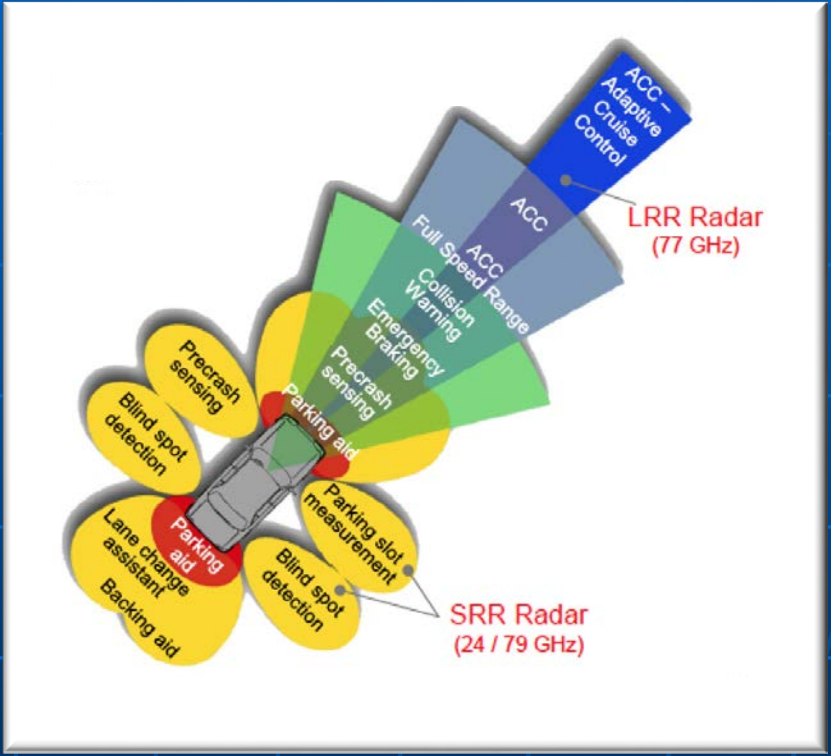

Prof. Cressler


Prof. Tummala

mm-Wave Automotive Radar Research


Dr. Sundaram

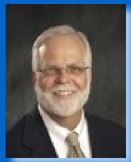
- Objectives:
  - Extended Range (Low SNR) by LNA
  - chip-package Synergy
  - SiGe for high speed and Si Mfg.
  - Board-Level Reliability
  - Low-cost
- Three Focus Areas
  - Device Innovation
  - Package Innovation
  - Chip-Package Co-Development



Short, Medium and Long Range RADAR Modules Critical to Fully Autonomous Driving

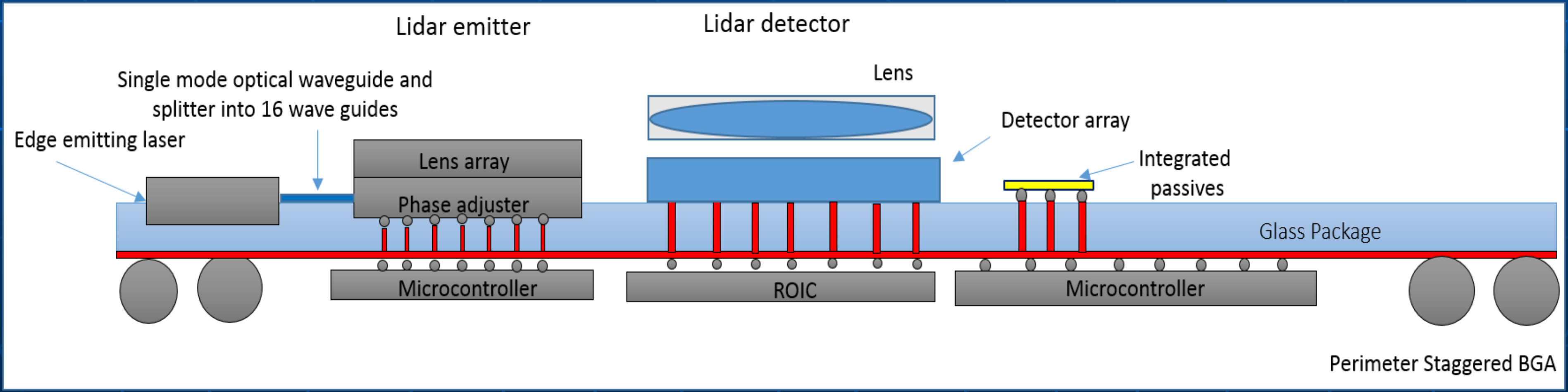
Prof. Wolter

Lidar Research



Dr. Tuell

- Design and demonstrate a 3D Glass Packaging platform for waveform-resolved Lidar module to support integrated collision avoidance
- Ability to see through fog/dust/rain/snow.
- Electrically steerable optical transmitter & receiver array enables high spatial and temporal resolution
- Smaller form factor for flexible integration (50x50x20) mm3
- Reaction time: ~1 msec
- High reliability due to solid-state Lidar system

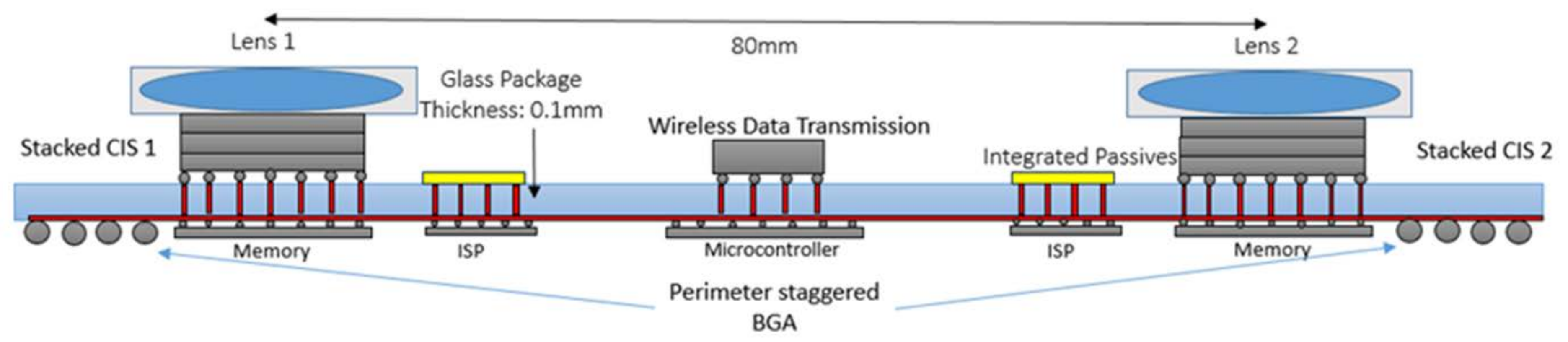


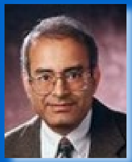
Prof. Wolter

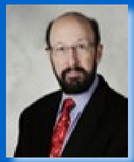
Camera Research

Prof. Hesketh

- Design and demonstrate most advanced and miniaturized mono and high speed stereo camera with integrated image processing.
- Reaction time: 1 msec
- High frame rate on demand: 1000 fps
- Optional wireless data transmission using Wi-Fi and Bluetooth
- Low cost and High Reliability for operation time up to 20,000 hours



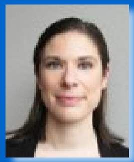

Prof. Joshi


Prof. Dupuis


Prof. Shen

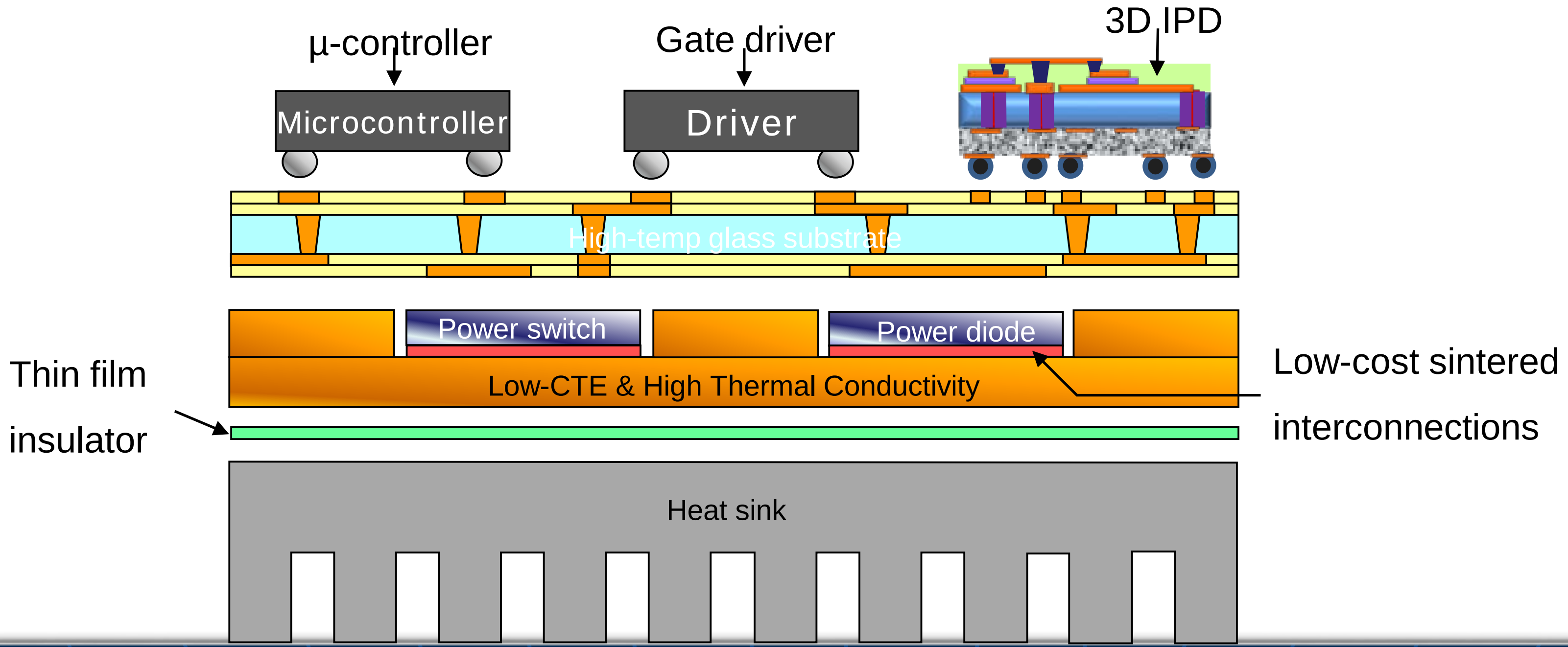
High Power & High-temp Electronics Research


Dr. Raj


Dr. Smet

- Integrated power, control and drive → ultra-thin
- CTE-matched “zero-stress” 3D integration
- Low thermal impedance, no liquid cooling
- Low cost

Design for high-temperature (<250°C), Hi-Rel.: Glass Power Embedding



Summary

- NAE is the Most Complex Electronics System, Requiring:
  - Technologies and Educated Workforce
  - Partnership with
    - Manufacturing Supply-chain and OEMs
- Georgia Tech Large-scale Global Industry Consortium Involves about 100:
  - Researchers
  - Developers
  - Manufacturers, and
  - OEMs

Georgia Tech Packaging Research Center
College of Engineering

Thank you

rao.tummala@ece.gatech.edu