Validation and Testing of Analog Machine Learning Systems

Yiorgos Makris
University of Texas/Dallas

Over the last decade, machine learning systems have become particularly popular and their widespread deployment has generated renewed interest and novel capabilities in a multitude of contemporary applications. However, as such systems transition from software to hardware implementations, several new challenges arise. More specifically, typical tasks such as validation and testing take on a different meaning, as the underlying hardware (i.e., machine learning system) has innately a rather fluid specification. Indeed, the malleability of the machine learning structure implemented by the hardware (i.e., machine learning system topology) along with the trainability which essentially customizes the hardware based on a given data set, either once or continuously, imply that the capabilities that need to be validated and tested in order to ascertain the hardware implementation of a machine learning system are far broader than those of a typical integrated circuit. This issue is exacerbated in analog implementations of machine learning systems, which are particularly popular in power-constrained environments, such as edge devices of the Internet of Things and industrial sensors/actuators. In this presentation, we will first elucidate the similarities of the problem at hand with that of validation and testing of analog integrated circuits. Then, we will discuss potential avenues for addressing the problem by extending previously developed self-test and self-calibration methods to ensure not only that a fabricated analog machine learning system complies with its specifications but also that it possesses the desired learning capacity both before and after its deployment, even in the face of adversarial training sets and potential silicon aging effects.