2021 Packaging Review
August 17-19 – Virtual Event
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Student Poster Information

(Abstracts)

Featuring:
Diego Vaca
Allison Osmanson
Yi Ram Kim
Jacob Dawes

Poster 1	Display Room: Gather Town
Poster Title:	**Bonding of Highly Oriented Pyrolytic Graphite as Heat Spreader for Portable Devices**
Task Number	Task 2947.001
Abstract:	Highly oriented pyrolytic graphite (HOPG) is considered to be used as heat spreaders for the thermal management of hot-spots on chips in mobile devices. However, their superior thermal properties are not fully exploited because the material and processes used to bond the HOPG to the chip can obstruct the heat flow. In this work, we compared the mechanical strength of three bonding solutions: gold-to-gold and copper-to-copper metallurgical bonding, CYTOP®, which is a polymer with good flowability and capable of producing thin bond lines (BL), and nanoporous copper. After bonding, shear tests were performed on the samples. The results indicate that the maximum shear force measured on 5 x 5 mm2 samples was in the range of 1.0 to 1.5 kgf, irrespective of the bonding technique. Further analysis revealed that the joint fractures in the HOPG itself by delamination, and not in the BL. This means that the selection of the bonding process must consider important factors such as the thermal behavior of the bond, the cost, the adaptation of the process to usual industrial practices, provided that the HOPG will comply with the mechanical demands of the system.
Student Presenter / University:	Diego Vaca/ Georgia Tech
	Dept: Mechanical Engineering Faculty Advisor: Dr Satish Kumar Graduation Date: July 2022 Email: dvaca3@gatech.edu Other Authors on the Poster: Dr. Vanessa Smet, Dr. Yogendra Joshi, Dr. Satish Kumar

Poster 2	Display Room: Gather Town
Poster Title:	**Mechanical Effects of Pulsed-DC Conditions on Electromigration Failure Kinetics in Wafer-Level Chip Scale Packages**
Task Number	2949.001
Abstract:	Accelerated electromigration (EM) studies on Wafer-Level Chip Scale Packages (WCSPs) suggest that the solder joint failure in pulsed direct current (pulsed-DC) conditions can be assisted by thermal fatigue mechanism. This phenomenon was especially distinctive in samples tested under higher duty factors (DF) of low-frequency pulsed-DC. These samples showed a drastic reduction in mean-time-to-failure compared to samples subjected to lower DF pulsed-DC or DC conditions, suggesting the existence of a mechanism accelerating the failure. The cross-sectional failure analysis of failed samples revealed a crack along the solder bump and under-bump metallization (UBM) interface, evidence of the involvement of mechanical failure. Subsequent analysis of the failure indicates that the cracking is rooted to the thermal fatigue by pulsation in temperature (and stress) with the pulse. Cyclic stress generation and plastic deformation by pulsating joule heat/temperature is believed to be responsible for the involvement of the fatigue in the failure mechanism. The finite element method (FEM) of the thermal fatigue mechanism which occurs in pulsed-DC conditions is implemented to gain a theoretical understanding of the mechanical effects of pulsed-DC failure on EM reliability.
Student Presenter / University:	Allison T. Osmanson University of Texas at Arlington
	Dept: Materials Science and Engineering Faculty Advisor: Dr. Choong-Un Kim Graduation Date: 12/2021 Email: allison.osmanson@mavs.uta.edu Other Authors on the Poster: Yi Ram Kim, Mohsen Tajedini, Choong-Un Kim

Poster 3	Display Room: Gather Town
Poster Title:	**Microstructural Effects on Electromigration Failure Kinetics in Wafer-Level Chip Scale Packages**
Task Number	2949.001
Abstract:	Previous electromigration (EM) studies on Wafer-level Chip Scale Packages (WCSPs) have indicated that the EM failure rate may be impacted by the grain orientation of Sn in the solder joint. The effect may exist because the body-centered tetragonal crystal structure of Sn may provide an easy EM path along c-axis, which can accelerate the EM failure kinetics in a significant degree. We have investigated this possibility by conducting microscopic investigation of the Sn grain orientation in early and late failures. Our investigation involves the use of scanning electron microscopy (SEM) and electron backscatter diffraction (EBSD), and inspection of degree of alignment between [001] grain orientation and EM direction. Our study confirms the so-called the alignment effect because the early failed joints are found to contains grains with c-axis alignment. The results suggest that the alignment effect needs to be addressed in order to improve EM reliability of solder joint. Control of grain orientation in solder joint may be the simplest way of achieving such goal, motivating ongoing studies of ours.
Student Presenter / University:	Yi Ram Kim University of Texas at Arlington
	Dept: Materials Science and Engineering Faculty Advisor: Dr. Choong-Un Kim Graduation Date: 12/2021 Email: yiram.kim@mavs.uta.edu Other Authors on the Poster: Allison T. Osmanson, Mohsen Tajedini

Poster 4	Display Room: Gather Town
Poster Title:	Heterogeneous Sensor System in Package (SSiP) Integration using Wafer-Level Molding
Task Number	2950.001
Abstract:	High-end electronic systems increasingly demand advanced packaging solutions such as fan-out wafer level packaging (FOWLP) to enable a broad array of system-in-package (SiP) devices at a competitive price point. In addition to design re-use, multi-chip integration at the package level allows each block to be implemented in an optimal CMOS process node for that block. This approach may combine circuits and devices from multiple process technologies, including MEMS transducers, optical components, magnetic materials, biosensor substrates, or low-loss RF materials. Leveraging FOWLP alongside high-end 3D printing provides a framework for highly reconfigurable redistribution layers and rapid prototyping of Sensor System in Package devices using a library of ICs, sensors, actives, passives, and other materials for electrical and optical functionality. This modular, on-demand manufacturability of multi-material and multicomponent electronic systems within a shared substrate, compared to PCBs, fixed-tooling, and Si-only SiP approaches, enables rapid functional diversification and co-location of heterogeneous components.
Student Presenter / University:	Jacob Dawes Oregon State University
	Dept: Electrical and Computer Engineering Faculty Advisor: Matthew Johnston Graduation Date: 12/23 Email: dawesj@oregonstate.edu