2021 Packaging CHIRP Center Review
August 24-26 – Virtual Event
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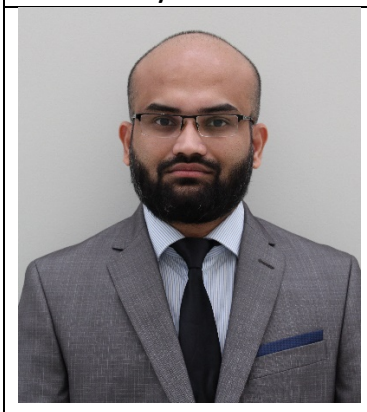
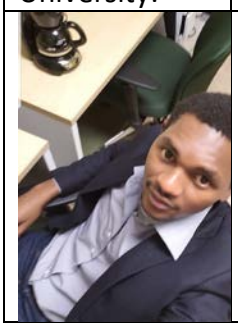
Student Poster Information

(Abstracts)

Featuring:
Sanoop Thekkut
Ronit Das
Michael Njuki
Gaurav Kothari
Zechen Zhang
Piyush Kulkarni
Diana Fallahtafti
Md Asaduz Zaman Mamum
Ezer Castillo
Andrew Pham
Soumya Bandyopadhyay

Poster 1	Display Room: Gather Town
Poster Title:	**Effects of Oxidation on The Inelastic Deformation of Nano-Copper Based Joints and Bonds**
Task Number	2878.005
Abstract:	The inelastic deformation properties of nanocopper joints with nanoporous structures vary under mild cycling conditions and depends on the specific microstructure obtained right after sintering. Additionally copper is prone to oxidation in air even at room temperature. This work shows the effect of oxidation on the creep properties of nanocopper based joints. It is found that joints sintered in forming gas are prone to rapid oxidation in air above 75°C and the calculated activation energy points towards the grain boundary diffusion mechanism. Joints sintered in H_2 ambient are more stable with less porous structures and shows more resistance towards oxidation.
Student Presenter / University:	Sanoop Thekkut/Binghamton University-SUNY
	Dept: Systems Science and Industrial Engineering (SSIE) Faculty Advisor: Dr. Peter Borgesen Graduation Date: May -2022 Email: sthekku1@binghamton.edu Other Authors on the Poster: Rajesh Sivasubramony, Yuki Kawana, Ninad Shahane, Patrick Thompson, Kabir Mirpuri, Christopher Greene and Peter Borgesen

Poster: 2	Display Room: Gather Town
Poster Title:	Reliable SnAgCuBi Micro-Joints Formed by Soldering at a Low Temperature
Task Number:	2878.012
Abstract:	Eutectic SnBi can be used for soldering at a lower peak temperature as it melts around 138-139˚C. However, the deformation and damage properties of the resulting joints as reported by many are somewhat inferior to those of SnAgCu. Generally, properties of these joints are enhanced by the addition of Sn but at a cost of increasing the reflow temperature. An approach to soldering SnAgCu bumps/pillars on a limited volume of eutectic SnBi and subsequent annealing may allow for the Bi to distribute throughout it and establish the concentration of interest. Results suggest this to be only practical for small joints, whereas larger ones would end up with a varying composition of Bi near the substrate and no Bi near the component, known as 'hybrid' joints. In many respects, SnAgCu with 2-6 weight-% of Bi is known to **improve** on the reliability of an alloy. The only counteracting effect is that annealing would also coarsen the Ag_3Sn precipitates, reducing the thermal fatigue resistance of SnAgCuBi joints. The thermal fatigue life of a SnAgCu solder joint occurs by the continuous coalescing of dislocations, during the high temperature dwell, leading to recrystallization, and eventually failure. However, to begin this evolution, Ag_3Sn precipitates need to coarsen enough, and it can be further delayed by the addition of Bi which also inhibits dislocation motion. A general comparison of annealed SnAgCuBi to that of unannealed SnAgCu in terms of the mobility of dislocations and the respective ductilities suggests that the thermal fatigue life of the former can be kept superior.
Student Presenter / University:	Ronit Das, SUNY Binghamton
	**Dept:** Systems Science & Industrial Engineering **Faculty Advisor:** Dr. Peter Borgesen (borgesen@binghamton.edu) **Graduation Date:** December 2022 (Expected) **Email:** rdas5@binghamton.edu **Other Authors on the Poster:** A. Mahmood, S. Thekkut, R. Sivasubramony, M. Njuki, C. Greene, N.G. Dimitrov and P. Borgesen

Poster 3	Display Room: Gather Town
Poster Title:	**Sporadic Voiding Effects in Micro Joints: Understanding and Control**
Task Number	2878.005
Abstract:	Electrodeposited Cu UBM or surface finish has been widely used for decades in electronic industry because Cu provides excellent electrical connection between the substrate and the flip chip, which gives a shorter path and reduces latency issues as compared to wire bonding. The interfacial reaction between Cu surface finish and solder under increasingly confined space is becoming a reliability risk due to such large miniaturization of the solder volume, and this has necessitated the need to study other systems where soldering is done on other substrates instead of traditional Cu substrate. These reliability issues include (i) faster Cu-Sn intermetallic compounds (IMCs) growth under such space confinement, (ii) more pronounced sporadic void formation in the Cu3Sn IMC layer, and (iii) a high rate of substrate degradation due corrosion. Nickel UBM having been successfully used as a diffusion barrier to prevent interdiffusion of Cu and Au in jewelry industry, has attracted attention in flip chip interconnections and 3D ICs in recent years as a diffusion barrier between Cu and Sn because of its slower reaction rate than traditional Cu-solder interfacial reaction at the same time preventing Cu from oxidation. In the reaction between conventional Ni and Sn interconnections such as BGA and flip-chip joints, Ni3Sn4 is the only compound formed between 75°C and 300°C and Ni_3Sn_4 growth is dominated by the diffusion of Sn in through it to the Ni surface, whereas the Ni out-diffusion is negligible. When Sn reacts with Ni to form a joint, it is estimated from the molar volumes of Sn, Ni, and Ni3Sn4 that volume shrinkage of 11.3% occurs. Although this amount of shrinkage is quite high, it does not cause any problem when the solder joints are large, as in the case of typical flip-chip (~100µm) and larger solder joints since intermetallic compounds (IMCs) occupy only a small part of the whole joint volume. Two different types of voiding issues related with Ni_3Sn_4 have been reported in literature. First, the entrapment of voids between the colliding IMC layers from opposing Ni surfaces when reacting to completion in Ni/Sn/Ni sandwich samples and secondly, voids formed at the interface between the solder and Ni_3Sn_4 layers, when the thicknesses of the Ni_3Sn_4 exceeded 5µm. Our work focuses on the later where voids have been observed for different types of Ni (electrolytic, electroless, Ni/Pd/Au) and for different solder systems as well. Previous research has suggested the reason for this voiding when the thicknesses of the Ni_3Sn_4 exceeded 5µm is due to volume expansion of Ni layer which may led to shear stress at the interface between IMC and solder. This shear stress induces the formation of voids. This would mean that the defect formation on Ni finishes is not preventable, except slowing the IMC growth enough to limit the stresses causing defects. Our results do however show that the defects formation does not always occur and when it occurs it can be controlled with proper process parameters.
Student Presenter / University:	Michael Njuki Binghamton University
	Dept: Chemistry Faculty Advisor: Dr. Dimitrov Graduation Date: 12/12/2024 Email: mnjuki1@binghamton.edu Other Authors on the Poster: S. Thekkut, R. Das, N. Shahane, K. Mirpuri, P. Borgesen and N. Dimitrov

Poster 4	Display Room: Gather Town
Poster Title:	**Thermally-Aware Die-Stacking Schemes for Processing Cores and Caches**
Task Number	2878.007
Abstract:	We present two minimally invasive thermally-aware microarchitectural techniques for exploiting the advantages of chiplet stacking for processing cores and the last level caches (LLCs). Both techniques mitigate hot spot formation compared to naive chiplet stacking solutions and do not need a significant redesign of the chiplets, other than the layout changes needed to accommodate the vertical interconnections. For stacking the processing cores, we rely on the knowledge of the hot spot locations to flip the layout of the cores along one or more geometric dimensions to avoid hot spots in vertically adjacent chiplet regions while preserving the adjacency to the LLCs in each chiplet. For the LLCs, the technique relies on remapping the physical locations of the rows to distribute the hot spots created by the typical access patterns. These two techniques are evaluated using a toolchain that comprises a cycle-accurate microarchitectural simulator that simulates the execution of typical benchmark applications, power and thermal models for the primary building blocks in each chiplet, and analysis tools that demonstrate the benefits of the proposed stacking techniques. Performance, complexity, and area tradeoffs are also discussed to demonstrate how the proposed chiplet stacking techniques fare against naive solutions for stacking processors and caches.
Student Presenter / University:	Gaurav N Kothari (State University of New York at Binghamton)
	**Dept:** Computer Science **Faculty Advisor:** Dr. Kanad Ghose **Graduation Date:** December 2022 **Email:** gkothar1@binghamton.edu **Other Authors on the Poster:** Anuroop Desu, Kanad Ghose, Bahgat Sammakia

Poster 5	Display Room: Gather Town
Poster Title:	**Minimizing Thermal Interfacial Resistance in Heterogeneous Integration**
Task Number	2878.003
Abstract:	Thermal interface materials (TIMs) are widely used in electronic devices owing to their ability to thermally bridge gaps and voids at the interface between heat producing chips and heat removal device. The design goal of TIMs is to minimize the thermal interface resistance during the device's service lifetime. Previous reports from industry focus on the average thermal properties of TIMs. We explored how thermal properties of different polymeric TIMs vary spatially, using a setup with a spatial resolution as low as 10µm. This resolution enables quantification of spatial variability, which is important to preventing hot spots. We developed an understanding of how polymeric TIM properties change due to bond line thickness, applied pressure, and thermal cycling conditions. Complementary characterizations of thermal interface materials made via electron microscopy, electron dispersive x-ray spectroscopy, x-ray imaging, differential scanning calorimetry, and mechanical testing will be shared. TIMs thermal properties measured with frequency domain thermoreflectance, flash diffusivity, and steady-state techniques for different bond line thicknesses will be related to these non-thermal characterizations.
Student Presenter / University:	Zechen Zhang/ Binghamton University
	Dept: Mechanical Engineering Faculty Advisor: Scott N. Schiffres Graduation Date: 12/31/2023 Email: Zechen Zhang (zzhan195@binghamton.edu) Scott N. Schiffres (sschiffr@binghamton.edu) Other Authors on the Poster: Zechen Zhang, Piyush A Kulkarni, Morteza H. Bagheri, Fatemeh Hejripour Rafsanjani, Christine Jacobs, John A. Hart, Bahgat G. Sammakia and Scott N. Schiffres

Poster 6	Display Room: Gather Town
Poster Title:	**Non-Destructive Evaluation of Thermal Interface Materials using Modulated Heating of Selective Cores**
Task Number	2878.003
Abstract:	The presentation will discuss a new technique to identify local defects (eg voids, bond line thickness deviation, spatial microparticle concentration gradients) in Thermal Interface Material (TIM) layers in electronic packages. Application of a modulated computational loads to individual package elements (eg CPU cores, GPU) allows local the measurement of the TIM1 layer between a silicon die and the internal heat spreader (IHS). The temperature amplitude and angular phase is a function of the thermal conductivity and thickness of the TIM1, and is sensed at different locations by the temperature-dependent current supplied to the electronic components or built-in temperature sensors. The temperature response to a periodically modulated heating flux in the core is simulated with varying defect size, die thickness and heating frequency. Voids can be detected by comparing the periodic response to reference conditions. The optimal modulation frequency range is defined in terms of the Si-Die thickness and core size to obtain the appropriate thermal penetration depth for sensing TIM1 layer defects. The testing method can further be extended to the use of multiple neighboring cores modulated at the same time at different frequencies for high throughput testing. Experimental results will also be discussed.
Student Presenter / University:	Piyush Kulkarni/Binghamton University
	Dept: Mechanical Engineering Faculty Advisor: Dr. Scott Schiffres Graduation Date: Email: pkulka10@binghamton.edu Other Authors on the Poster: Fatemeh Rafsanjani Hejripour, Zechen Zhang, Bahgat Sammakia, Scott N. Schiffres

Poster 7	Display Room: Gather Town
Poster Title:	**Characterization and Parametric Optimization of Two-Phase Cooling of Commercial and 3D-printed Cold Plates**
Task Number	2878.006
Abstract:	The objective is to carry out experimental studies on single-phase and two-phase cold plates for high heat flux scenarios and develop an optimization methodology for families of cold plates designed for high heat flux applications.
Student Presenter / University:	Najmeh (Diana) Fallahtafti/ Binghamton university
	Dept: Mechanical Engineering Faculty Advisor: Bahgat Sammakia Graduation Date: Email: nfallah1@binghamton.edu Other Authors on the Poster: Srikanth Rangarajan, Yaser Hadad

Poster 8	Display Room: Gather Town
Poster Title:	**Design and Optimization of a Chip-Attached Micro-Pin Fin Cooling System for Heterogeneous Integration Applications**
Task Number	2878.006
Abstract:	The main objective of this project is to mitigate high heat fluxes of hotspots by the micro-pin fins directly printed on the chip surface. Opposed to the conventional cooling solutions, the proposed thermal management solution does not involve TIM and spreading thermal resistances which improves its thermal performance significantly.
Student Presenter / University:	Najmeh (Diana) Fallahtafti/ Binghamton university
	Dept: Mechanical Engineering Faculty Advisor: Bahgat Sammakia Graduation Date: Email: nfallah1@binghamton.edu Other Authors on the Poster: Srikanth Rangarajan, Yaser Hadad

Poster 9	Display Room: Gather Town
Poster Title:	**Correlated Moisture Diffusion, Ion-Transport, and Bond-wire Corrosion in Filled Polymers**
Task Number	2878.008
Abstract:	Over the last decade, Copper wire is rapidly replacing the traditional but expensive gold metal to serve as interconnects in modern microelectronic packaging. When operating in a high-humidity environment, however, the Cu-Al interface has a substantially higher tendency to produce less corrosion-resistant intermetallic compounds (IMCs) than the Au-Al counterpart. In our research, the physics of moisture diffusion and corrosion are combined with filler-tunable electrical and mechanical properties of EMCs, and the entire system is modeled using COMSOL Multiphysics, a commercially available FEM-based tool. In high voltage/temperature and humidity settings, we report on moisture-assisted Cu-Al bond-wire corrosion and Al bond pad deformation over time for various Molding Compounds. Furthermore, by incorporating the effect of IC self-heating in the moisture-assisted corrosion process, we present its relevance for the qualification and lifetime enhancement of Cu-Al interconnect technology in EMCs during burn-in testing.
Student Presenter / University:	Md Asaduz Zaman Mamun, Purdue University
	Dept: ECE Faculty Advisor: Muhammad A. Alam Graduation Date: 2024 Email: mmamun@purdue.edu

Poster 10	Display Room: Gather Town
Poster Title:	**Electrochemical Preparation of Nanoporous Cu Films as New Solder Materials for Interconnection**
Task Number	2878.011
Abstract:	Alternative materials for chip-to-substrate interconnection based on nanoporous Cu (np-Cu) films have been of interest in the last few years. np-Cu generally possesses a high surface-area-to-volume ratio, which lowers its melting temperature (compared to the bulk Cu counterpart). Further modification of np-Cu with a thin coating of Sn allows for the generation of a Cu-Sn joint that is anticipated to have a lower sintering temperature and improved resistance compared to that of pure Cu. In this work, we present an all-electrochemical preparation of np-Cu films. The electrosynthesis begins with the deposition of Cu-Zn precursor alloys (with Zn content of at least 60 atomic percent), which then undergoes selective de-alloying where the removal of Zn allows for the reorganization of the remaining Cu atoms to form the np structure. Our findings reveal highly porous Cu films with metal ligament sizes ranging from 20-30 nm and relatively high surface areas. The preparation, electrochemical, and morphological characterization of the Cu-Zn alloy films before and after de-alloying will be discussed.
Student Presenter / University:	Ezer Castillo / Binghamton University
	Dept: **Chemistry** Faculty Advisor: **Nikolay Dimitrov** Graduation Date: **2022** Email: **ecasti14@binghamton.edu** Other Authors on the Poster: **Nikolay Dimitrov**

Poster 11	Display Room: Gather Town
Poster Title:	**Mechanical Failure of Cu-Sn Solder Joints**
Task Number	2878.009
Abstract:	The effects of the microstructure on the fracture mechanisms of Cu-Sn intermetallic compounds (IMC) in solder joints under tensile load are studied with numerical simulations. When solder joints are exposed to elevated temperature environments Cu_6Sn_5 and Cu_3Sn nucleate and grow due to the reaction of Cu and Sn, and the fracture strength is degraded. During early stages of the thermal treatment, the Cu_3Sn layer of the IMC is thin and composed of a single stack of grains, and the simulations indicate that failure occurs at the Cu_6Sn_5 / Cu_3Sn interface. After hundreds of hours at temperatures over 150°C the Cu_3Sn layer thickness grows and is composed of a stack of several grains. Then, failure switches to intergranular fracture inside the Cu_3Sn layer. Therefore, the reduction of the fracture strength is a consequence of a transition in the Cu_3Sn layer from a single stack of grains to a multi-stacked structure. This structural transition occurs by the reduction of grain size and the growth of the Cu_3Sn layer thickness.
Student Presenter / University:	Andrew Pham / Purdue University
	Dept: Mechanical Engineering Faculty Advisor: Marisol Koslowski Graduation Date: May 2025 Email: pham89@purdue.edu Other Authors on the Poster: Xiaorong Cai

Poster 12	Display Room: Gather Town
Poster Title:	**Cascaded Vapor Chambers for Spreading of Non-Uniform Heat Loads**
Task Number	2878.002
Abstract:	Thermal management of heterogeneous electronic devices relies on spreading high local heat fluxes in the package lid. The use of intra-lid vapor chambers is an attractive approach if they can be designed for the thermal management of a large total heat load simultaneous with localized high-flux hotspots. Conventional vapor chambers, having a single vapor core, require thick evaporator wicks to avoid the capillary limit at high total power, but these thick evaporator wicks impose a large conduction resistance to hotspots. The recently proposed cascaded multi-core vapor chamber (CMVC) concept consists of a bottom-tier comprising multiple vapor cores that can each diffuse high heat flux hotspots before they reach the top tier, which acts as a conventional single-core vapor chamber. The current study experimentally investigates the use of cascaded vapor chambers for heat spreading of a non-uniform heat load to illustrate this design rationale. The thermal resistance of a solid copper benchmark, a conventional vapor chamber, and a cascade of two vapor chambers are compared for non-uniform heat input. Experiments are performed by interfacing the heat spreaders with a central heater generating the peak heat flux surrounded by a film heater that produces a lower heat flux background power; the other side of the spreaders is interfaced to a cold plate to provide a controlled boundary condition. The results demonstrate that the cascaded vapor chambers offer a notable reduction in thermal resistance relative to the conventional vapor chamber. The enhancement in performance is attributed to the local dampening of the peak heat fluxes at a low thermal resistance, thereby reducing the total thermal resistance of the cascaded vapor chambers relative to the standalone vapor chamber. This result reveals that cascades of vapor chambers have the potential to perform better than conventional vapor chambers through attenuation of hotspots at a low thermal resistance.
Student Presenter / University:	Soumya Bandyopadhyay/Purdue University
	School: Mechanical Engineering Faculty Advisor: Dr. Justin A. Weibel Graduation Date: Aug, 2023 Email: bandyop0@purdue.edu Other Authors on the Poster: Norawish Lohitnavy, Amy M. Marconnet, Justin A. Weibel