From Failure to Success:

High-risk Semiconductor Research – A Lesson in Serendipity

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Former and current students
Doyle, Kavalieros, Doczy, Metz, Dewey, Chau (Intel)
Engel-Herbert, Mayer, Narayanan (Penn State)
Salahuddin (Berkeley), Schlom (Cornell), Kummel (UCSD),
Raychowdhury, Khan, Naemi, Yu (GTech), Pop (Stanford),
Ye, Roy (Purdue), Cho (UTDallas), Fay, Niemier, Hu (Notre Dame)

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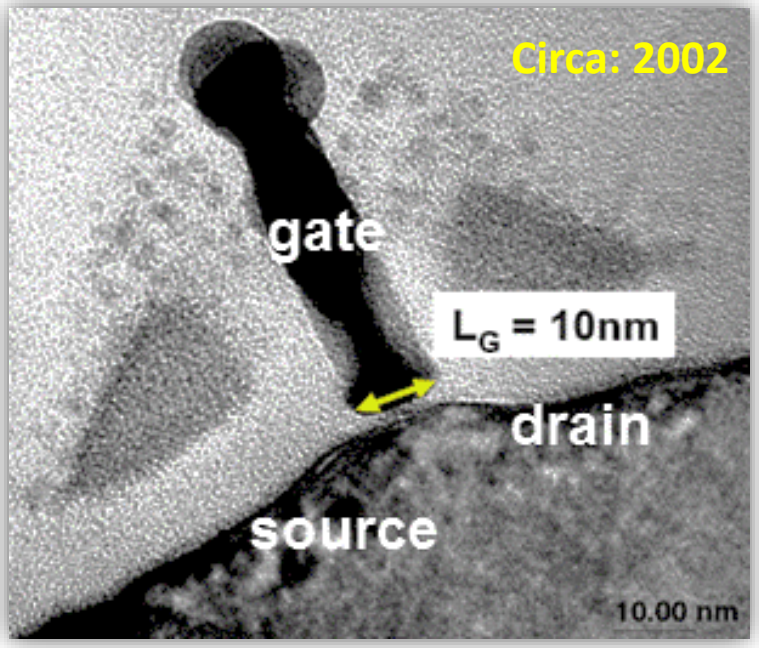
My journey

UNIVERSITY OF NOTRE DAME

- Learn from doing things (corporate research)
- Inspire the students (academic career)
- Lead a multi-university center (my current life)

10nm Transistor



B. Doyle, S. Datta, J. Kavalieros, R. Chau, "Transistor Elements for 30nm Physical Gate Lengths and Beyond" Intel Technology Journal, May 2002

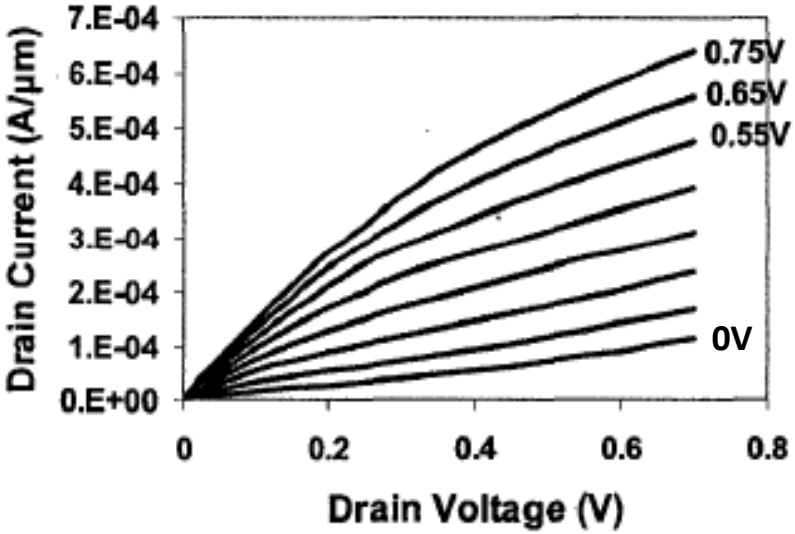


Figure 8: Family of Id-Vd curves for the 10nm research device.

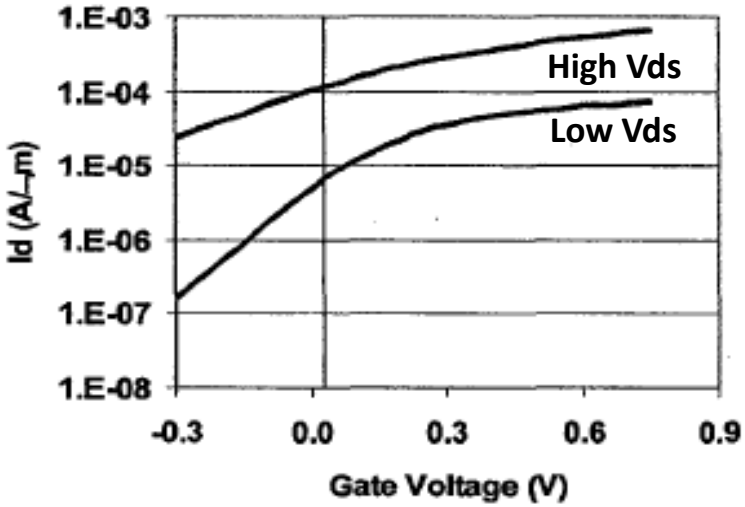
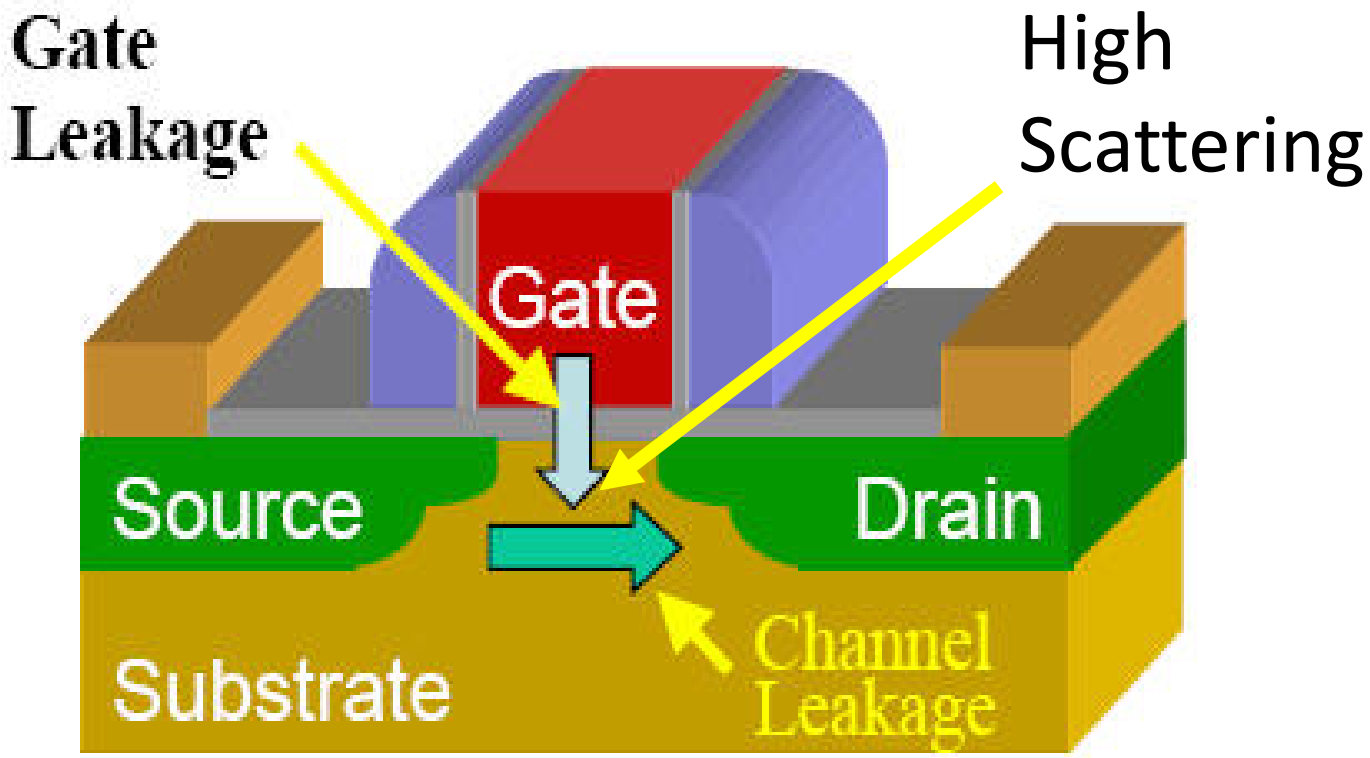


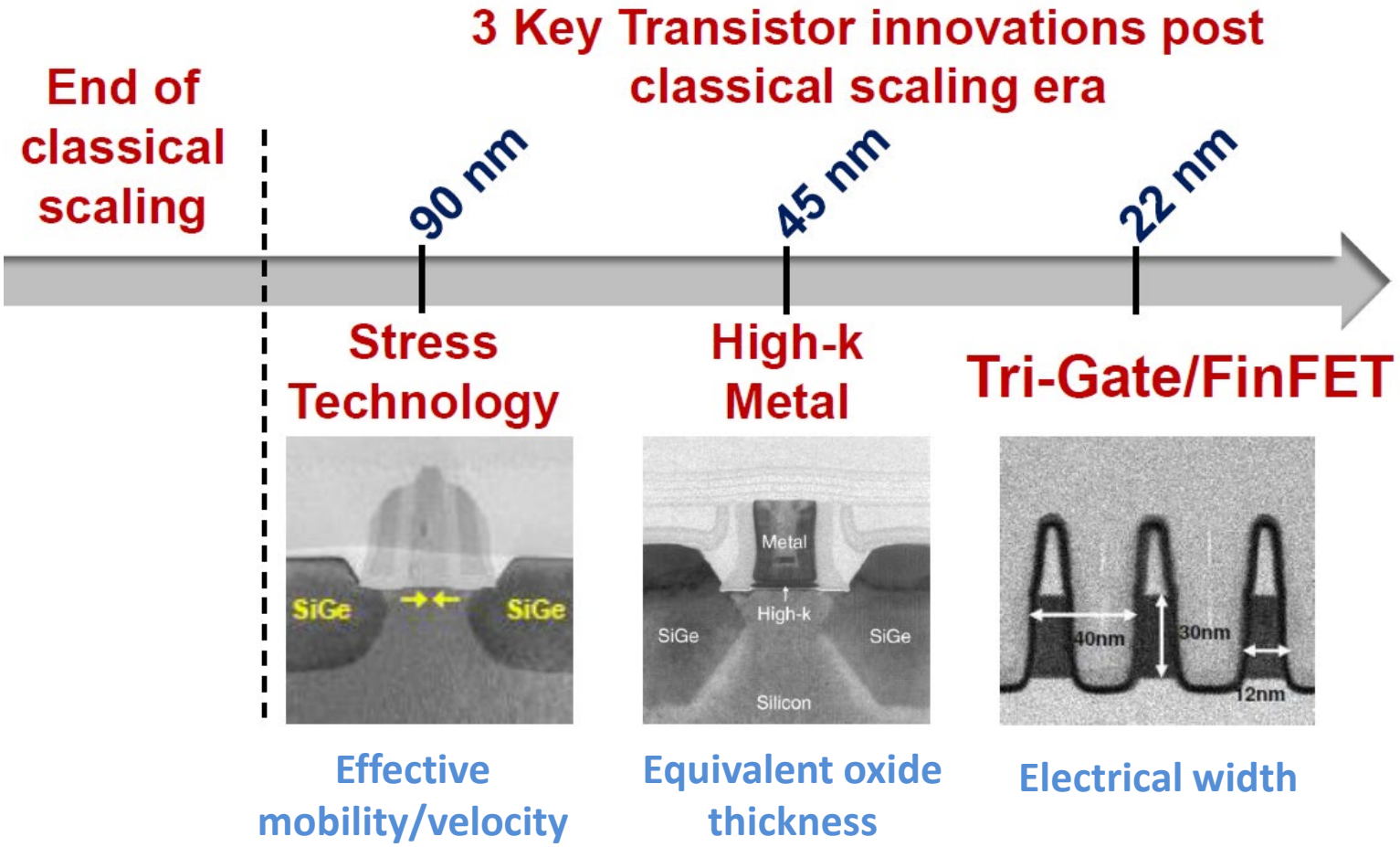
Figure 7: Id-Vg characteristics at Vd=50mV and 0.75V for the 10nm experimental device.

Classical Scaling Ends



Need fundamental innovations to a) improve channel transport, b) reduce gate leakage and c) improve electrostatics

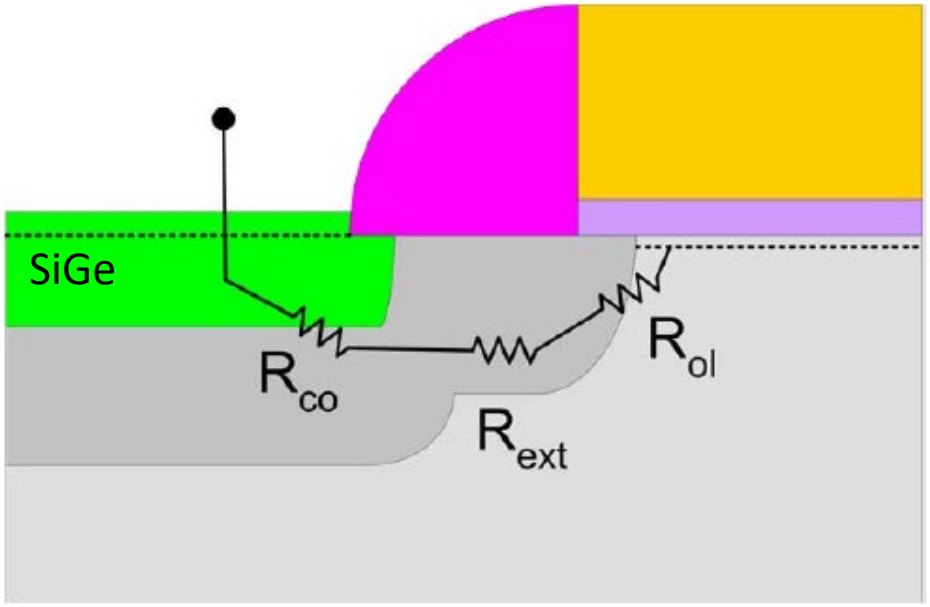
Equivalent Scaling Begins

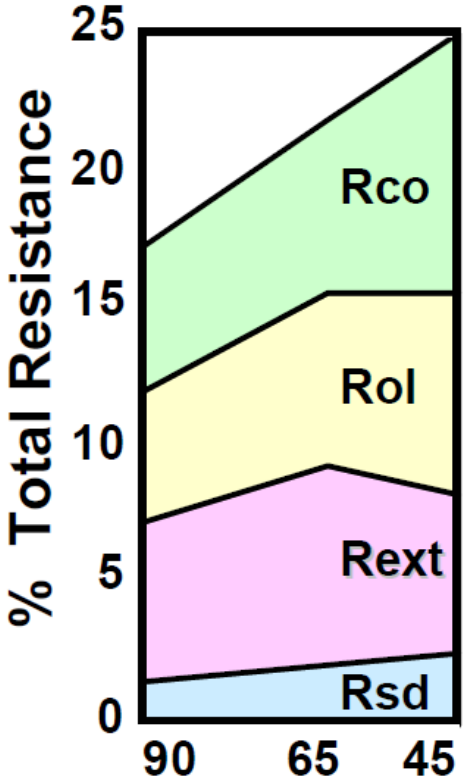


3 key transistor innovations that shaped this era of effective scaling

Lessons in serendipity embedded in each

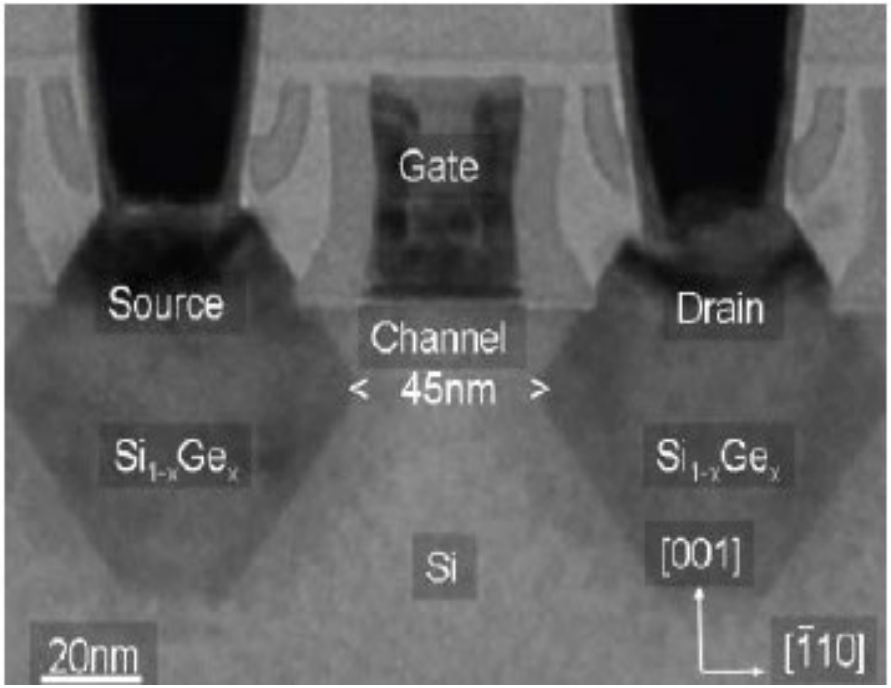
Elevated Source Drain

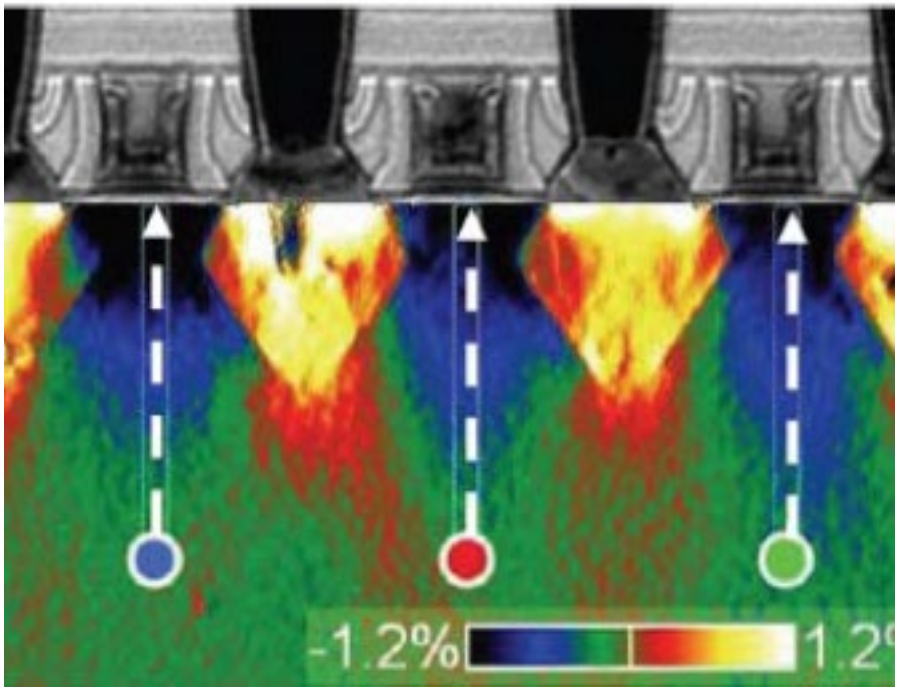




Series resistance gets bigger fraction of on-resistance

Embedded Source Drain

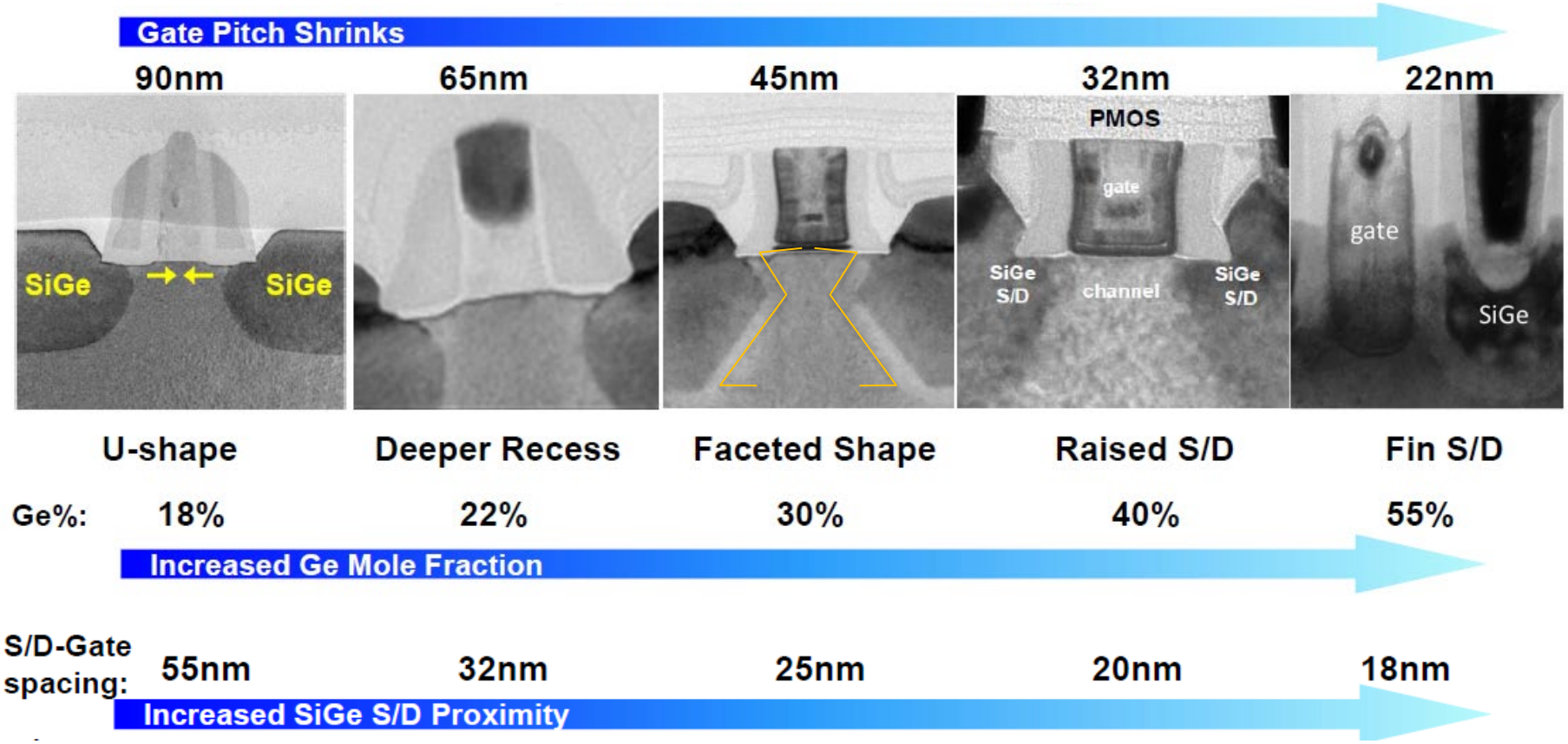




Hole mobility responds in a remarkable fashion

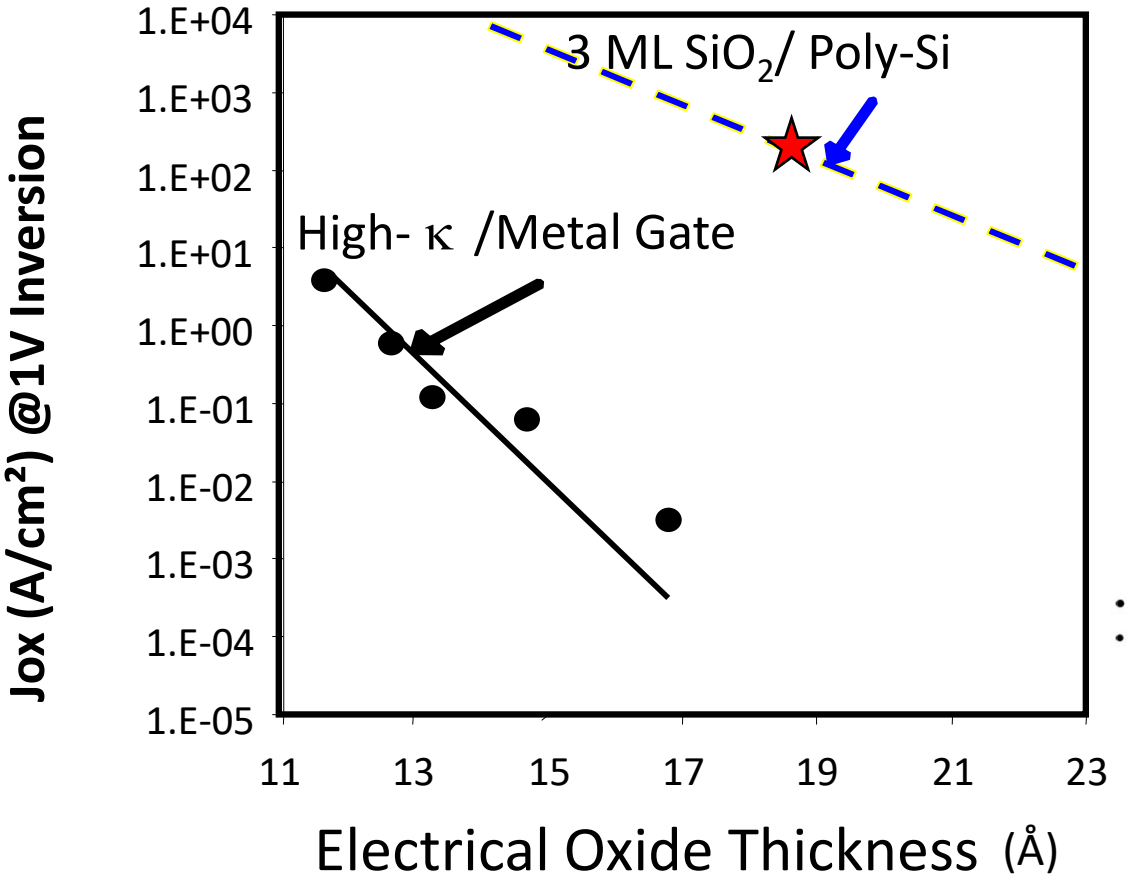
Local stressor in PMOS and does not affect NMOS

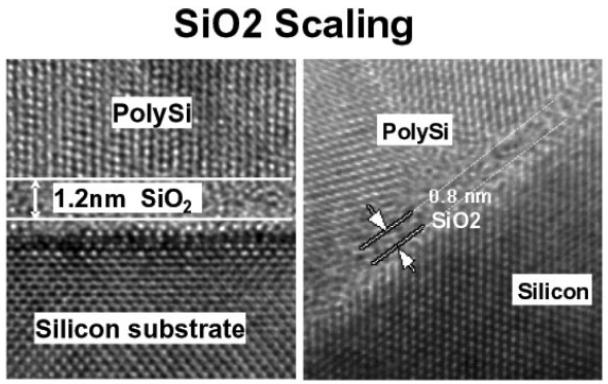
Local Stressor



SiGe S/D was intended for lowering external resistance
eSiGe S/D becomes a local stressor for the channel

High-k metal-gate



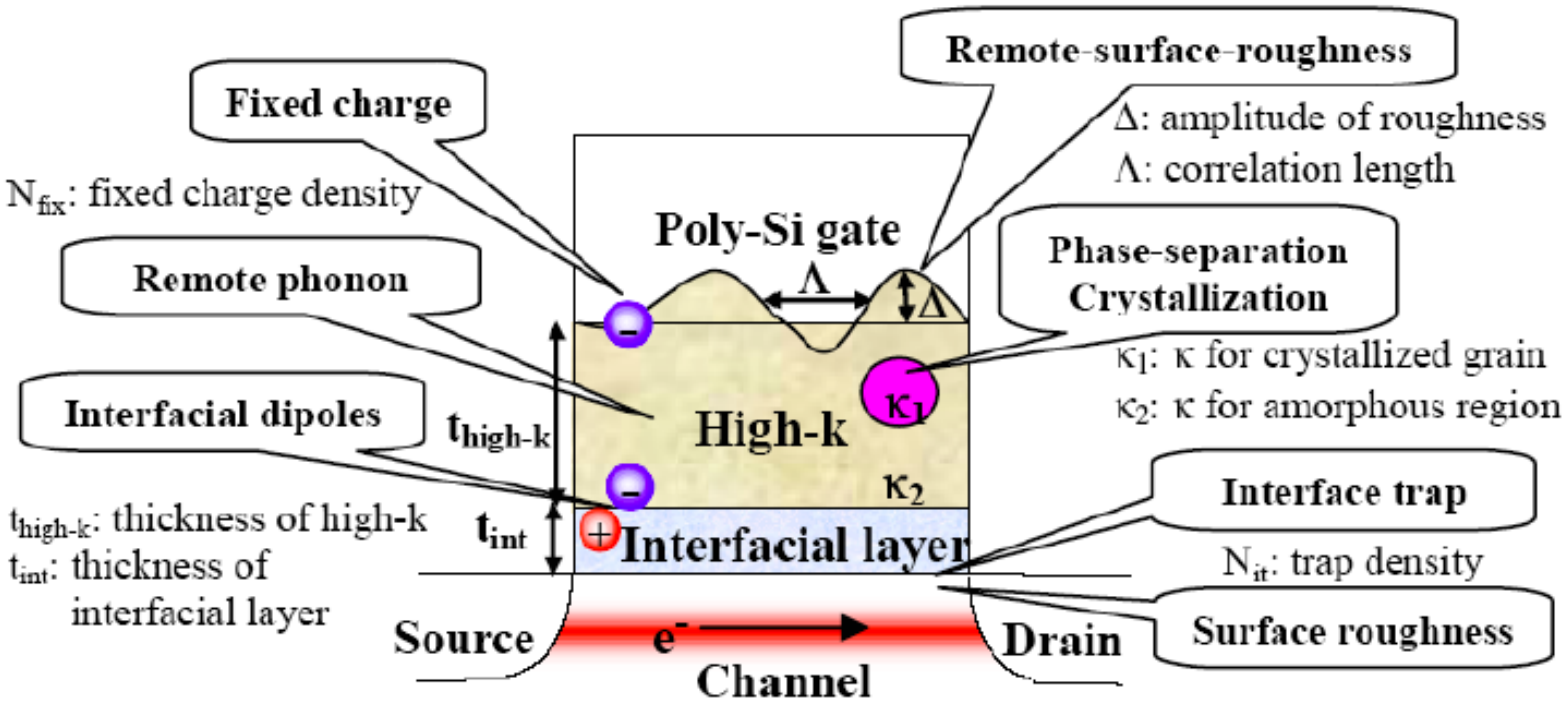


- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

Gate leakage increases with SiO_2 scaling -> running out of atoms

High-k (HfO_2) Gate Stack enables T_{elec} scaling with low gate leakage

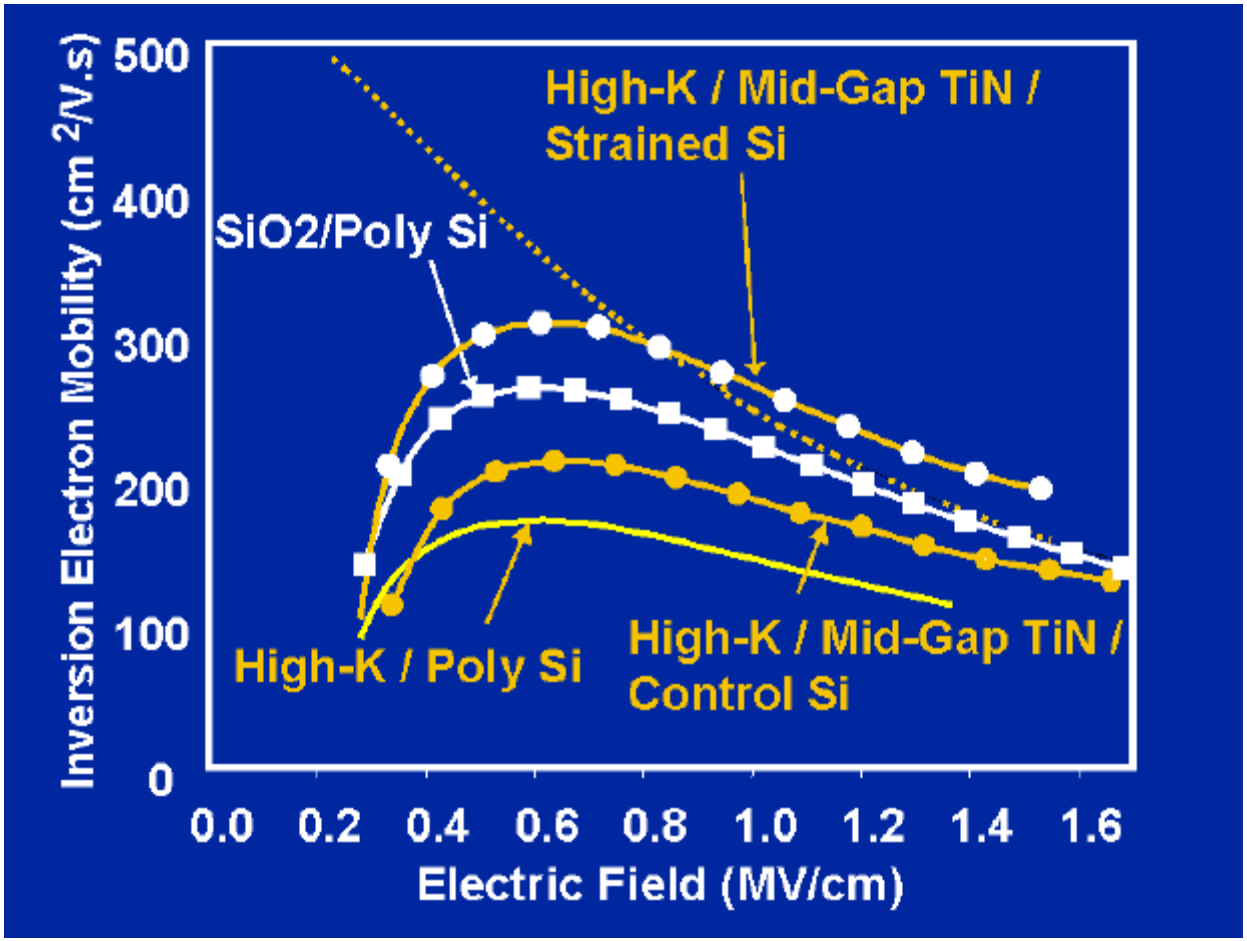
Gate Stack Challenges



S. Saito, et al., IEEE IEDM, Washington, DC, Dec., 2003.

Bulk & interface traps:	Poor reliability
Remote phonon scattering:	Poor mobility
Technology Integration:	Complexity and cost

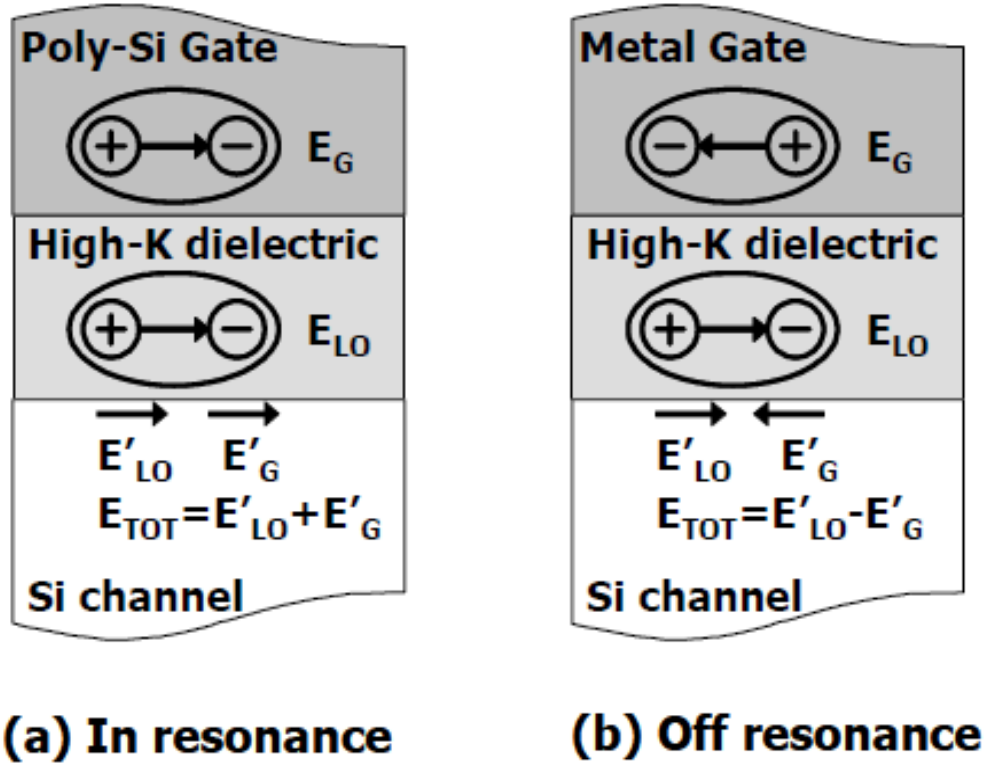
Strained Si + High-k / MG stack



Combined channel strain + high-k + metal gate to recover mobility

S. Datta, J. Kavalieros, R. Chau, M. Doczy *IEDM 2003*

Metal Gate Screening

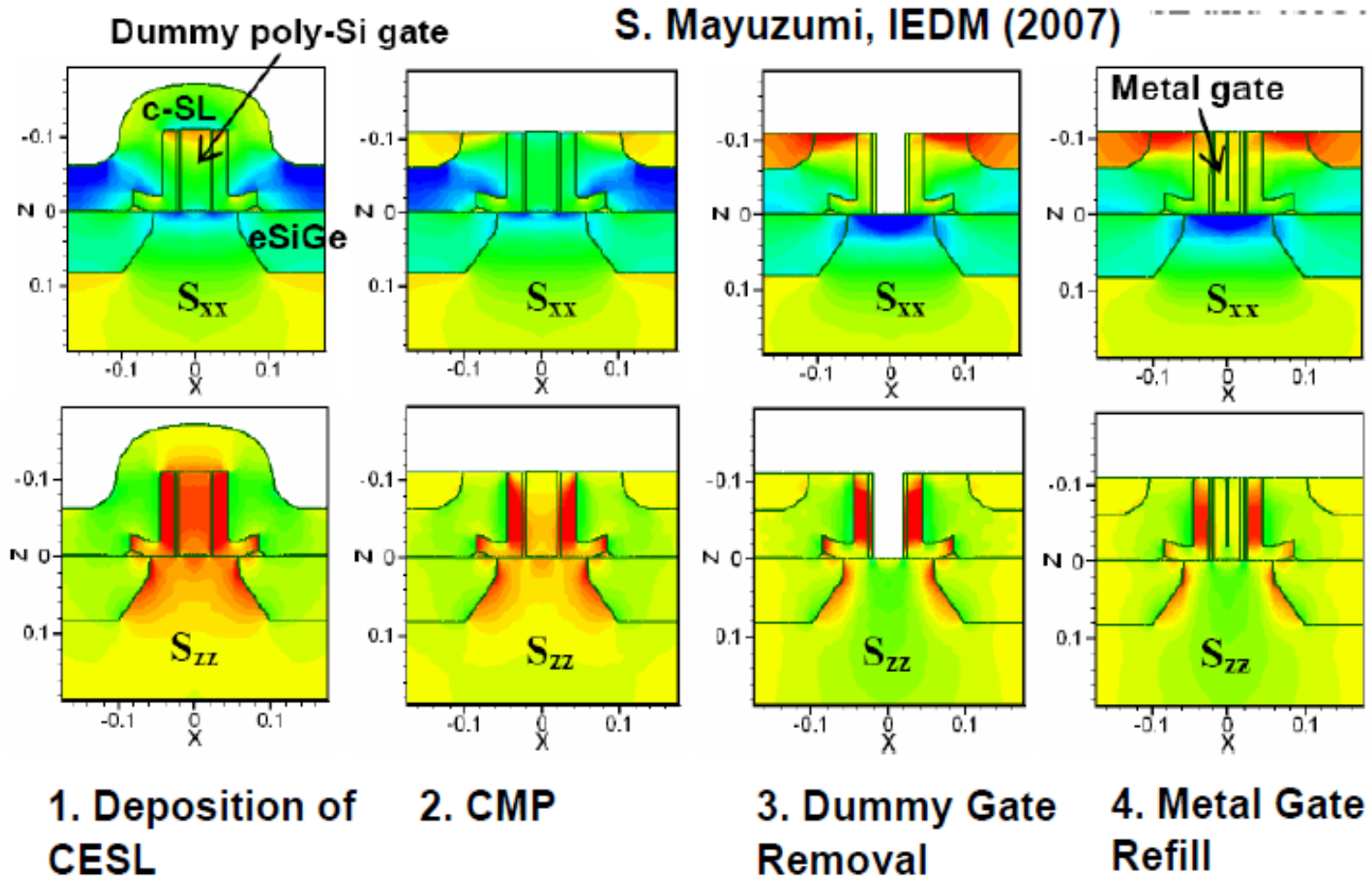


(a) In resonance **(b) Off resonance**

poly-Si gate plasmon frequency in resonance with HfO_2 dipoles degrading channel mobility

R. Chau, S. Datta, J. Kavalieros et al *INFOS 2005;* R. Kotlyar, M. Giles et al, IEDM 2004

Gate-Last Enhances Channel Strain

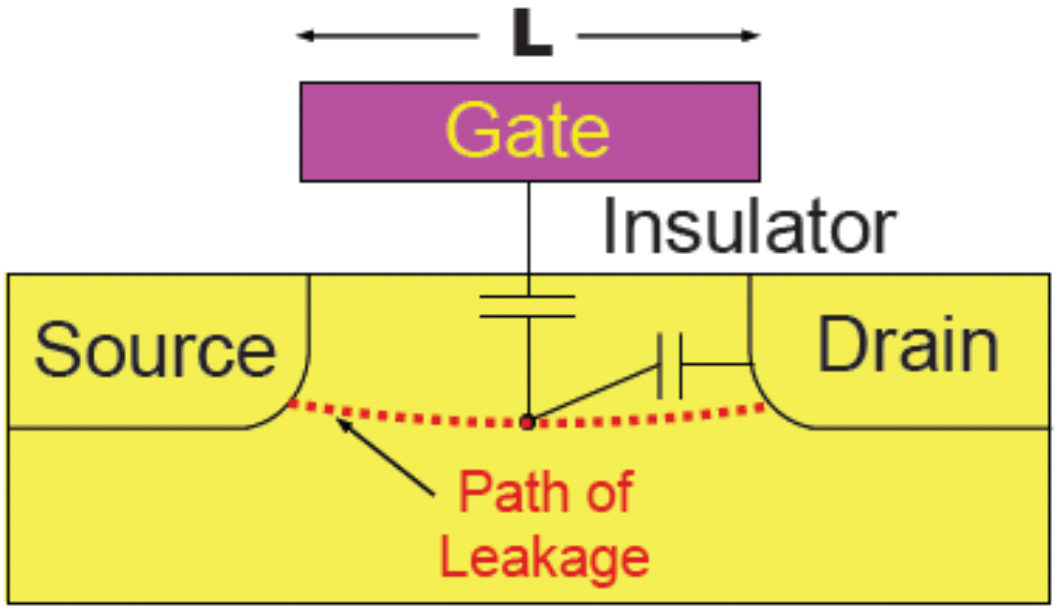


Gate last was intended for gate metal WF engineering

Longitudinal compressive strain ε_{xx} is enhanced

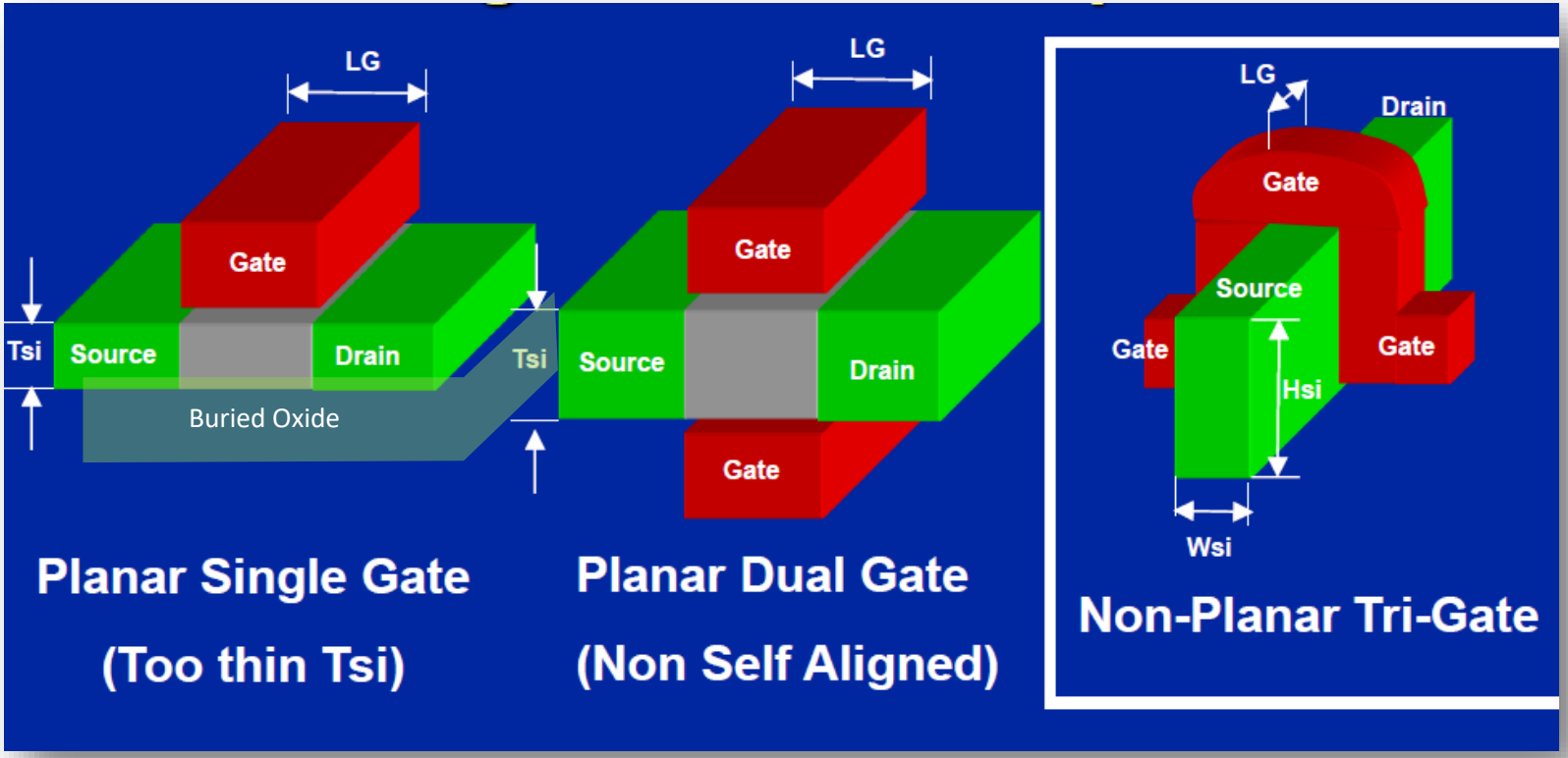
Replacement metal gate acts as effective stress enhancers

Multi-Gate Transistor



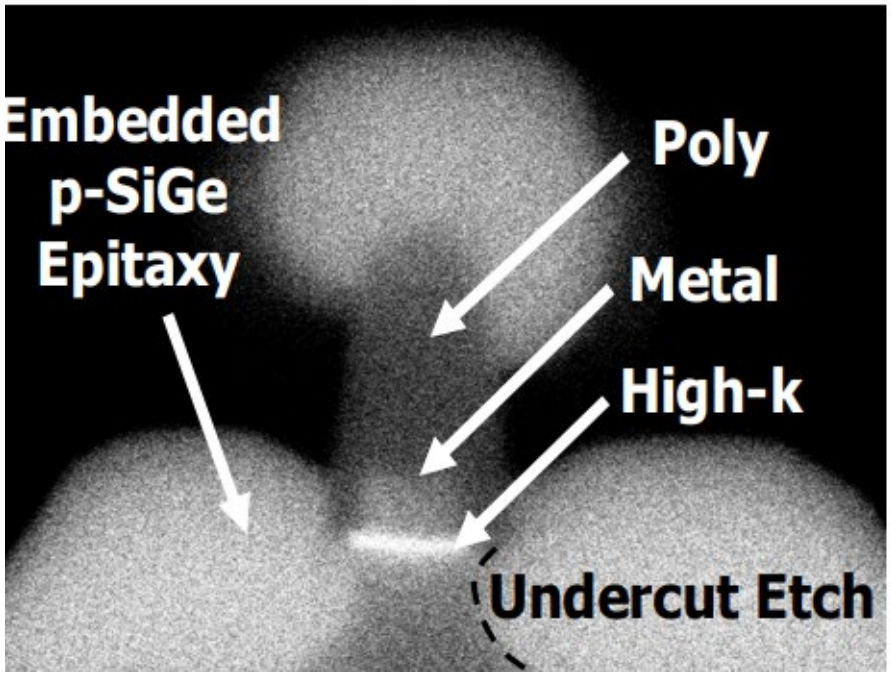
"Even thin insulators cannot control leakage paths that are away from the gate"

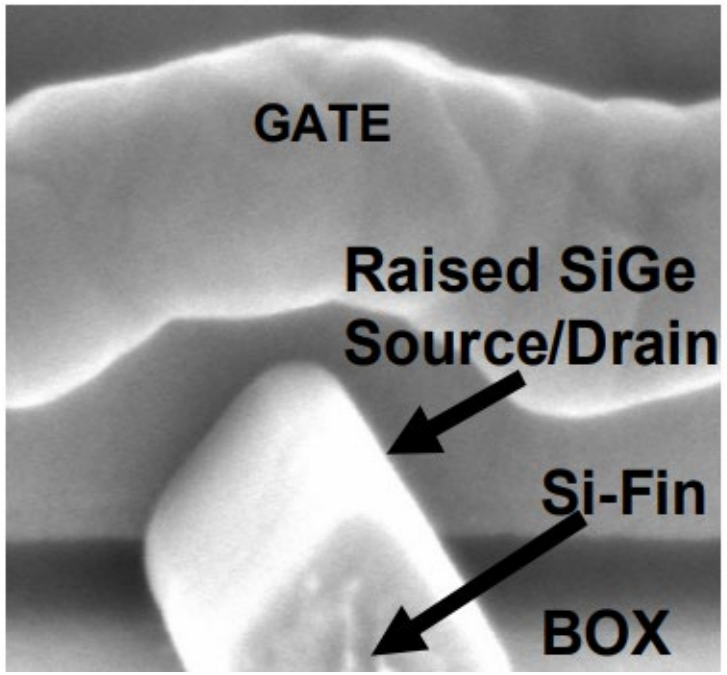
From Single-Gate to Tri-Gate



Ultra thin body, double-gate or Tri-Gate architecture allows gate length scaling

High Performance Tri-gate transistors

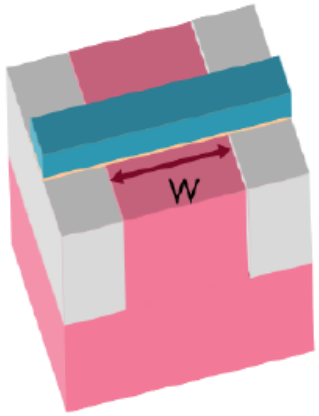


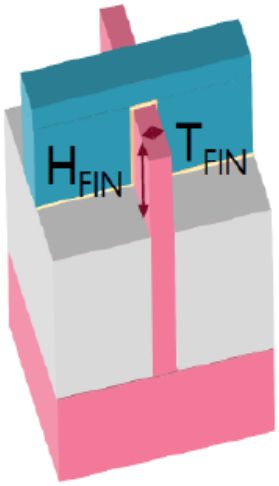


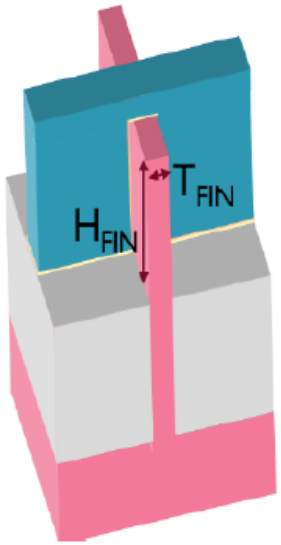
Combine the benefits of fully depleted Tri-gate architecture with high-k /metal gate stack, strain and crystallographic plane engineering

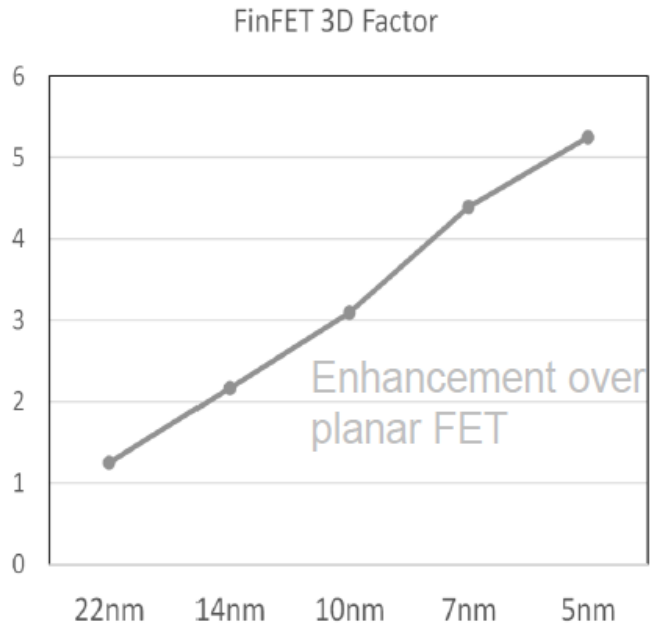
J. Kavalieros, S. Datta, B. Doyle, R. Chau *VLSI Symp on Tech 2006*

Electrical Width





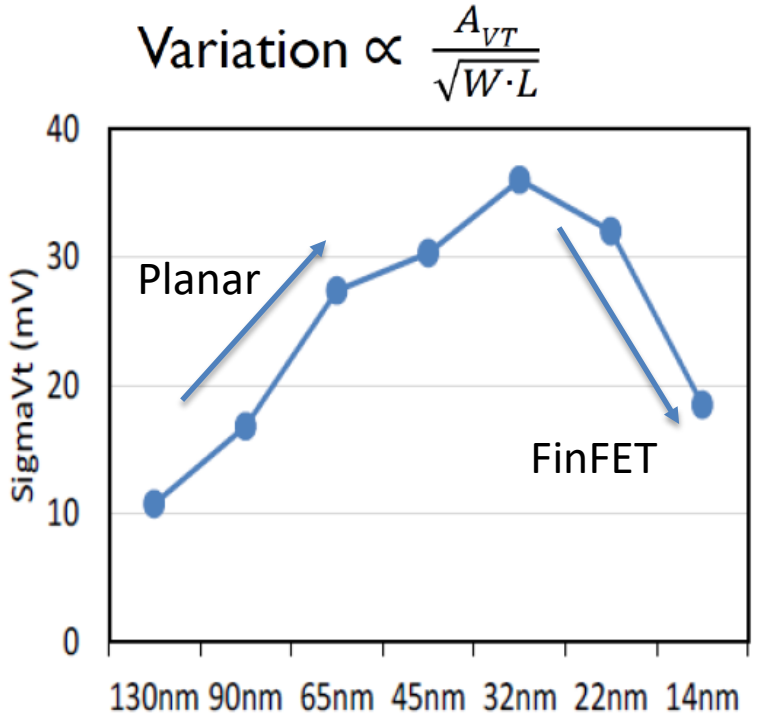




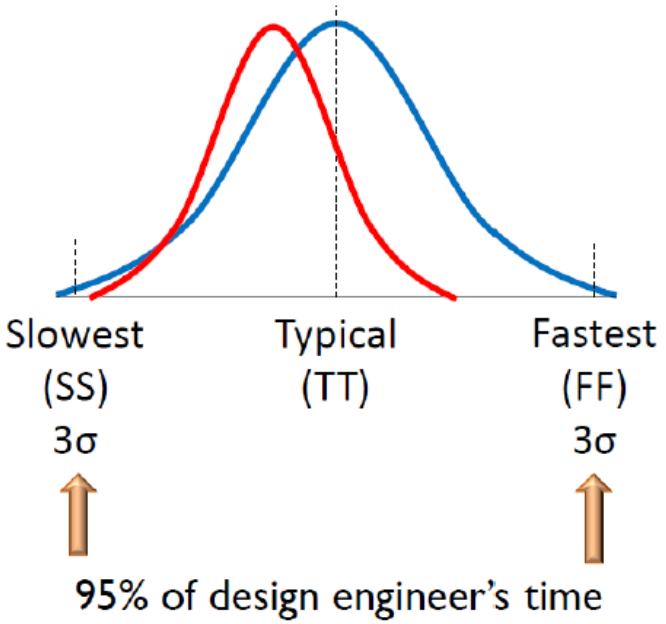
$$\text{3D Factor} = \frac{\text{Total width of FinFET}}{\text{Planar width used}} = \frac{2 \times H_{FIN} + T_{FIN}}{\text{Fin Pitch}}$$

Part of Tri-gate appeal is improved electrostatics
Other part is **folded width**

Improved Variation



S. Natarajan (Intel), IEDM 2014

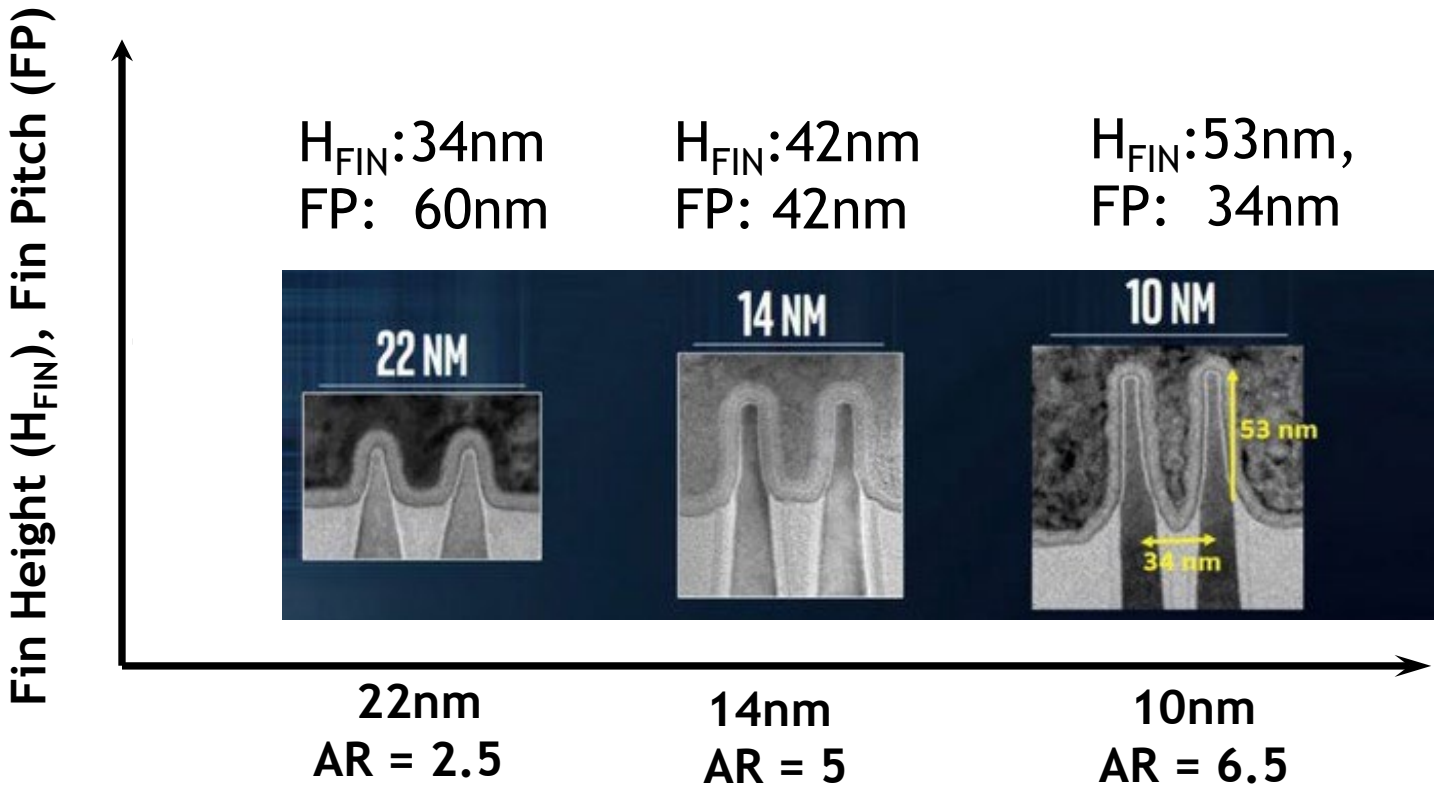


Greg Yeric (ARM), IEDM 2015

Tri-gate was intended primarily for electrostatics

FinFET 3D factor enabled effective width scaling with improved variation

FinFET evolution



Fin height and fin pitch evolution over last 3 generations

Academic Career Begins ….

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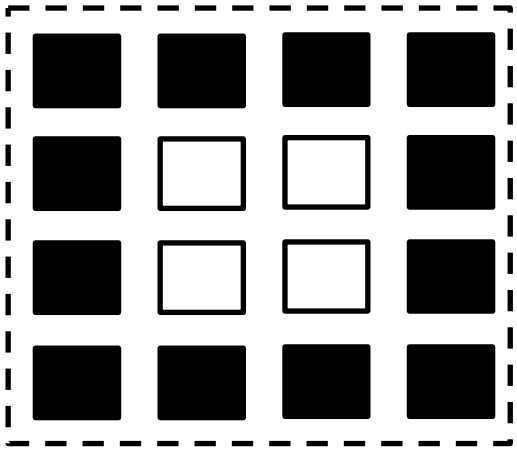
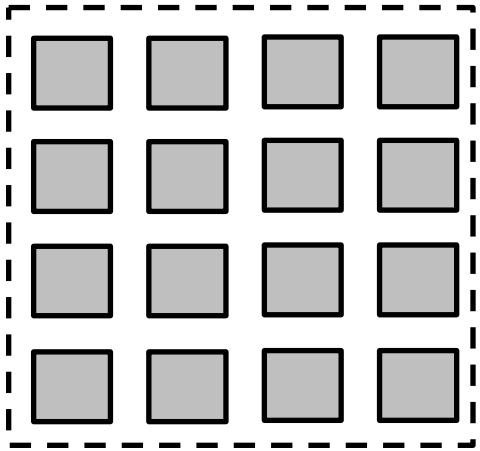
From left, Suman Datta, professor of electrical engineering at Penn State, and doctoral student Dheeraj Mohata, in the University's Nanoscale Devices at Circuits Lab. On the screen behind them is a model of their heterojunction tunneling field effect transistor (TFET).
IMAGE: Penn State

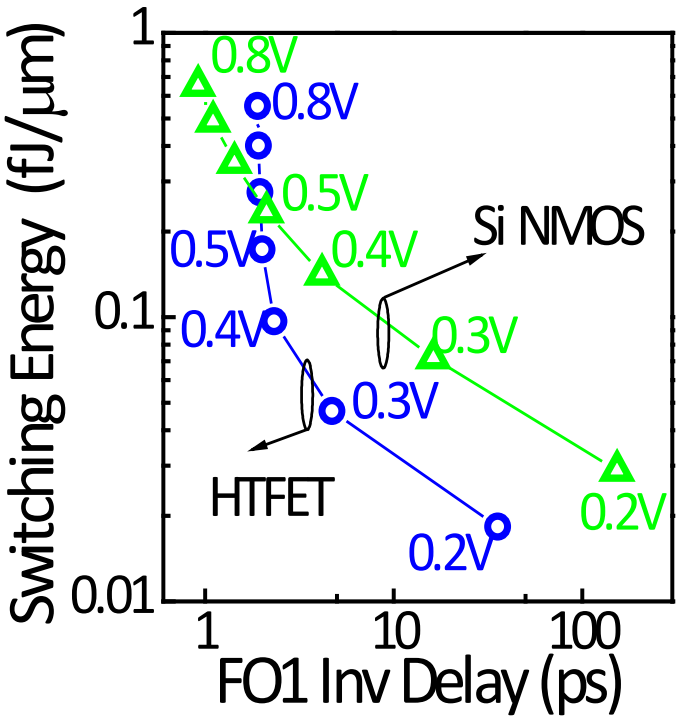
Steep Slope FETs: Dark to Dim Silicon



Dark silicon (MOSFET)

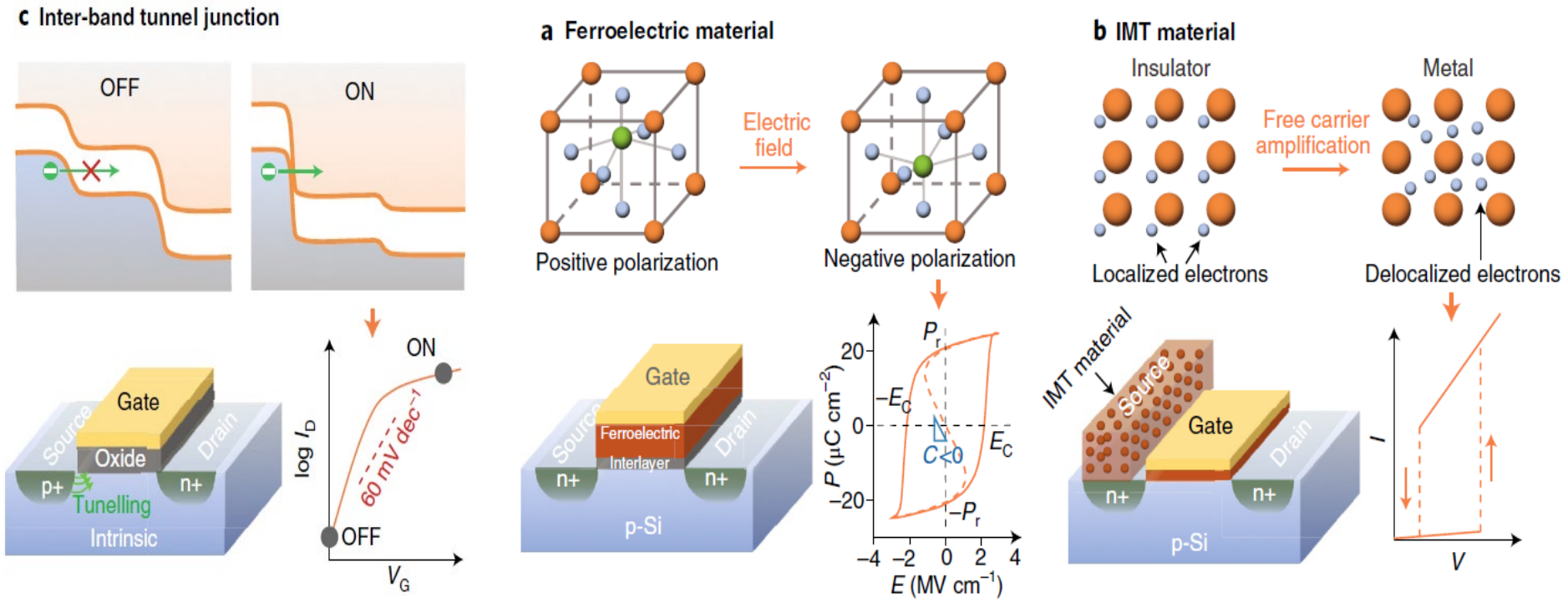


Dim silicon (Steep Slope FET)



Steep slope *(<kT/q)* transistors to operate with higher performance than MOSFETs at lower supply voltages

Steep slope FETs



Inter-band tunneling, Ferroelectric negative capacitance, Insulator-metal phase transitions to enable transistors with *steep slope and low voltage operation*

Heterojunction Tunnel FETs

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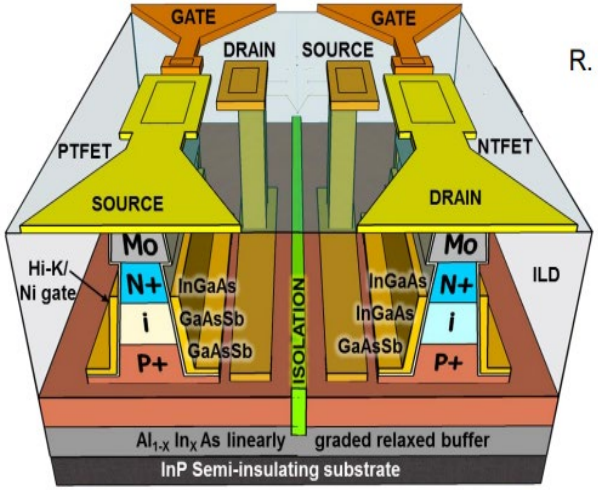
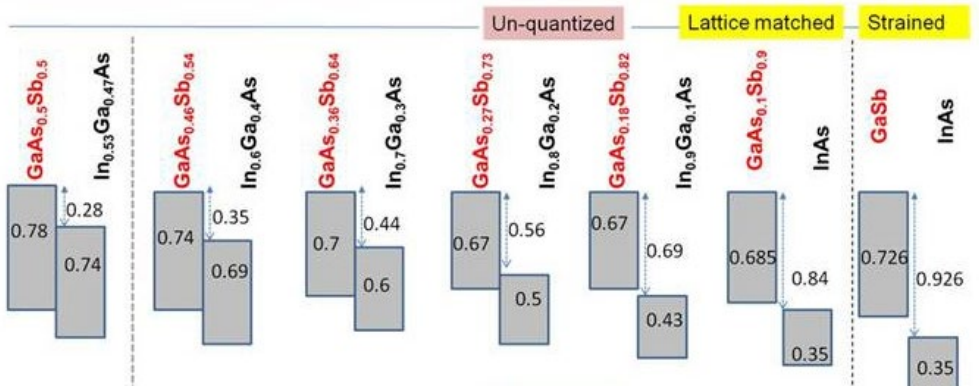
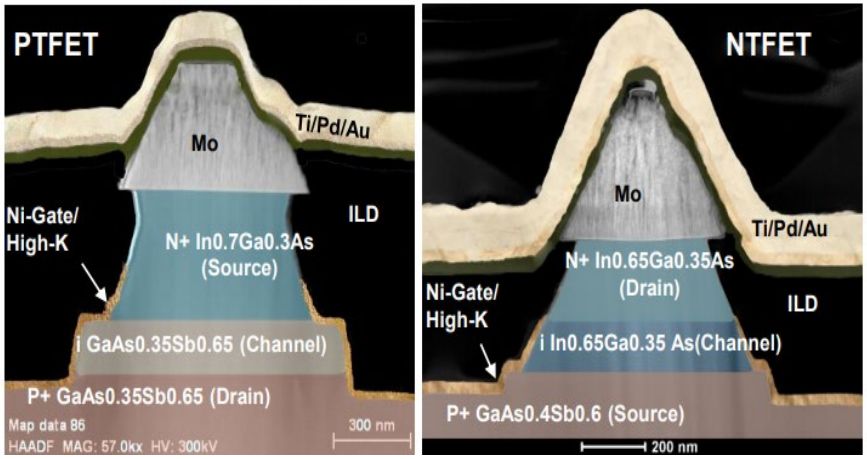
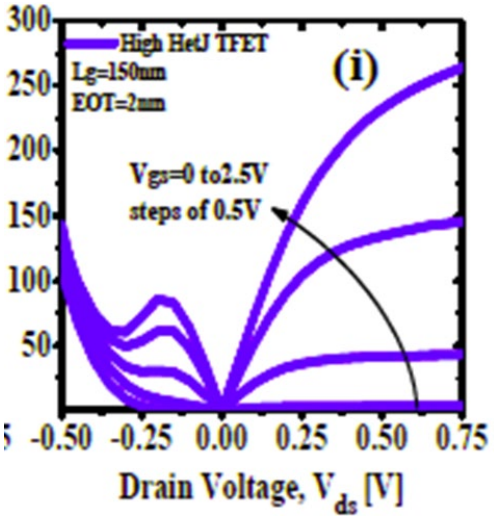


R. Pandey, VLSI Symp 2015





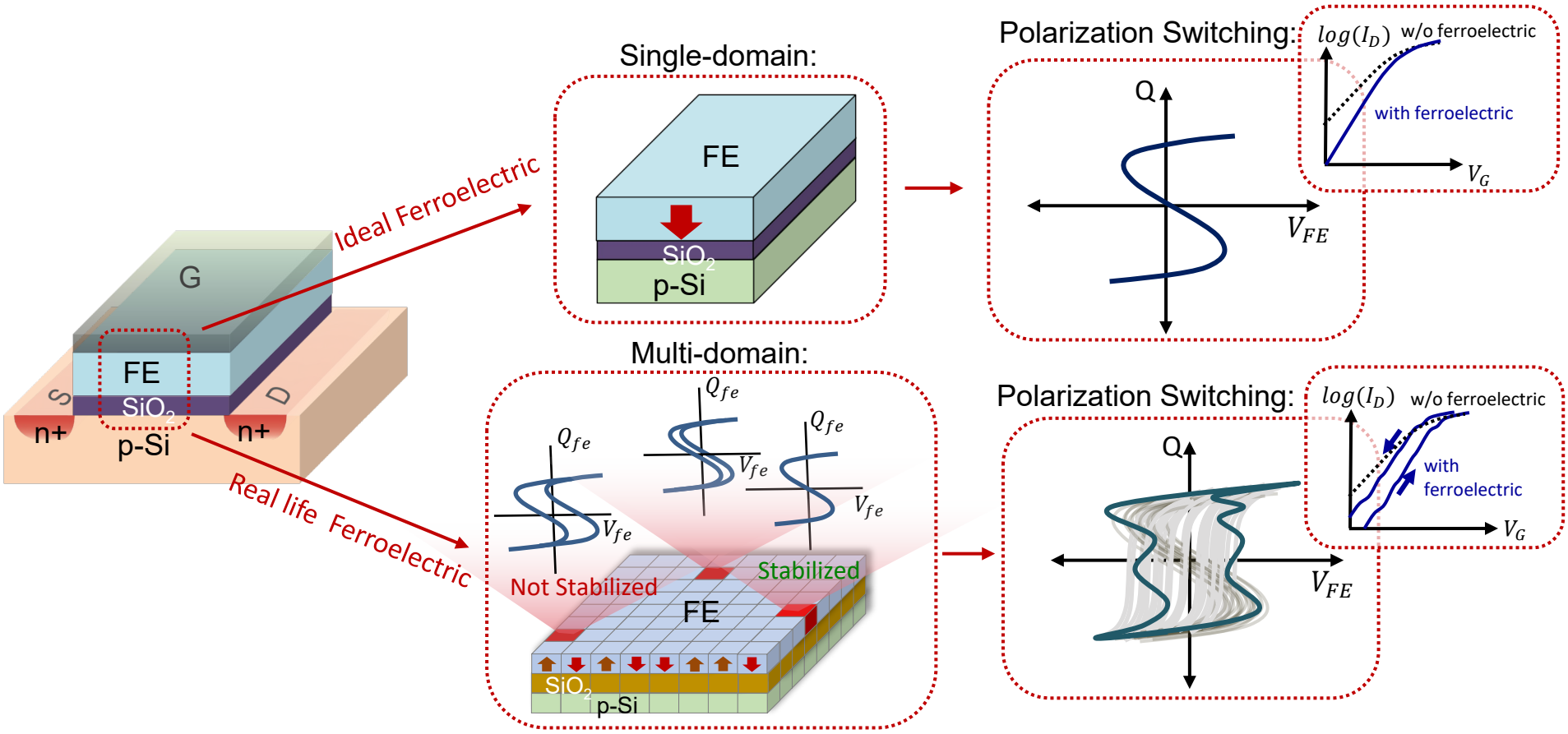


Tunnel FETs can beat sub-threshold CMOS

Risk: On-current limitation to support high-performance computing

R. Bijesh, S. Datta, *IEDM 2013*

Ferroelectric NCFETs

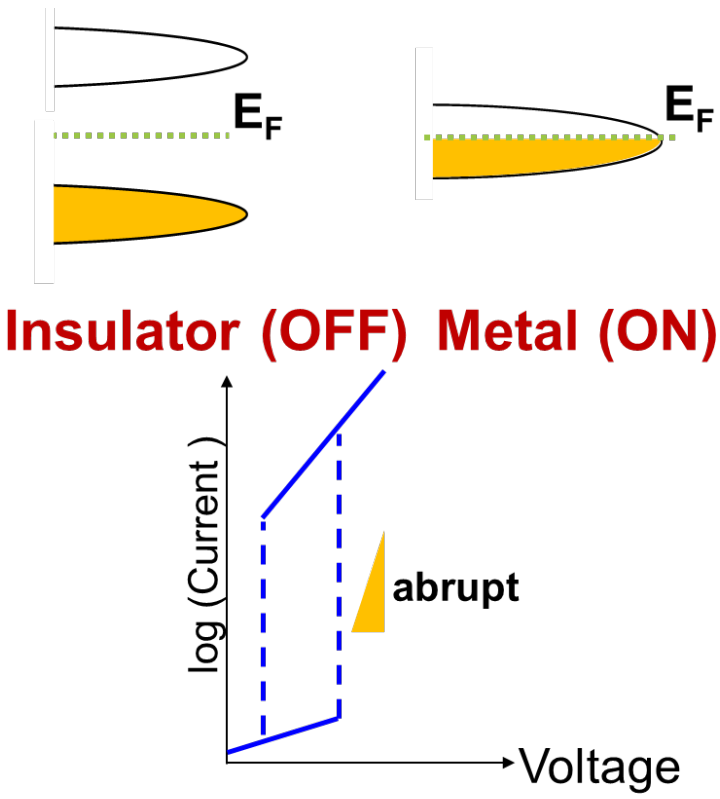


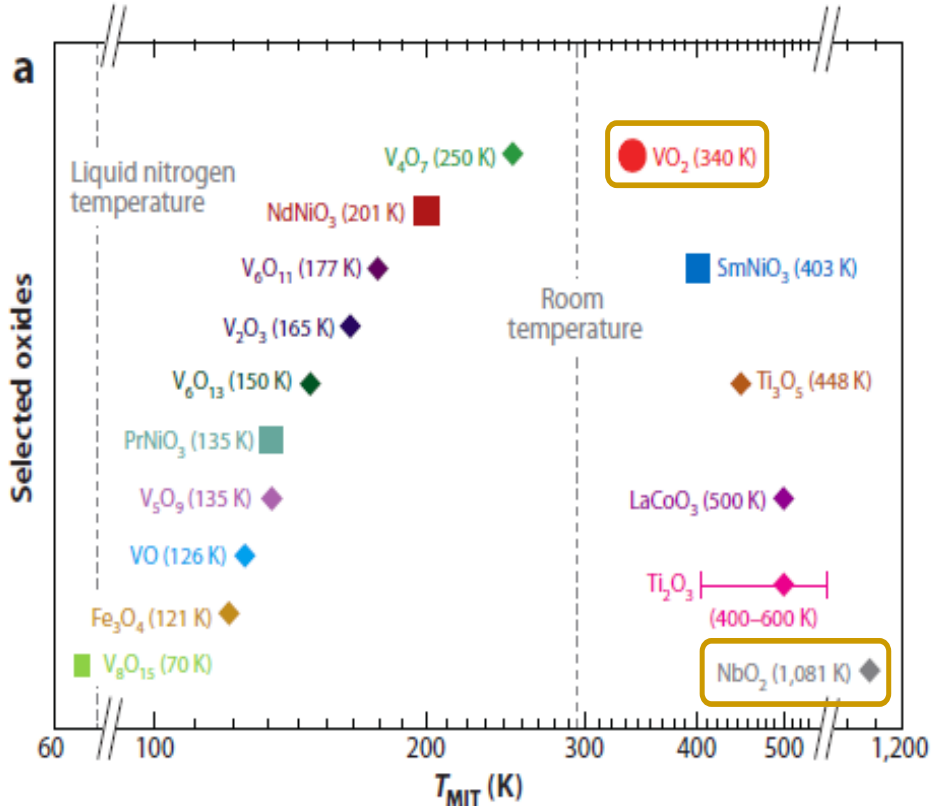
NCFETs can beat super-threshold CMOS

Risk: Stabilization of negative capacitance in multi-domain Ferroelectric

J. Gomez, A. Khan, S. Datta *IEDM 2019*

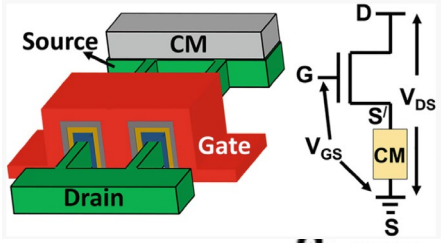
Phase Transition in Correlated Oxides

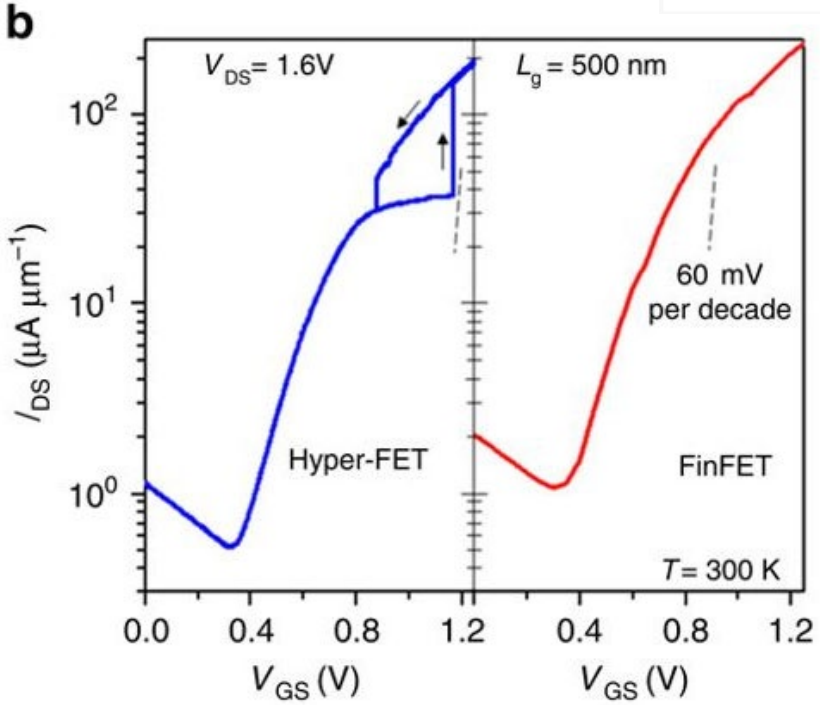


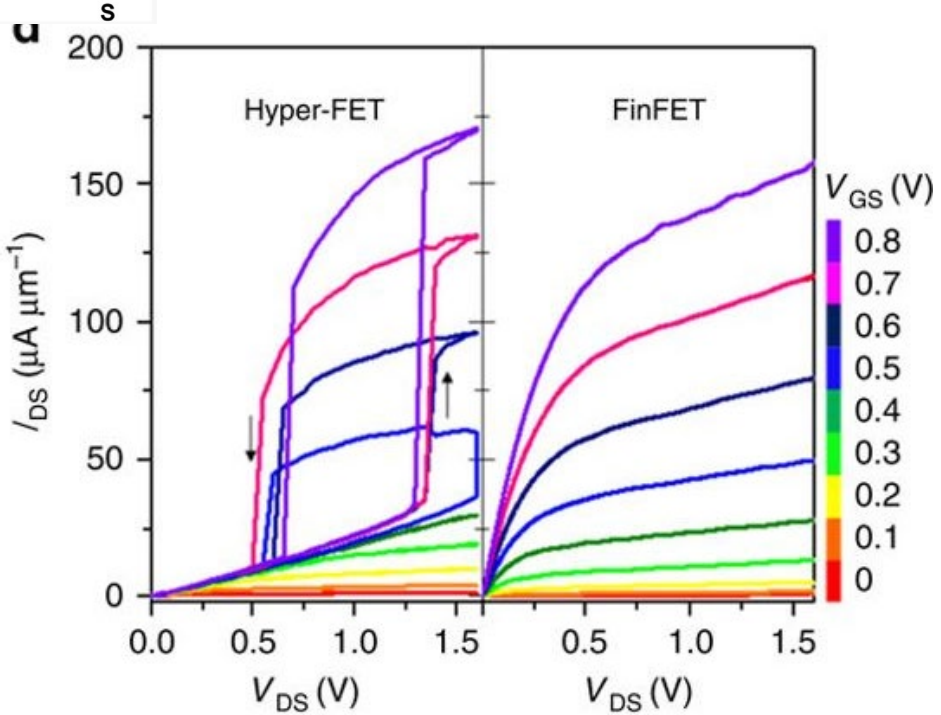


Electrically induced collapse of transport gap around the Fermi level

Phase Transition FETs







Phase Transition FETs show on-off ratio gain over traditional FETs

Risk: phase transition is triggered at high current level in nanosec time scale

N. Shukla, D. Schlom, S. Datta *et al Nature Comm 2015*

Tunnel FET to MIS Tunnel Contact

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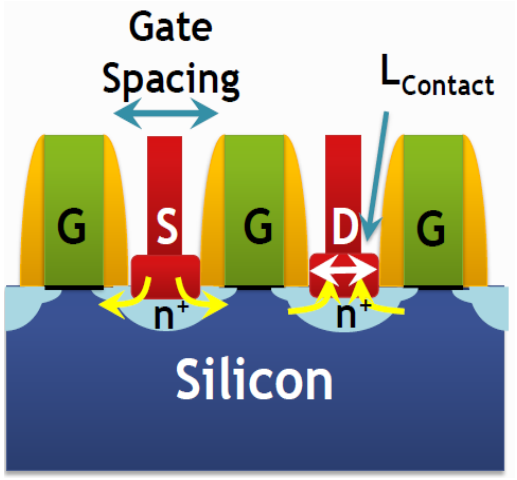
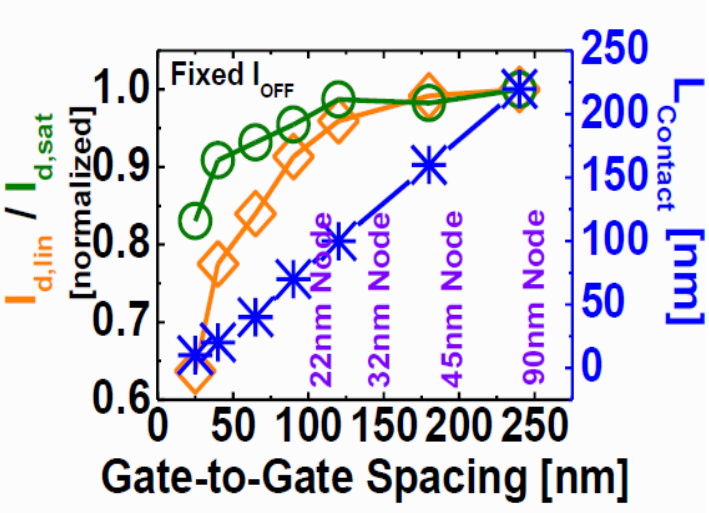
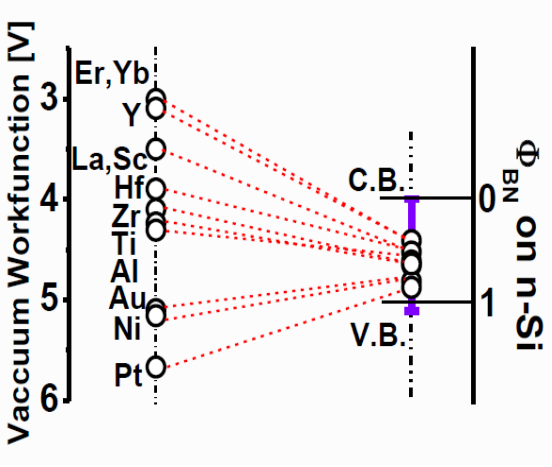
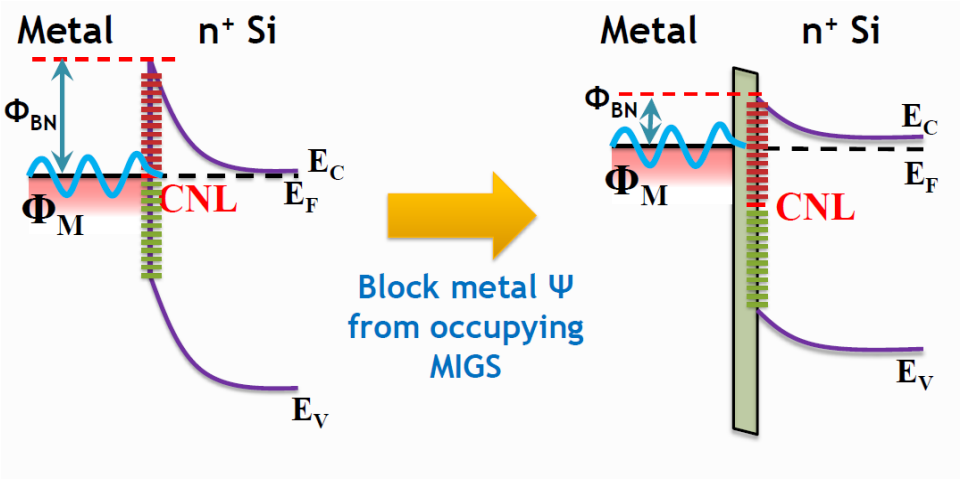






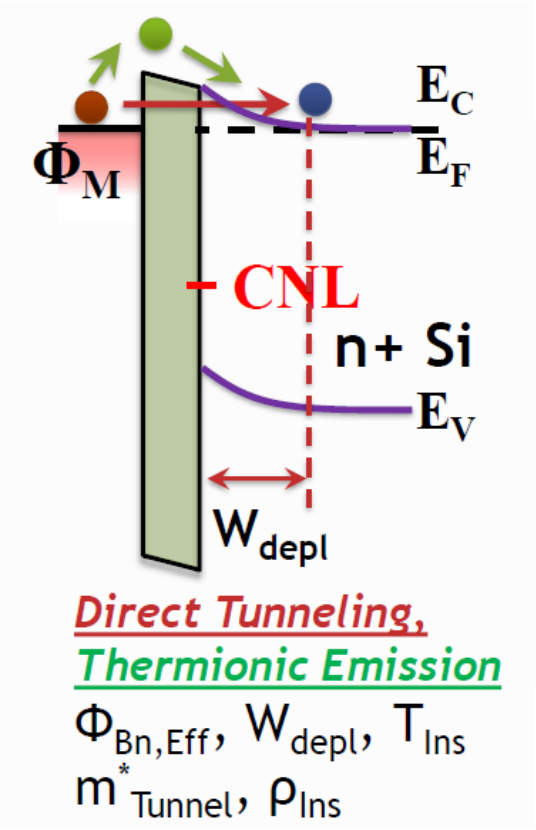


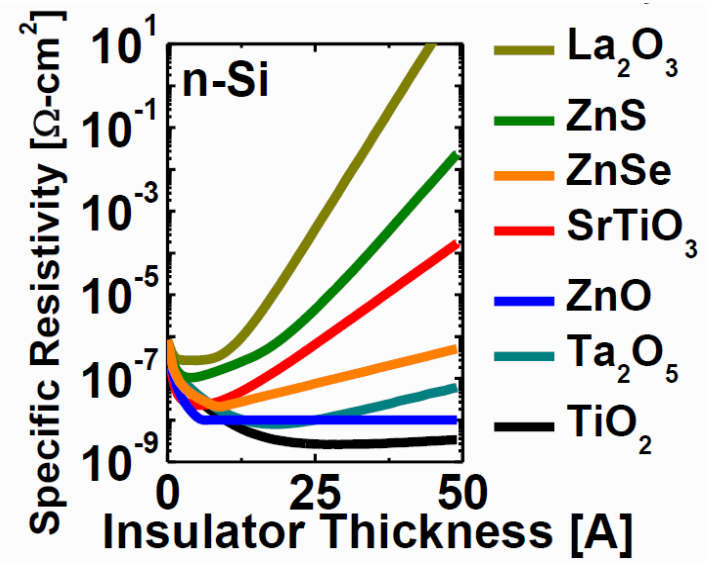
$$\rho_c \propto \exp\left(\frac{\Phi_{BN}}{\sqrt{N_D}}\right)$$

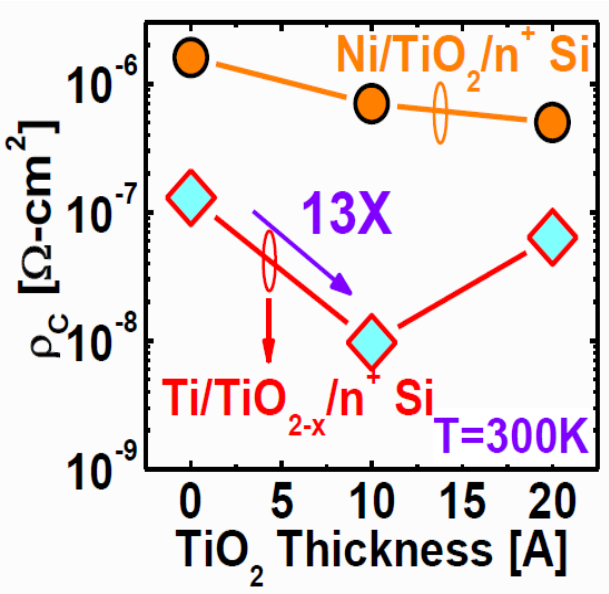
Fermi level pinning prevents barrier height reduction

Insert an insulator between metal and silicon

MIS Tunnel Contact







- ρ_C = 9.1x10^{-9} Ω-cm^2 obtained using M-I-S contact

A. Agrawal, S. Datta et. al., *Appl. Phys. Lett.* 2012

NCFET to Low EOT MOSFET

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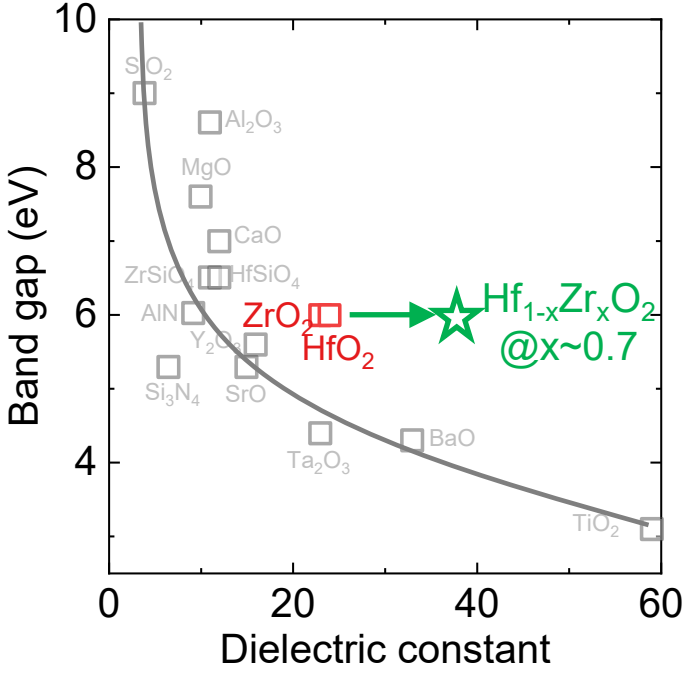
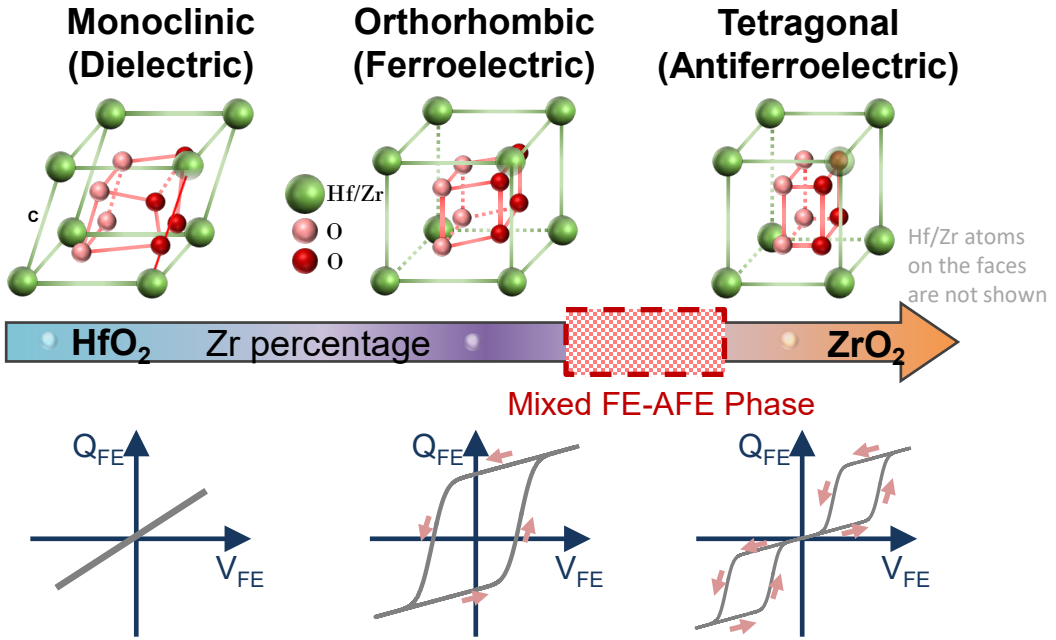
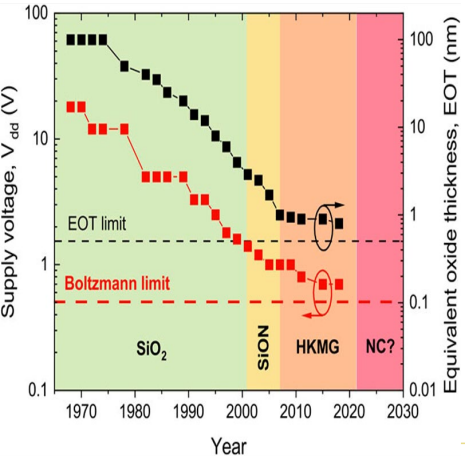
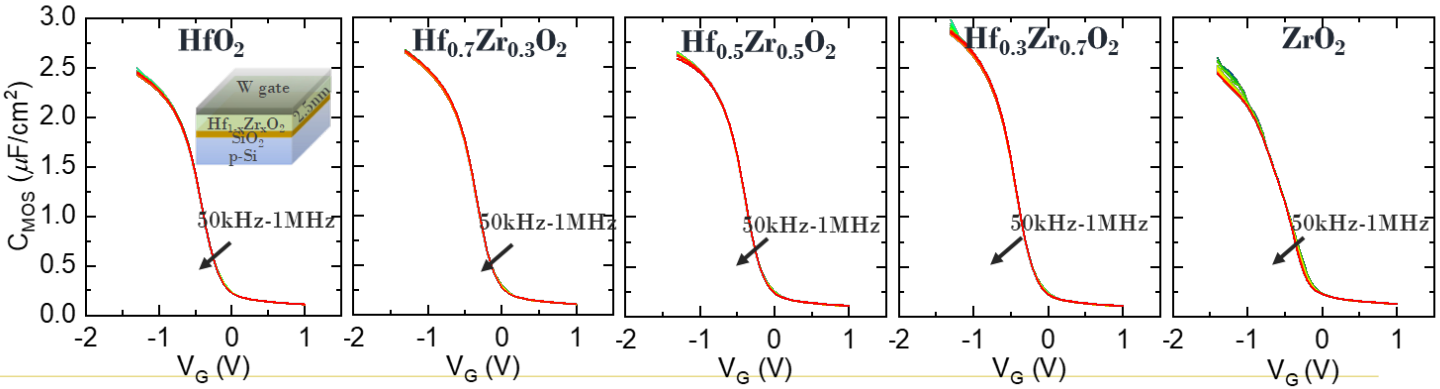


FE to AFE Phase transition in $Hf_{1-x}Zr_xO_2$



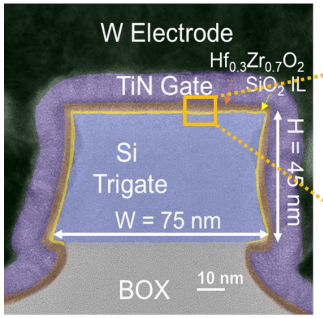


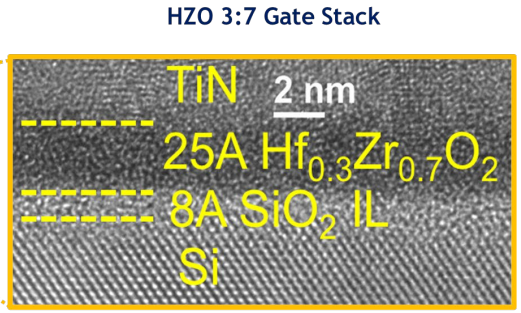
2.5nm oxide

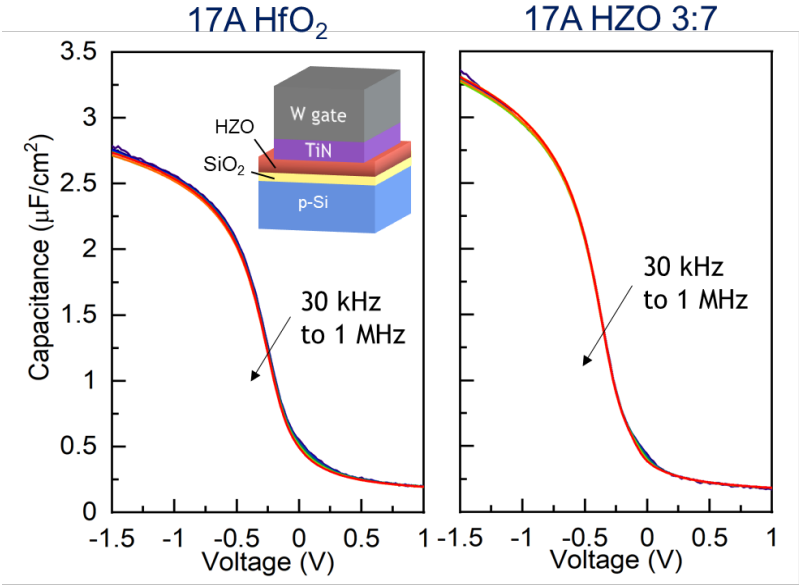


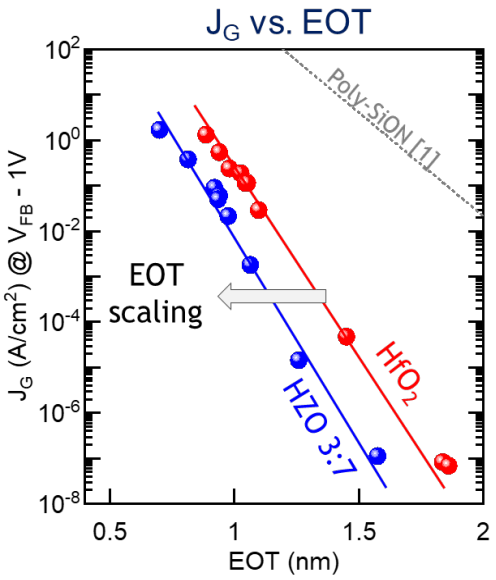
K. Ni, S. Gupta, S. Datta *IEDM 2019*

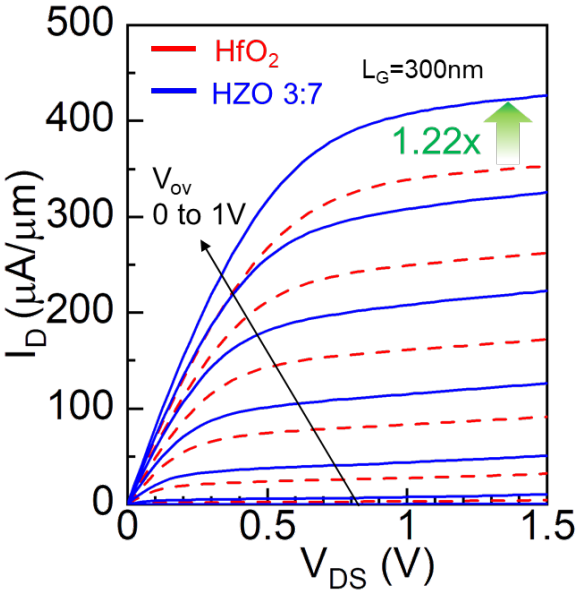
Thinner EOT, higher g_m MOSFET











22% EOT scaling without mobility degradation was demonstrated in Tri-gate FETs with mixed FE-AFE phase higher-κ dielectric (70% Zr-doped HfO_2) gate-stack

Phase FET to Phase Transition Nano Oscillator

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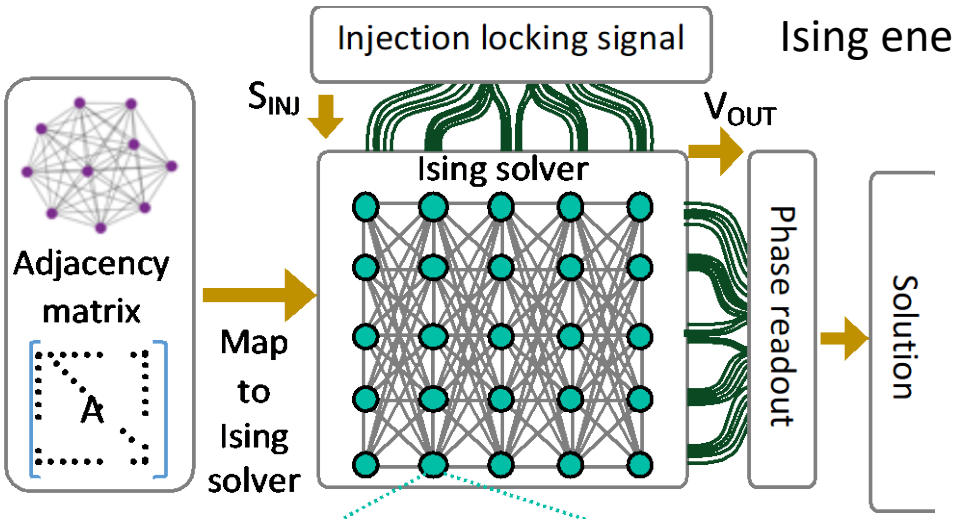
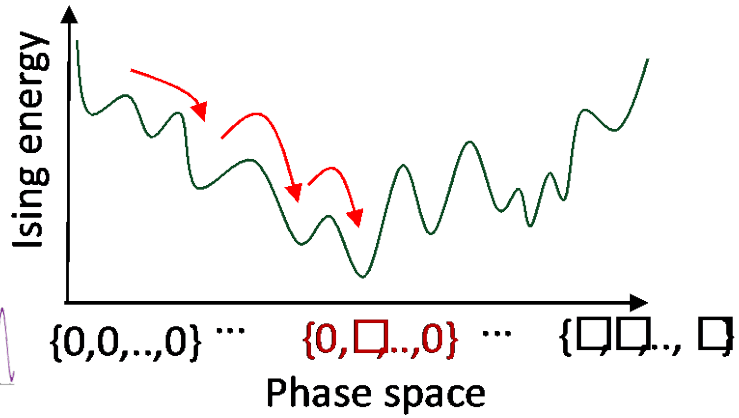
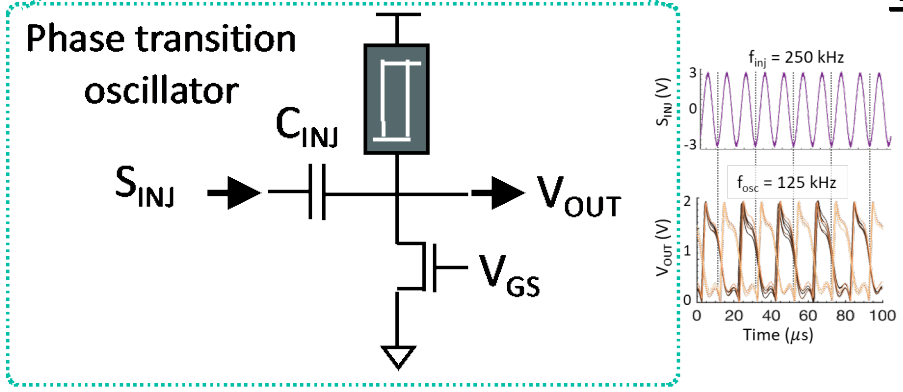


Ising energy: $H = -\sum J_{ij} S_i S_j$

Classical annealing can be utilized for ground-state search





Harness continuous-time dynamics of a network of coupled phase transition oscillators to construct an electronic *Ising Hamiltonian solver operating at room temperature*

Phase FET to Phase Transition Nano Oscillator

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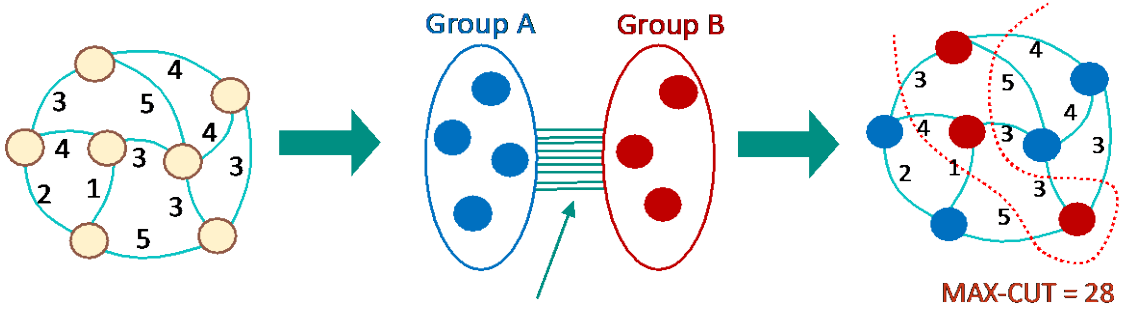
MAX-CUT Problem:

Partition graph to maximize

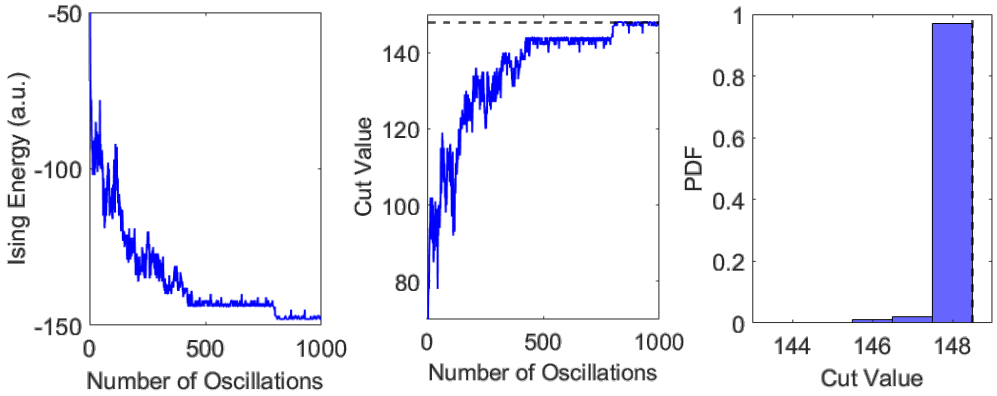
weights of edges crossing the cut



Map MAX-CUT to Ising Model

- Represent nodes as spins s_i
- Represent edges as "antiferromagnetic" coupling
- Minimizing Ising energy

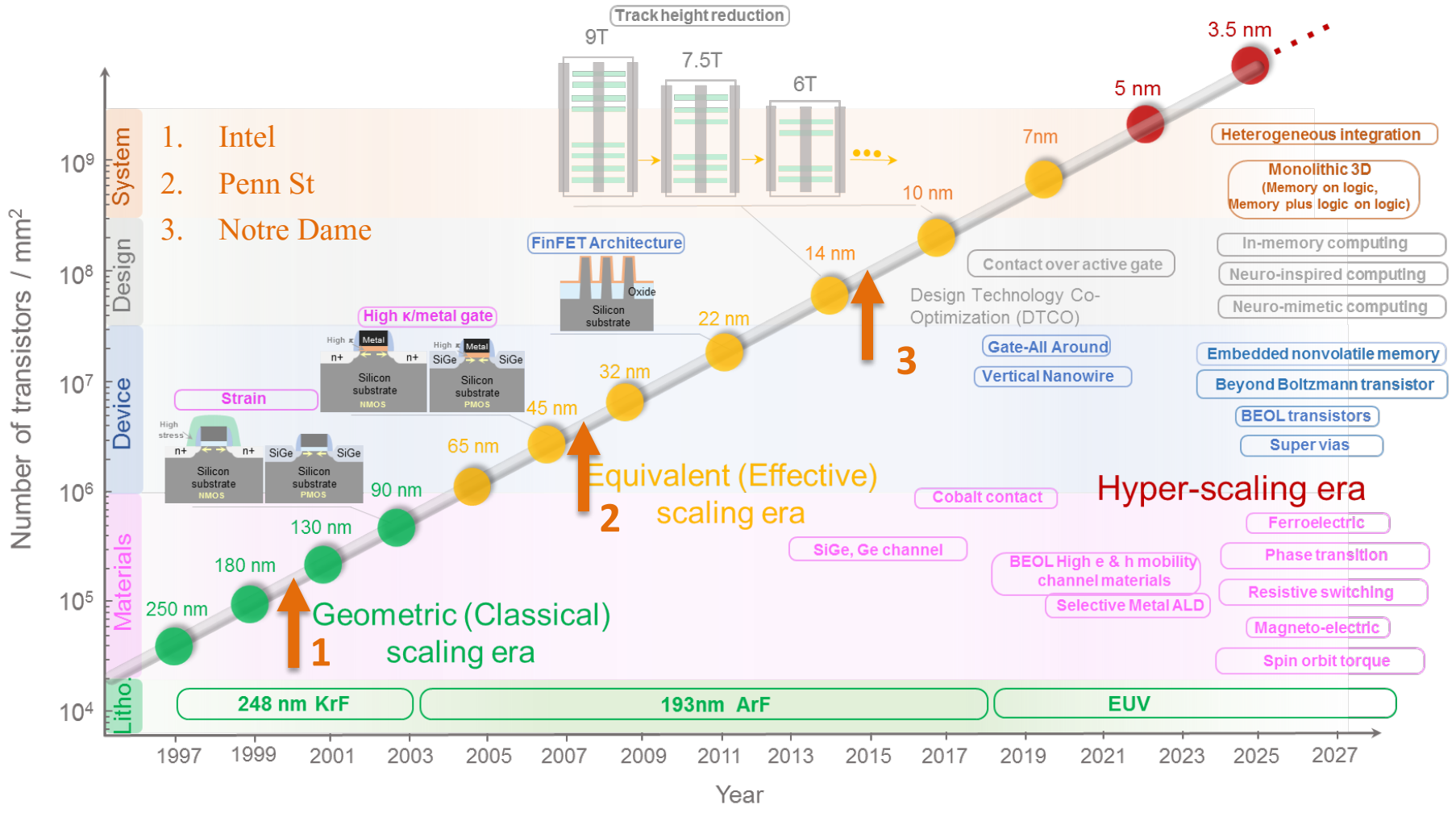
$$H = -\sum_{i<j} W_{ij} s_i s_j$$



Use coupled oscillator network to efficiently solve Max-Cut Problem

S.Dutta, A. Khanna, S. Datta et al Nature Electronics 2021

Transistor Scaling slowing down ?



Need a holistic approach to semiconductor research

S. Salahuddin, K. Ni, and S. Datta, *Nature Electronics 2018*

Compute Performance Gain

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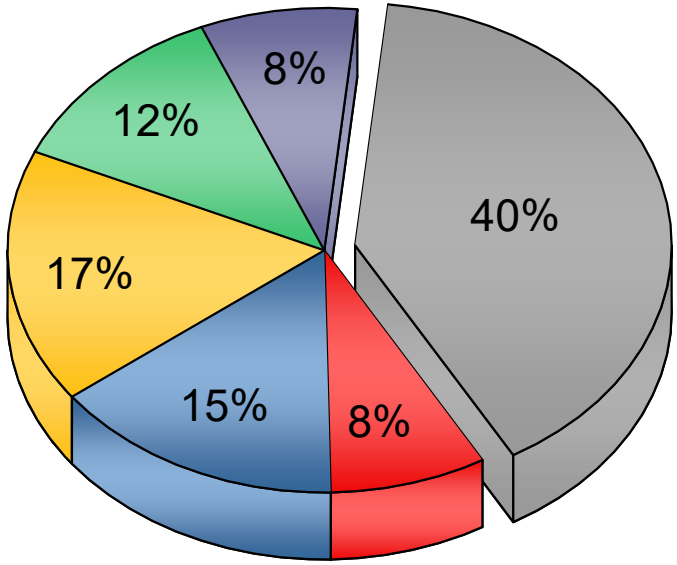
Compilers
Power Management
Microarchitecture

- Software Advancement
- Integration of system components
- Architectural Efficiency



Process Technology

- Higher performance, denser logic transistors
- Back-end-of-line RC reduction

Additional Die Size
Additional TDP

- Bigger Die
- Increased thermal design point

60% of compute performance gain over last decade came from advances in process technology, die size increase and thermal design point

Source: Lisa Su (AMD), ERI DARPA Summit, 2019

ASCENT
Applications and Systems Driven Center for Energy-Efficient Integrated Nanotechnologies

ascent.nd.edu

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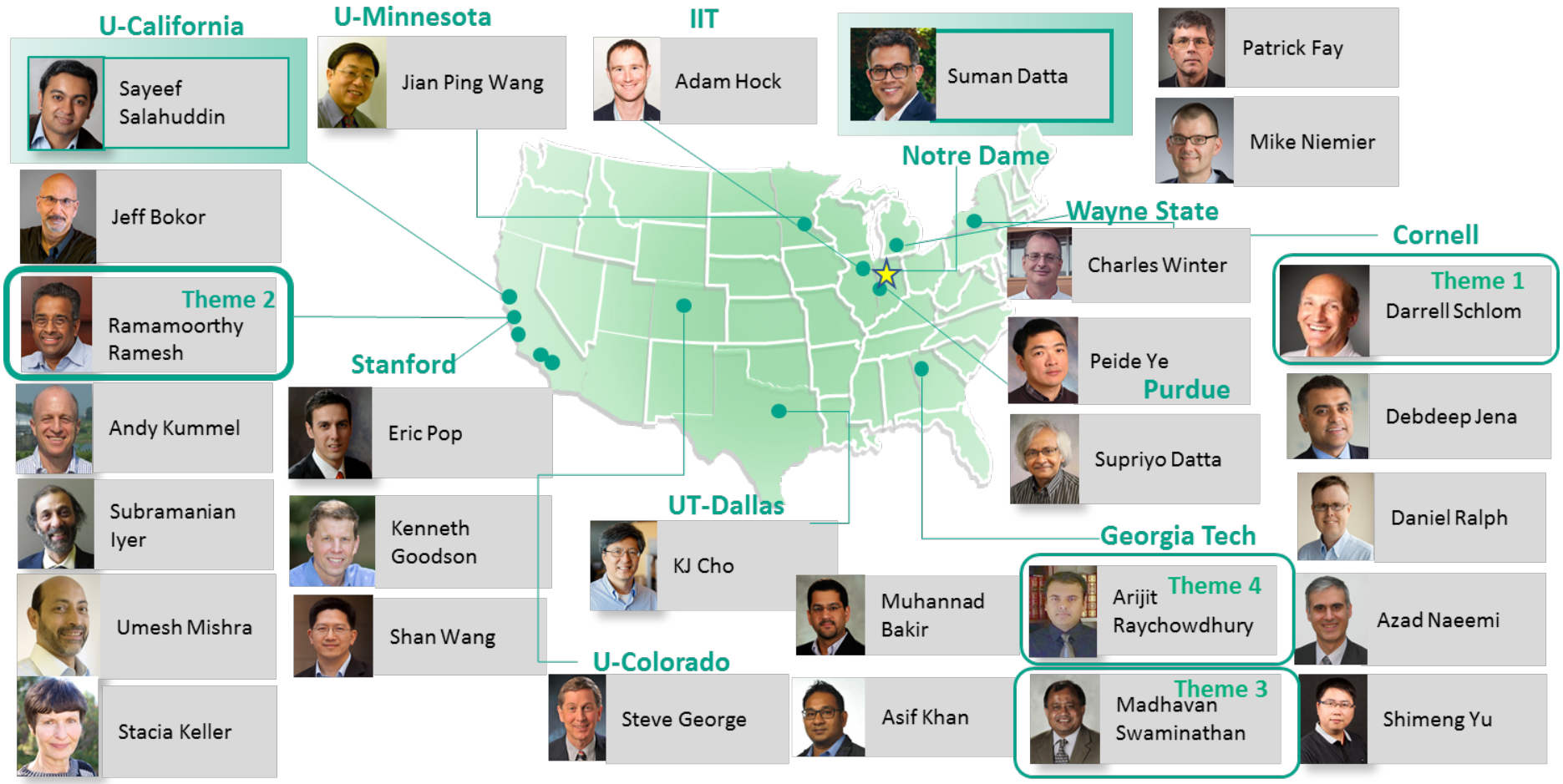

Herding cats or leading All-Star Team

ASCENT: *Applications & System Driven Center on Energy – Efficient Integrated Nanotechnologies*

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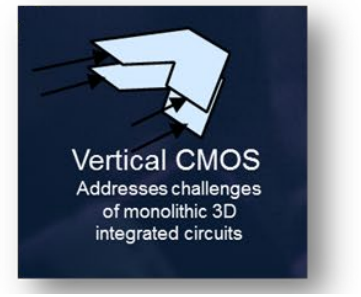

Go vertical

- *BEOL FETs*
- *Barrier less Vias*
- *Selectors for 3D memories*
- *Fine-grained thermal*
- *FEOL FETs (NC)*

Augment charge with spin

- *SOT MRAM*
- *VCMA MRAM*
- *Magneto-electric*
- *Probabilistic spin devices*

Embrace heterogeneity

- *Millimeter-wave packaging*
- *Chip to chip signaling*
- *Power delivery*
- *Reconfigurable RF*
- *Package-level Thermal*

Compute with memory

- Analog weight cells
- Stochastic compute
- Collective compute
- Secure compute

Design, build and benchmark semiconductor materials, devices, packages and compute fabrics to establish semiconductor technology roadmap for our commercial & defense partners

One of 6 centers in JUMP program (sponsored by SRC and DARPA)

Monolithic 3D Research Vectors

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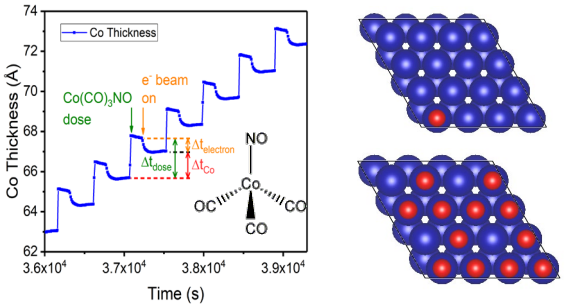
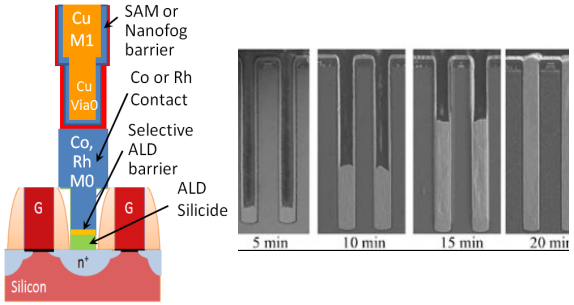
Electron Enhanced ALD



- EE-ALD of Cobalt
- Computational growth study

George, Hunter (Colorado, Wayne St)

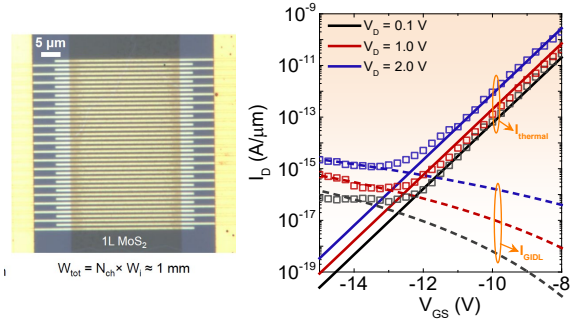
Self-aligned Contacts & Vias



- Hyper Selective ALD of silicide
- Hyper-elective Co (and Ru) ALD

Kummel (UCSD)

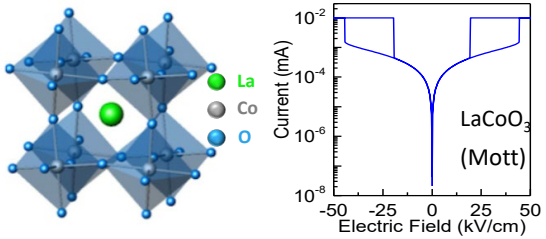
Atto-amp I_{off} FETs



- ML MoS_2 layer on silicon
- 5nm thick In_2O_3 FETs on silicon

Pop, Datta (Stanford, Notre Dame)

3D Memory & Selectors

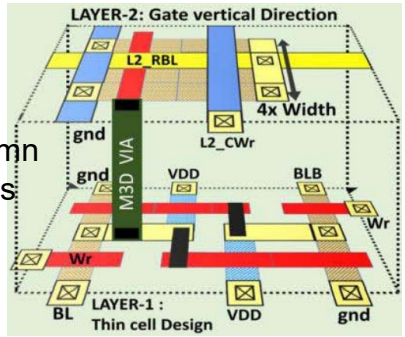


- Selectors for 3D Memory; Mott and Metal Ion Threshold selectors

Schlom, Wong, Datta (Cornell, Notre Dame, Stanford)

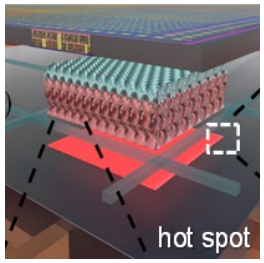
Sequential M3D Design

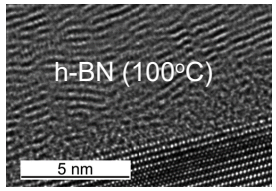
- 3D SRAM with concurrent row & column data access
- 3D DRAM



Datta, Narayanan (Penn St, Notre Dame)

M3D Thermal Management





- Layered materials (hBN) with anisotropic thermal conductivity

Pop, Goodson (Stanford)

Heterogeneous Integration Research Vectors

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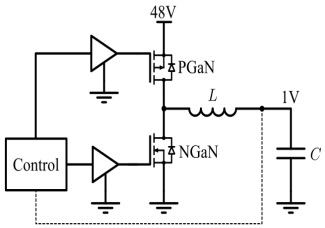
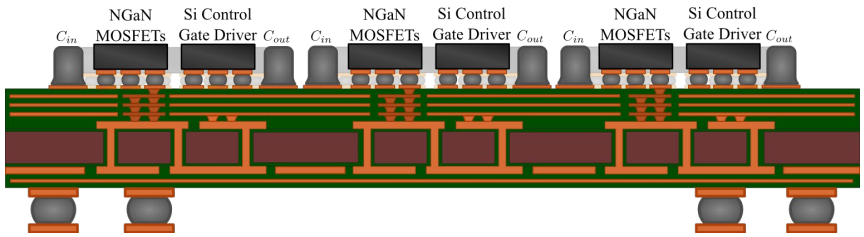
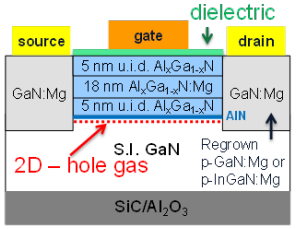
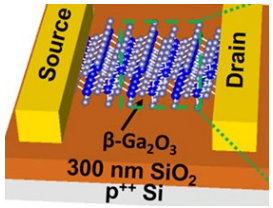
Power Delivery







GaN n/p FET



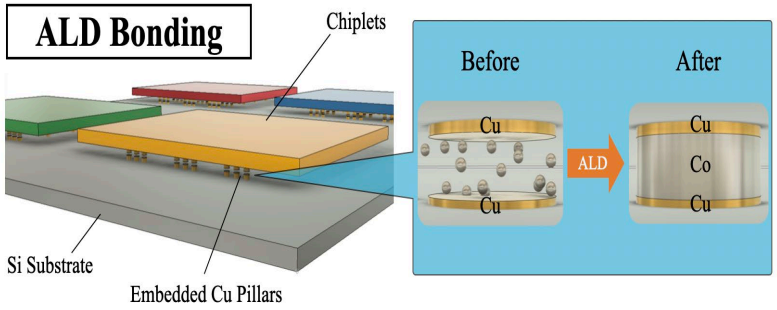
β-Ga_2O_3 nFET

Package integrated 48-to-1V voltage converter & regulator for data centers

Raychowdhury, Misra (Georgia Tech, UCSB)

Ye (Purdue)

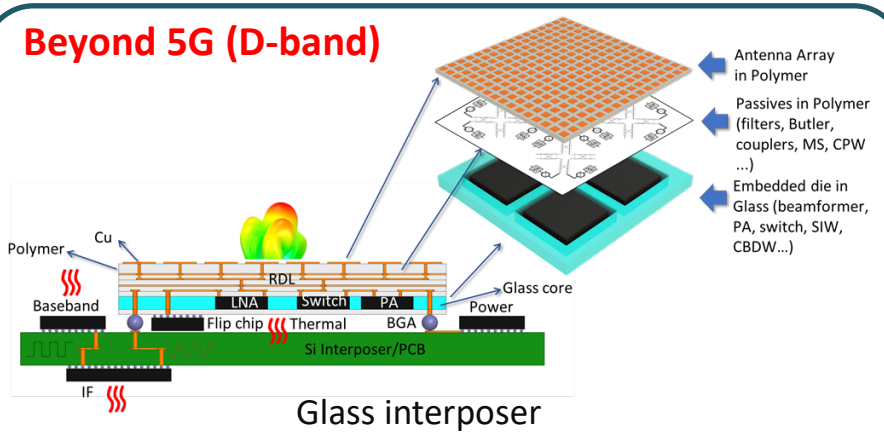
High-speed Digital Signaling (Logic + Memory)



Low temperature (200°C) ALD bonding shows the potential to form nanoscale I/O's

Kummel, Bakir (UCSD, Georgia Tech)

Beyond 5G (D-band)



Glass interposer

RF Switches

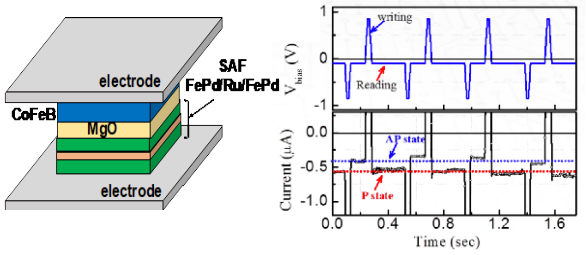
BAW FET Filters

High Gain 3D Antennas + SIW

Datta, Fay, Jena, Swaminathan (Notre Dame, Cornell, Georgia Tech)

Beyond CMOS Research Vector

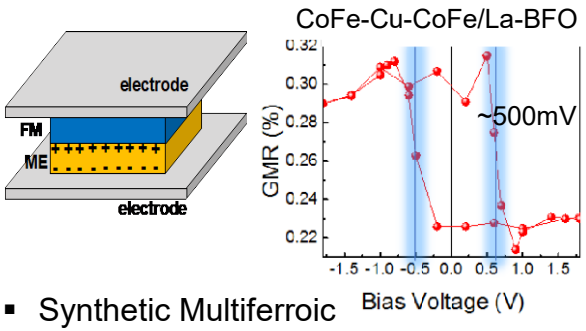
Bi-directional VCMA



- Field-free bidirectional VCMA with SAF
- p-MTJ with J~10^5 A/cm^2 demonstrated

JP Wang (Minnesota)

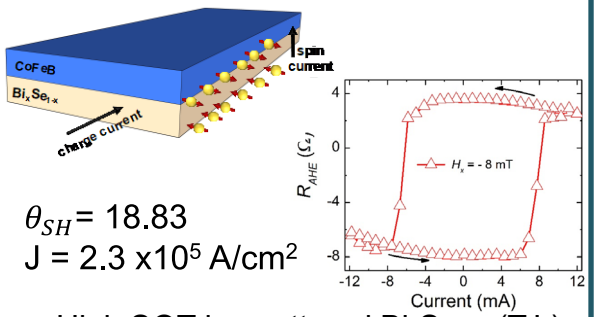
Magneto-electric (ME)



- Synthetic Multiferroic
- Voltage-driven bidirectional switching

Ramesh (Berkeley)

Topological Insulator (TI)

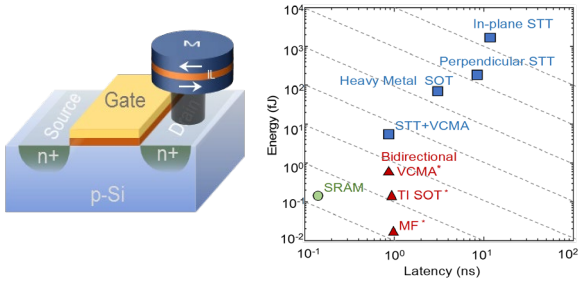


θ_{SH} = 18.83
J = 2.3 x10^5 A/cm^2

- High SOT in sputtered Bi_xSe_{1-x} (T.I.) and Iridate

Wang (Stanford, Minnesota)

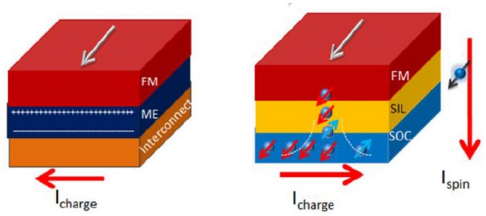
Embedded Memory



- Logic compatible, high endurance, embedded memory applications

JP Wang, Salahuddin (Berkeley)

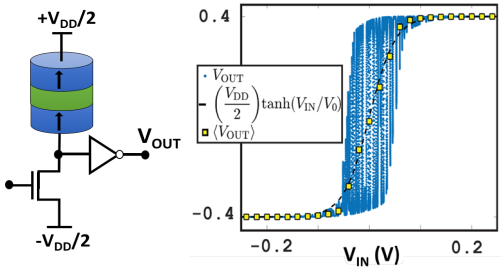
Spin Logic (Majority gate)



- 10aJ class logic operation

Ramesh (Berkeley)

Probabilistic Computing



- p-bits for Deep Belief Network, Ising machines

Salahuddin, Datta (Berkeley, Purdue)

Merged Logic-Memory Research Vector

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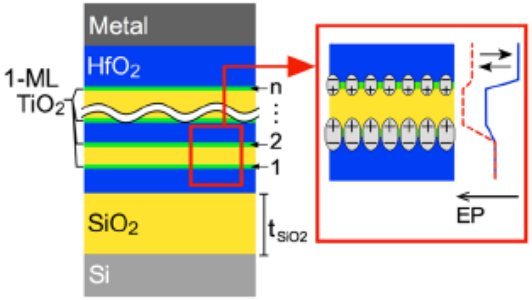
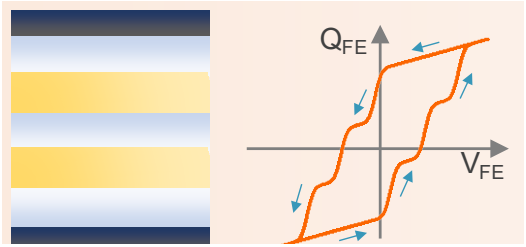
Analog RRAM



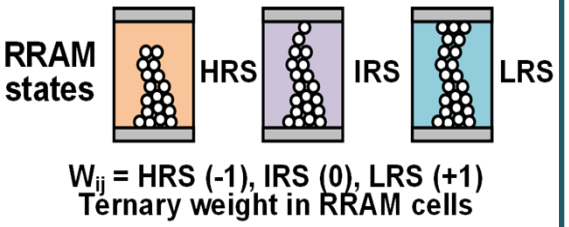
- Interface dipole modulated (IDM)

Analog FeFET



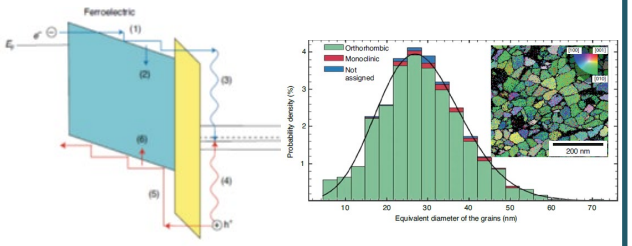
- Partial Polarization switching, polarization rotation, FE Superlattice

RRAM CIM (with C-BRIC)



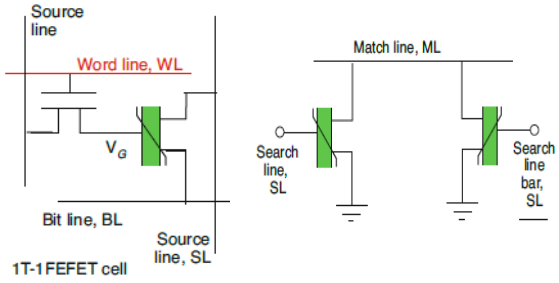
- CIM accelerators with foundry (TSMC) 1T-1R RRAM

FeFET Endurance & Variation



- Understanding fundamental reliability issues in FeFETs

FeFET CIM (with CRISP)



- CIM accelerators (simulation based)

NVMExplorer (with ADA)

- Cross-stack Framework for CIM accelerator design

Lessons Learnt during High-Risk Semiconductor Research

UNIVERSITY OF NOTRE DAME

Serendipity happens but it is not luck. It's being in the right place at the right time with the *right training and mindset*

Scaling is not a Law of Physics. It's hard work by scientists and engineers, our *ingenuity and audacity to compete and thrive*, driven by *free market economics*

Materials scientists, device physicists, circuit designers, system architects & algorithm experts will collaborate to drive semiconductor *innovations that provide application and system level benefit*. A tsunami of investment in semiconductors in the *United States, Europe and Asia* is coming !

"Such an exponential will continue for a very long time"

Family

"Families are the compass that guides us. They are the inspiration to reach great heights, and our comfort when we occasionally falter"