Impact of Not Planned For

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Contributors

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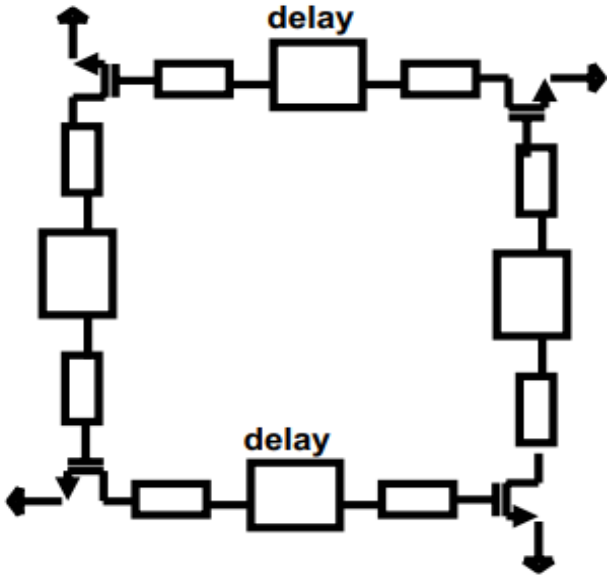
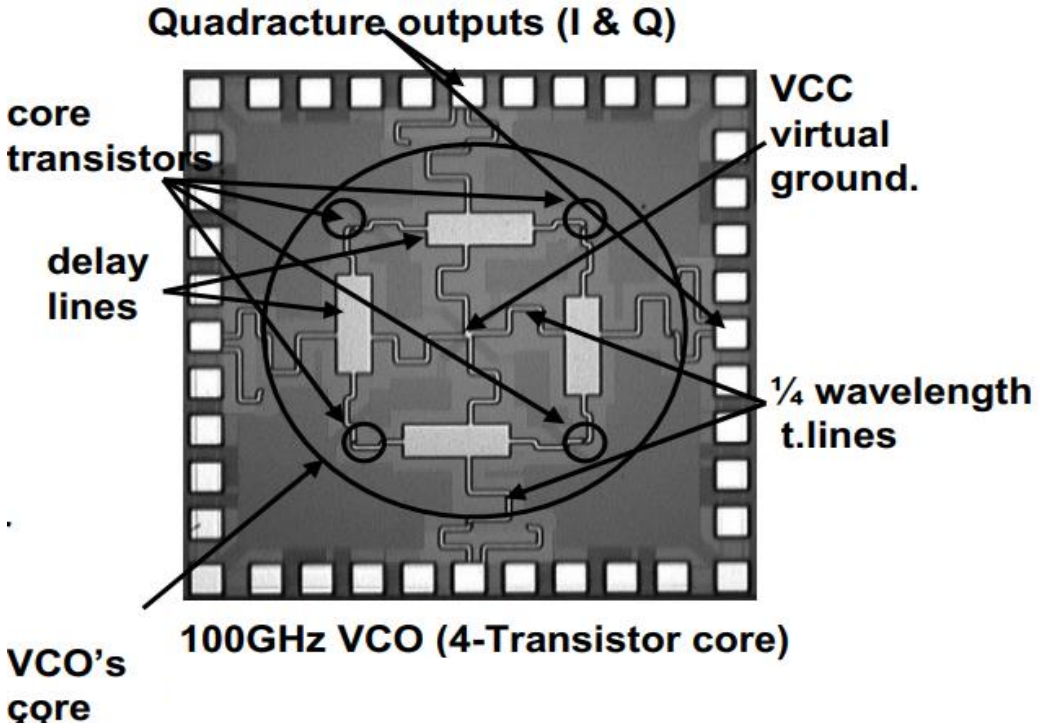
Outline

- Research turned out to be unexpectedly challenging.
- Research turned out to be unexpectedly much easier.
- Conclusion

100-GHz Oscillator in 130-nm CMOS



4-Transistor-core VCO

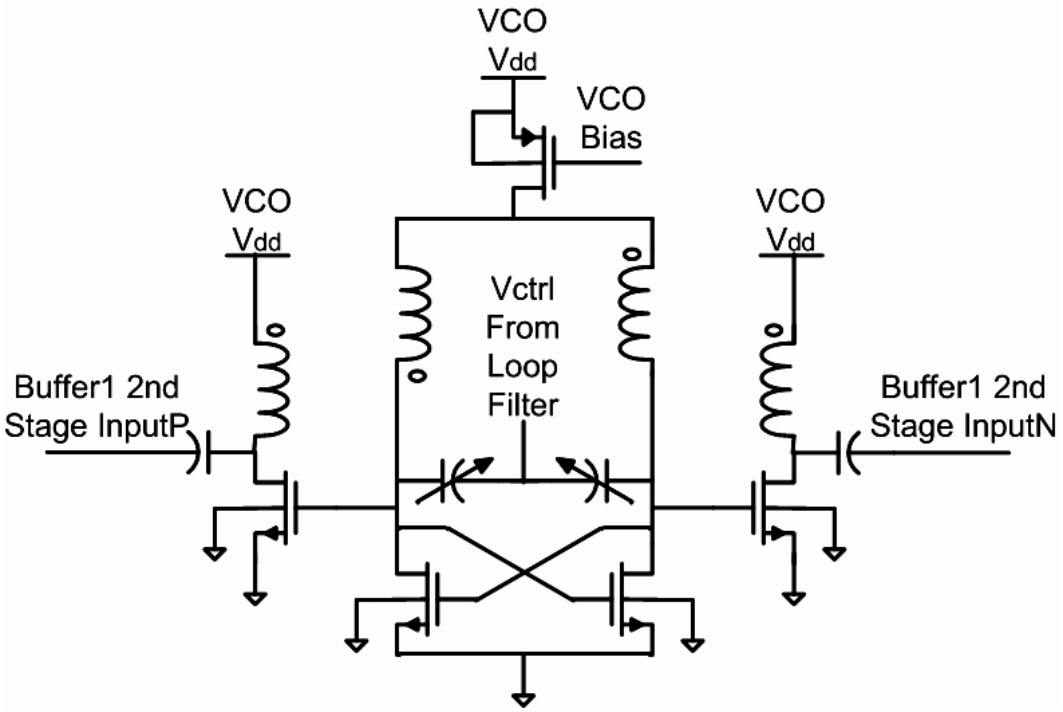


100GHz VCO (4-Transistor core)

State of art in 2004: 100-GHz oscillation in 90-nm bulk CMOS demonstrated. Measured weak output power (-65 dBm or 0.3 nW) while consuming 100-mW DC power.

Luiz M. Franca-Neto, Ralph E. Bishop, Brad A. Bloechel, "64GHz and 100GHz VCOs in 90nm CMOS Using Optimum Pumping Method," Paper 24.6, International Solid-State Circuits Conference, 2004.

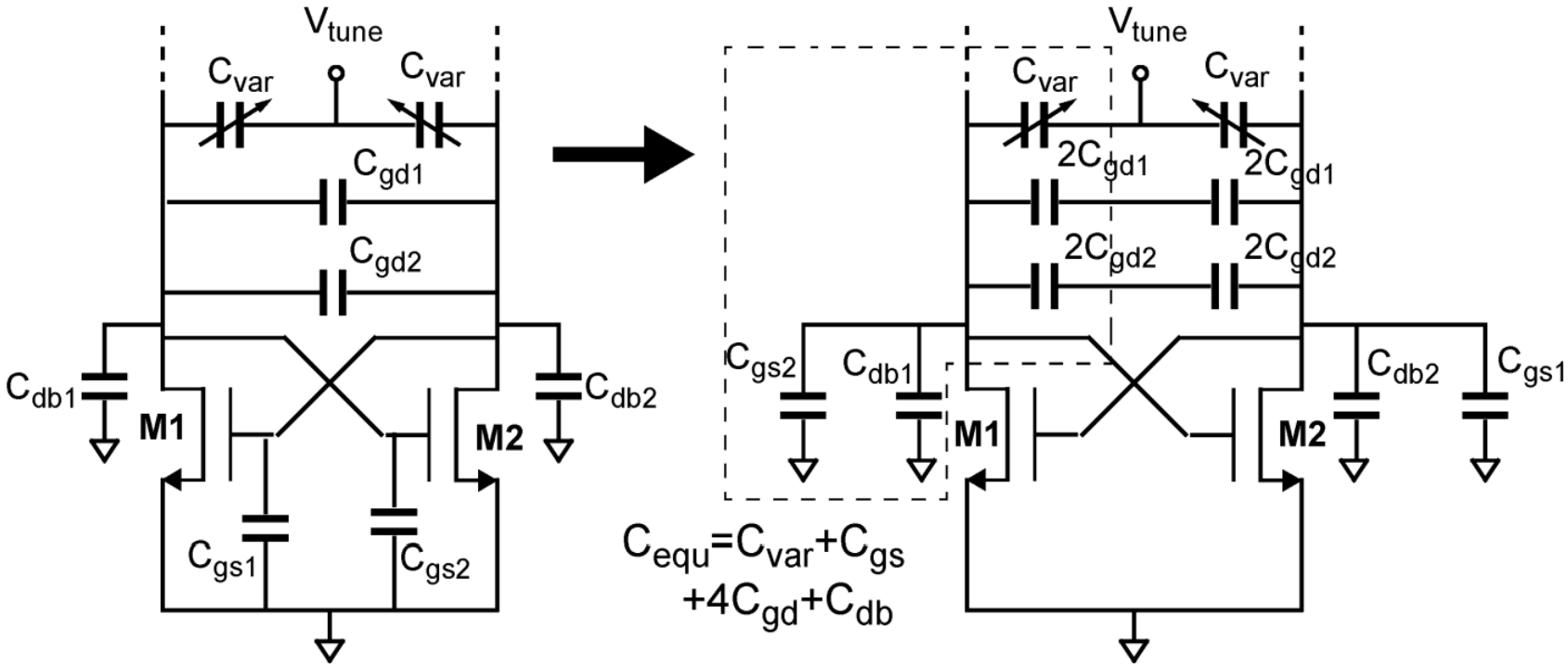
100-GHz Oscillator in 130-nm CMOS



- 1st Attempt: Simulations showed that 100-GHz oscillation possible in 130-nm CMOS: Taped out and measured. No oscillation.

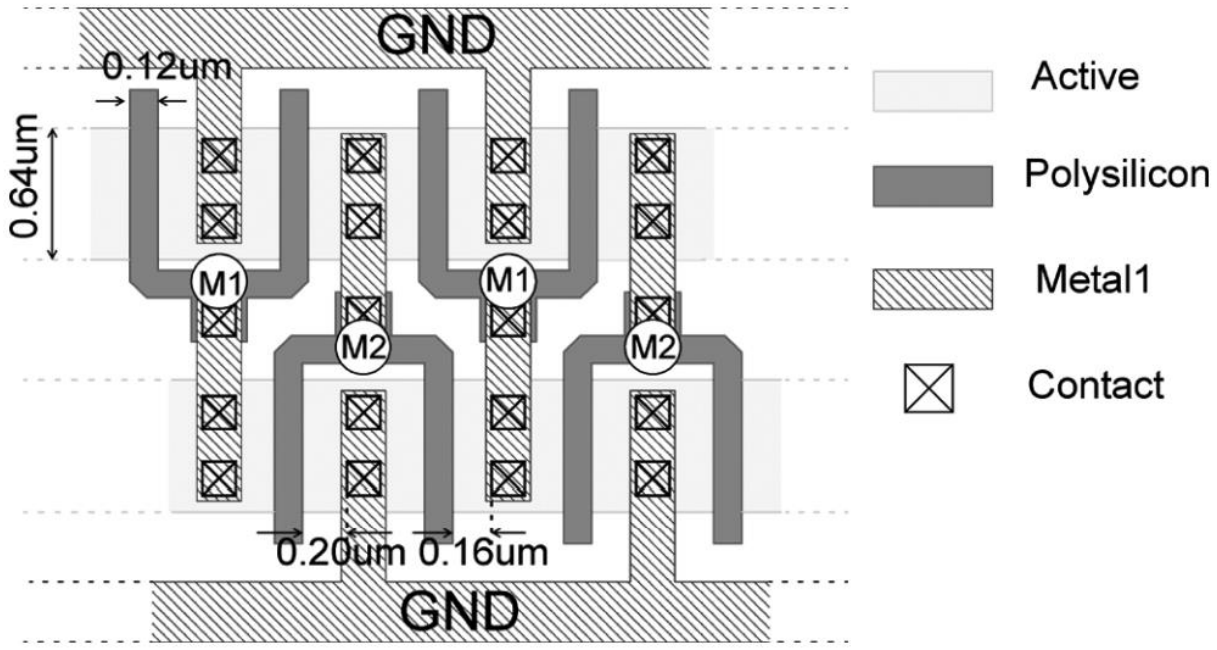
- 2nd Attempt: Must be the transconductance being too low. Widen the core transistors. Taped out and measured. Once again, no oscillation. Models are good up to frequencies less than 10 GHz. Started to use HFSS.

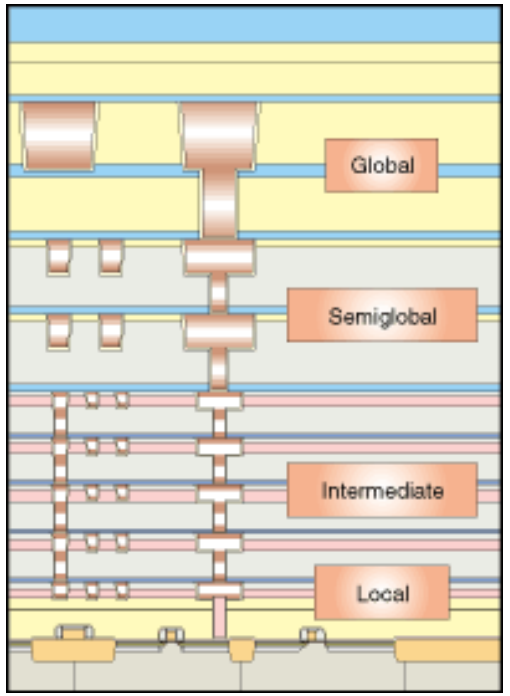
100-GHz Oscillator in 130-nm CMOS



- C_{gd} is more important due to Miller effect.
  $C_{equ}=C_{var}+C_{gs}+C_{db}+4C_{gd}$ $(+C_{ds}+\ldots)$

100-GHz Oscillator in 130-nm CMOS



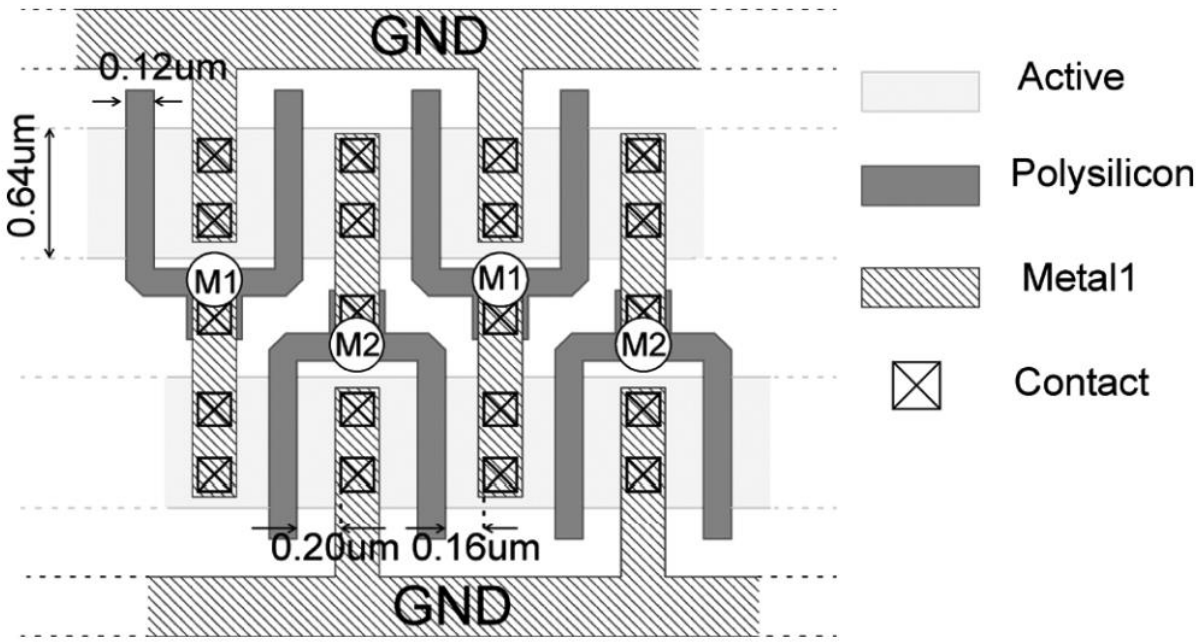


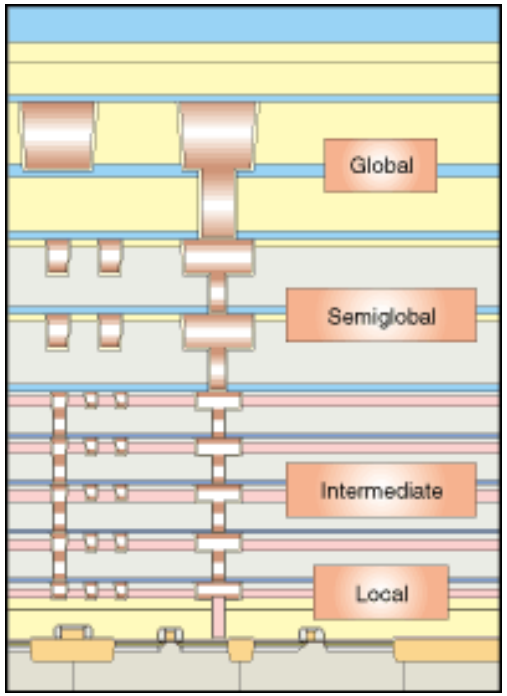
http://www.sony.net/Products/SC-HP/cx_news/vol33/featuring.html

- Layout optimization to lower the capacitance associated with the drain to gate connection.
- Metal 1-6 stack for drain to gate connection for drain and source.
- Later on: Metal 1-2 for source connections and Metal 1-3 stack for drain connections.

$$C_{equ}=C_{var}+C_{gs}+C_{db}+4C_{gd}\ (+C_{ds}+\ldots)$$

100-GHz Oscillator in 130-nm CMOS





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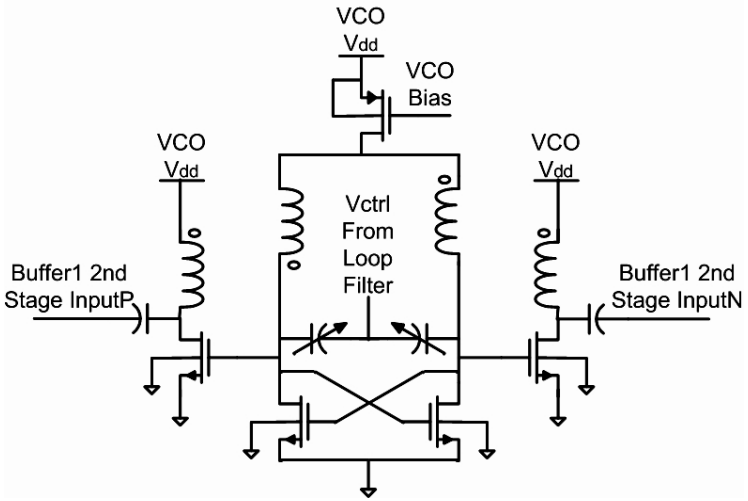
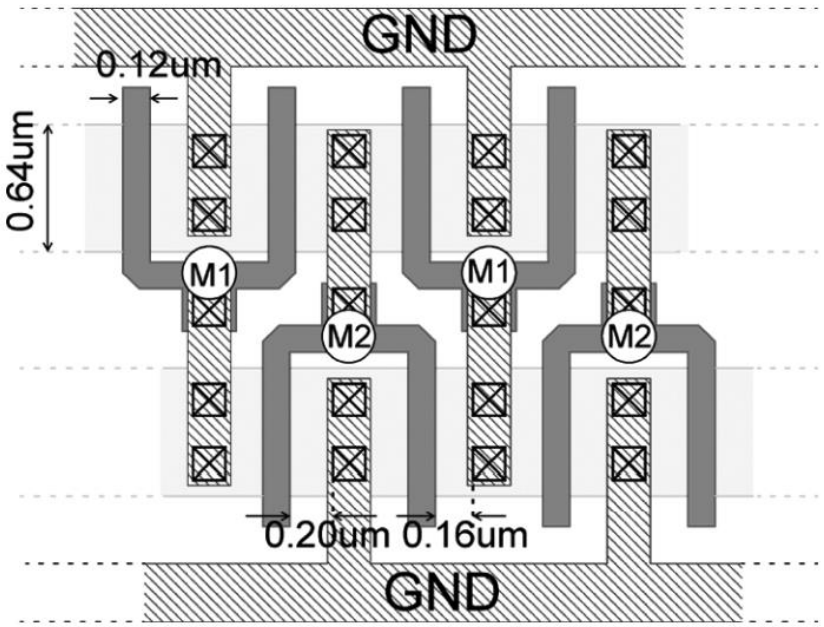
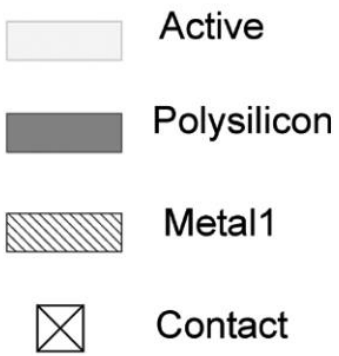
- Increase the spacing between gate poly and drain contact/metal to lower C_{GD} but increases C_{DB}.
- Optimal gate to polysilicon spacing is 0.16 μm.

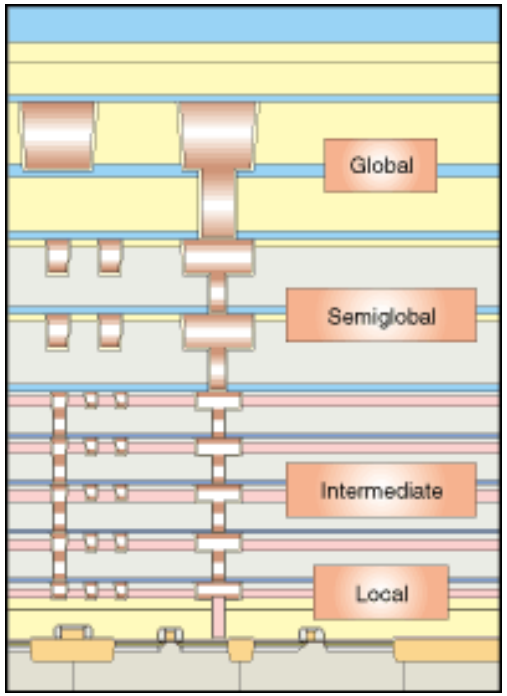


$$C_{equ}=C_{var}+C_{gs}+C_{db}+4C_{gd}\ (+C_{ds}+\ldots)$$

100-GHz Oscillator in 130-nm CMOS







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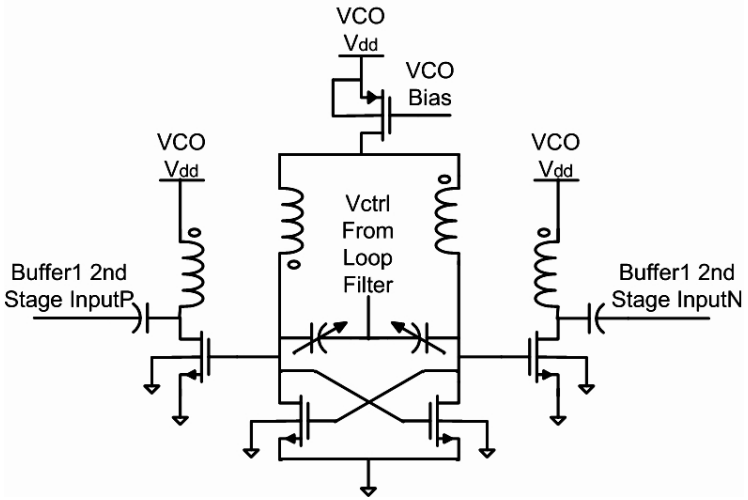
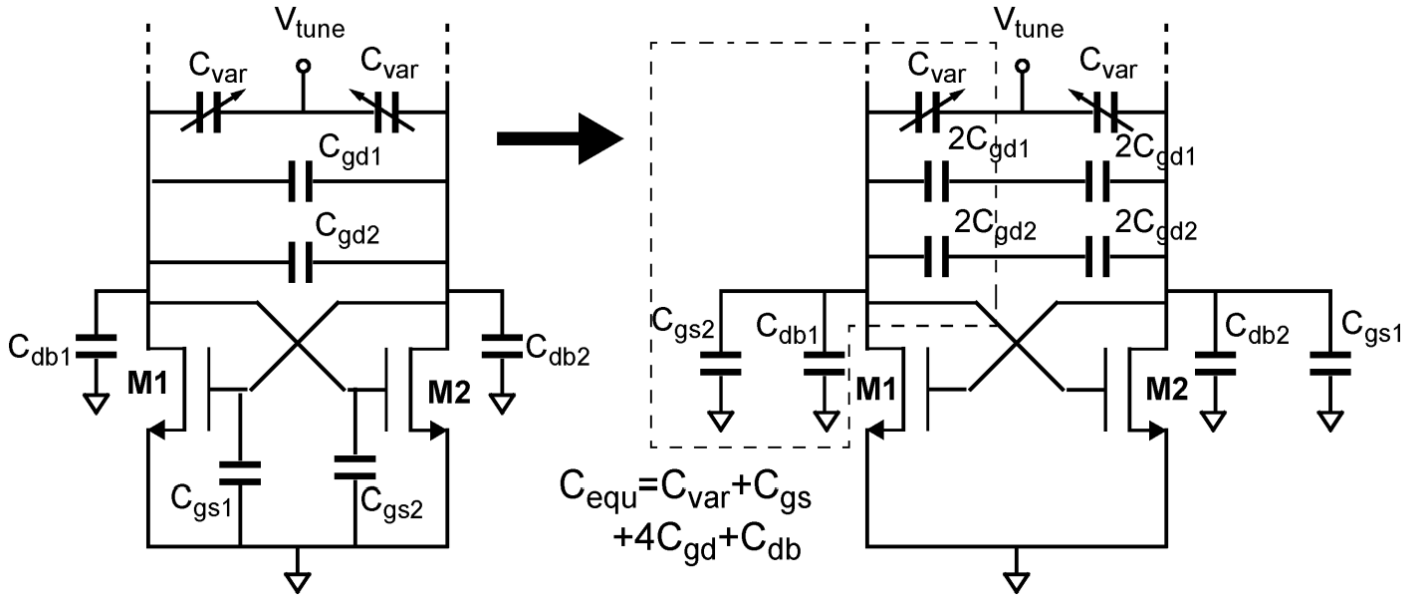
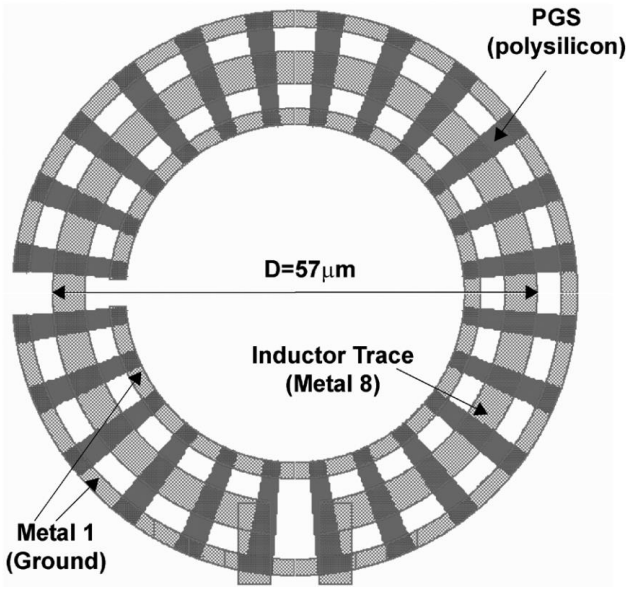


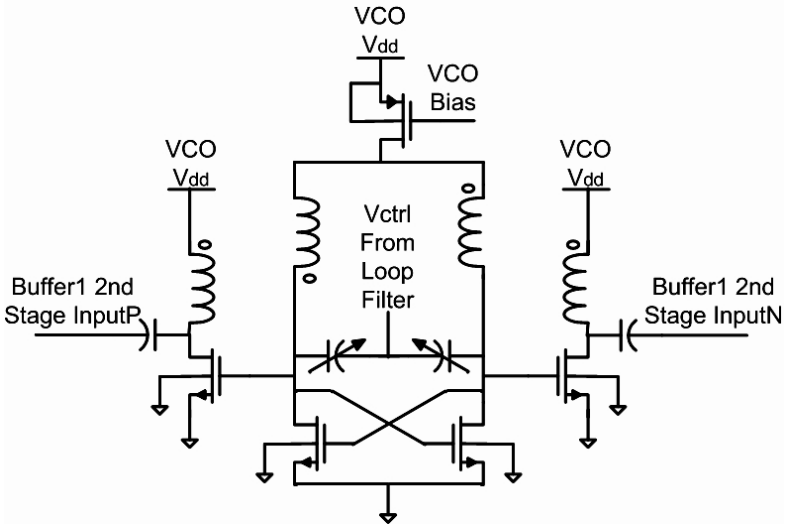
- Increase the spacing between gate poly and source contact/metal to lower C_{GS}. Greater flexibility to increase since C_{SB} is grounded.
- Spacing of 0.20 μm.

$$C_{equ}=C_{var}+C_{gs}+C_{db}+4C_{gd}\ (+C_{ds}+\ldots)$$

100-GHz Oscillator in 130-nm CMOS

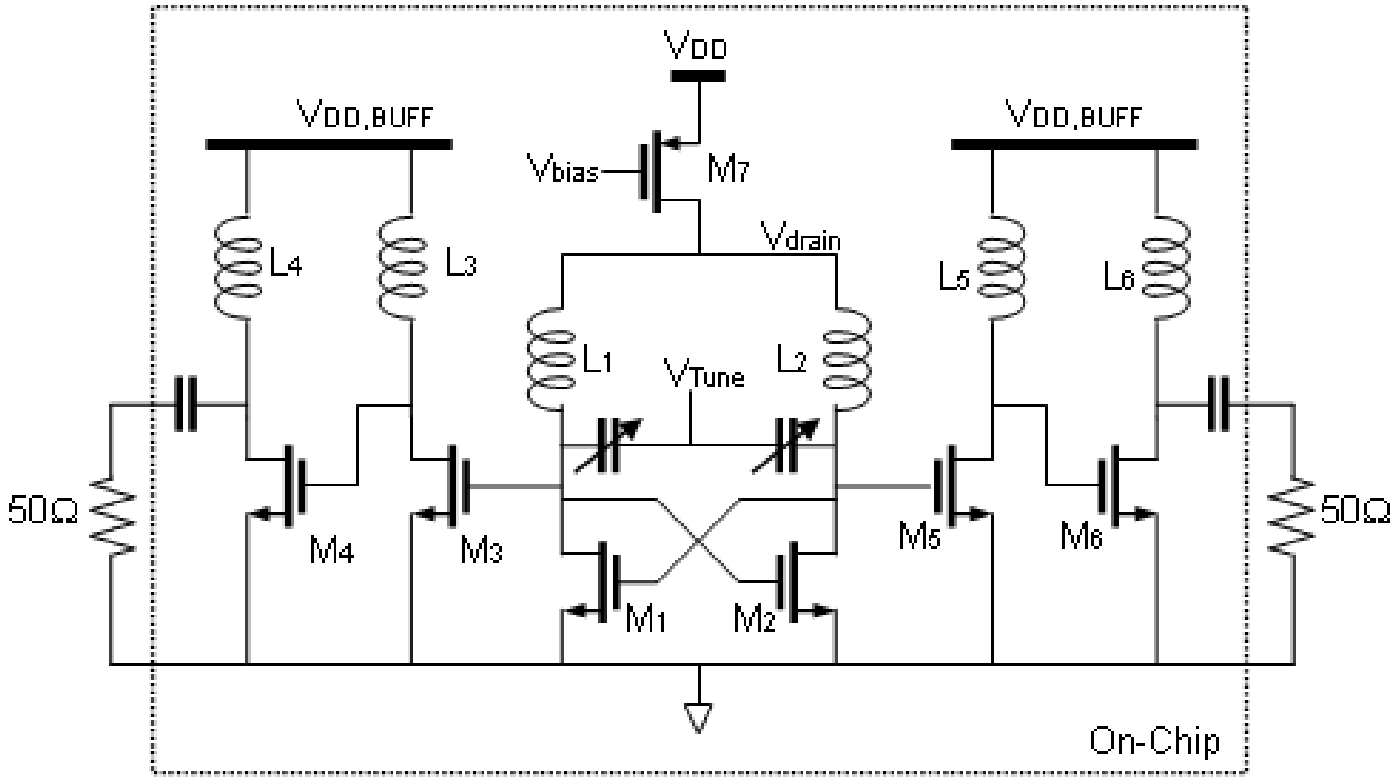






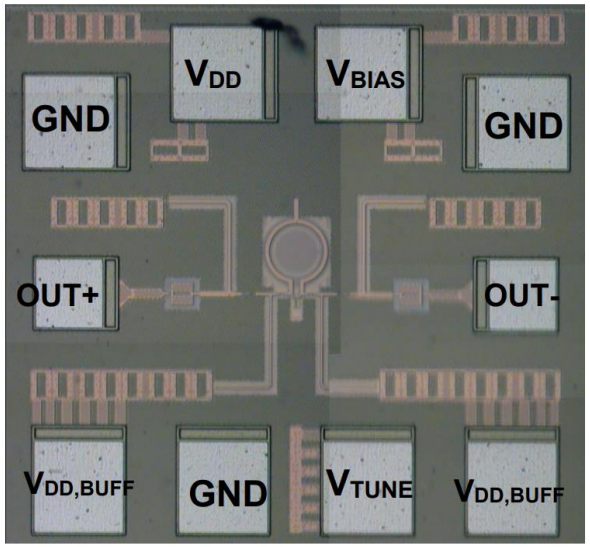
- C_{gd} is more important due to Miller effect. $C_{equ}=C_{var}+C_{gs}+C_{db}+4C_{gd}$ $(+C_{ds}+\ldots)$
- Increase the spacing between ground bars for the ground shield to reduce the parasitic capacitance of the inductor.

100-GHz Oscillator in 130-nm CMOS

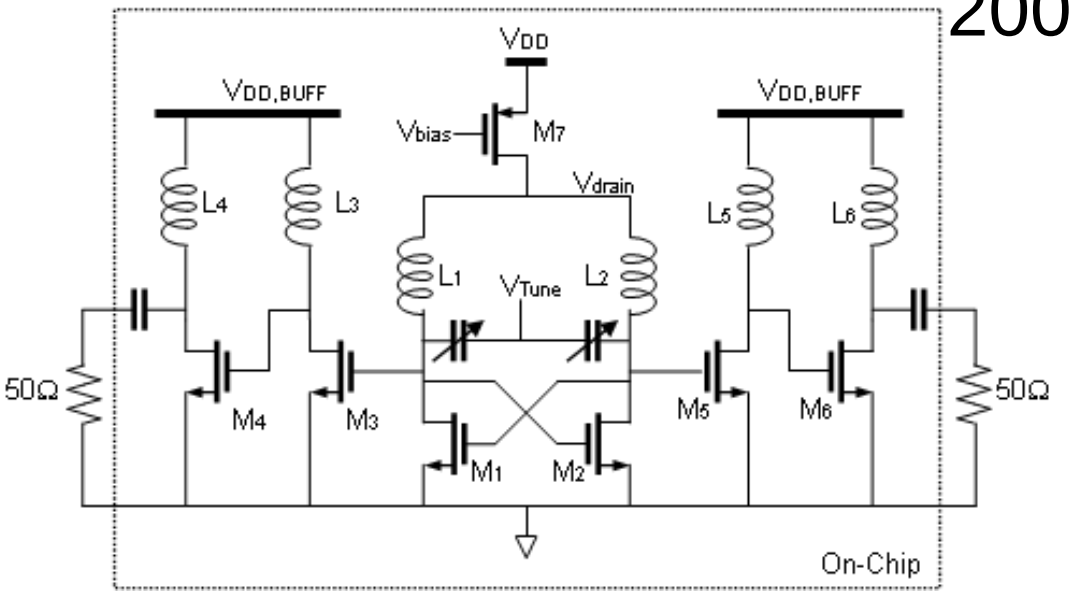


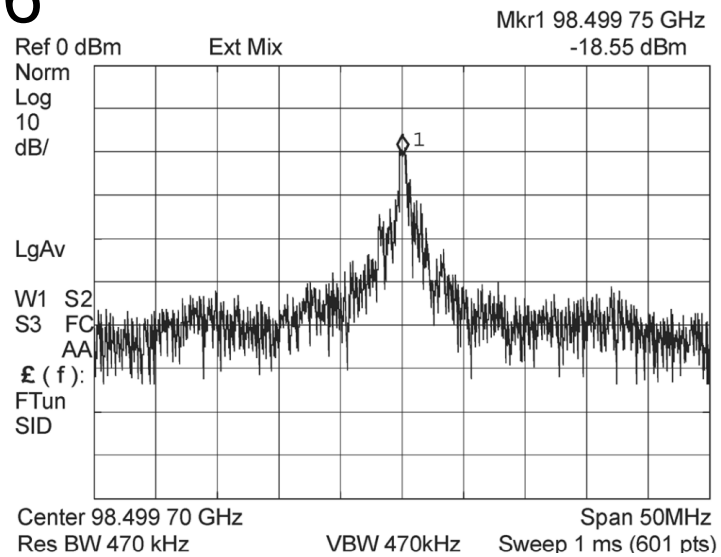
- Tapered buffer/isolation stages in order to reduce the load for the main tank.

100-GHz Oscillator in 130-nm CMOS



2006

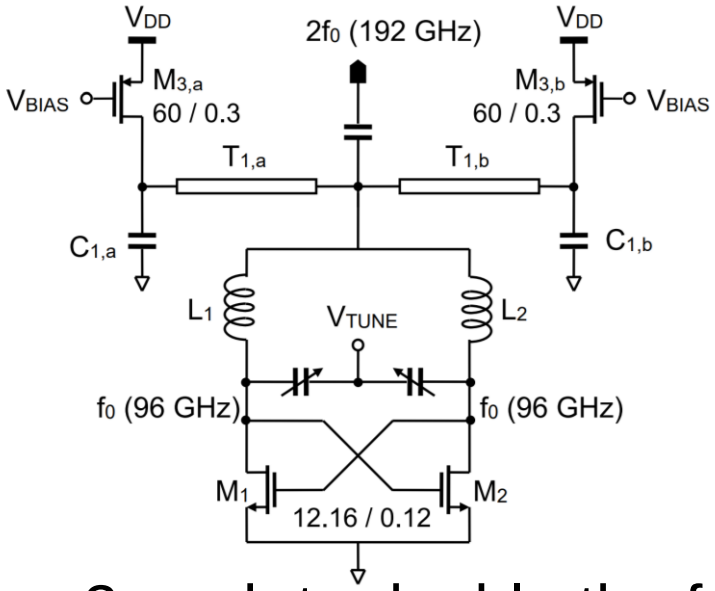


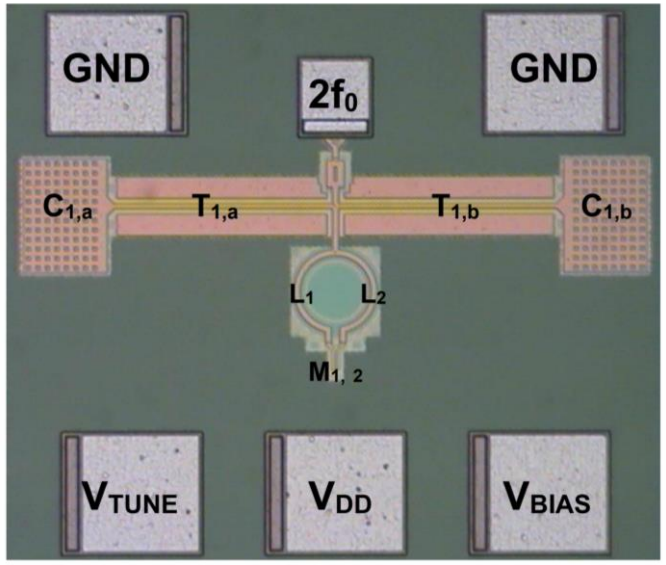


Ref	Frequency (GHz)	Phase Noise (dBc/Hz)	V_{dd} (V)	P_{dc} (mW)	Tuning (GHz)	Technology
This work	59	-89@1MHz	1.5	9.8	5.8	0.13-µm CMOS
	98.5	-102.7@10MHz	1.5	7–15	2.5[a]	
	105.2	-97.5@10MHz	1.2	7.2	0.2	
[2]	50	-100@1MHz	1.3	13	1.0	0.25-µm CMOS
[3]	51	-85@1MHz	1.0	1	1.0[a,b]	0.12-µm CMOS
[4]	40.7	-89@1MHz	1.8	11.3	6.0	0.13-µm SOI CMOS
[5]	103.9	<-94@10MHz	1.5	180	N/A	90-nm CMOS
[9]	60.6	-90@1MHz	1.5	21	8.3[b]	90-nm SOI CMOS

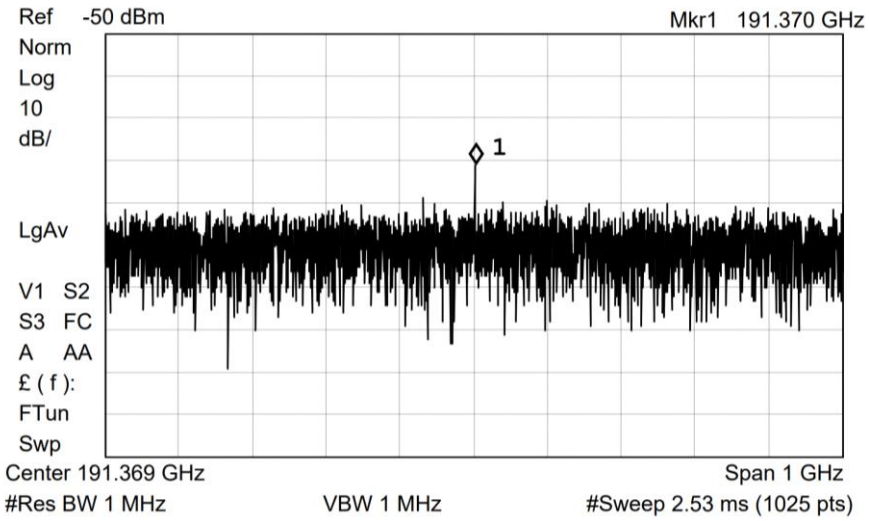
- ~45 dB higher output power at ~6-7X lower DC power consumption using a less advanced technology.
- Can be frequency tuned.
- Identified techniques to increase the transistor size while maintaining the operating frequency.

192-GHz Signal Generation in 130-nm CMOS





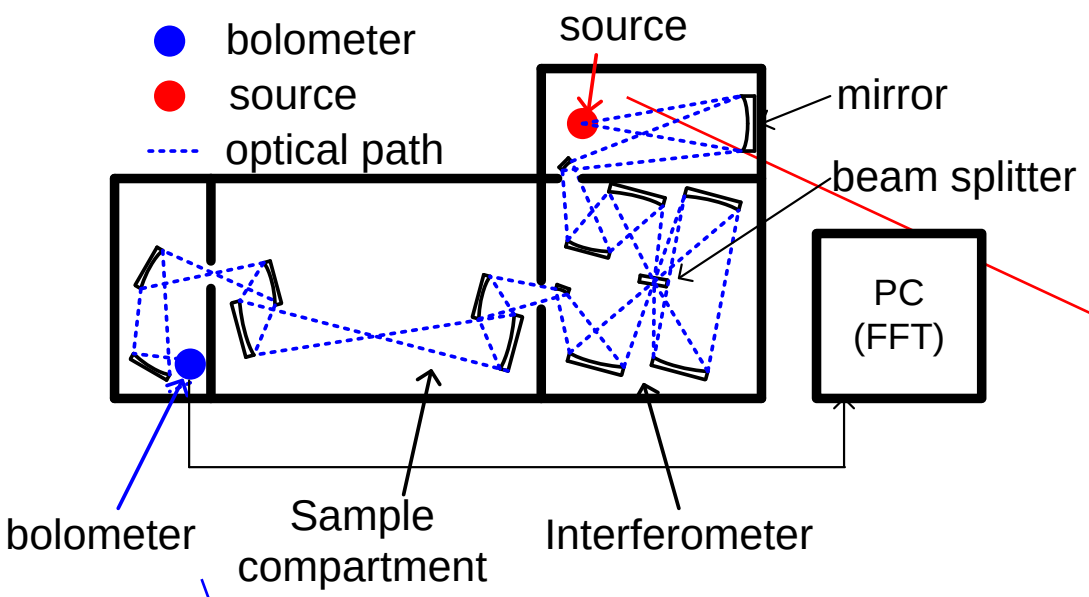
2006



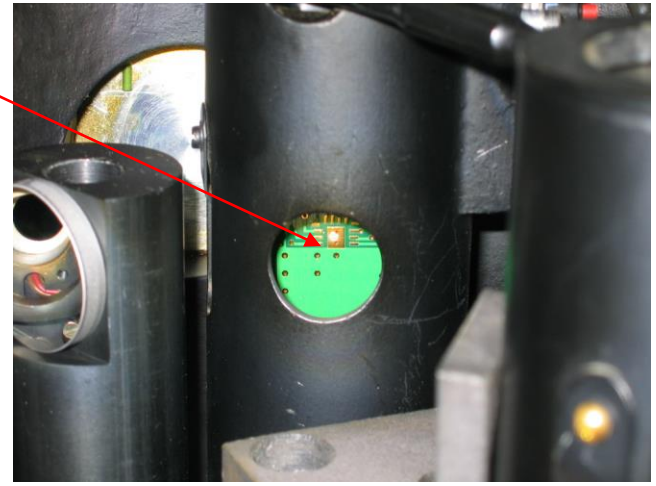
- 2-push to double the frequency.
- Since no buffer required, the core transistors can be increased for higher fundamental output power.

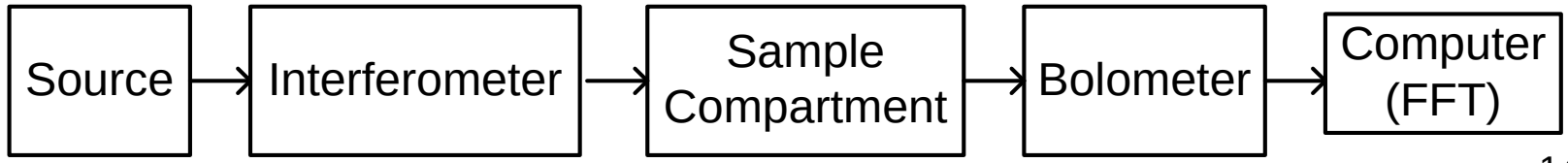
Parameters	
Output Frequencies (GHz)	191.4 – 192.7
Output Power	-20 dBm
DC Power Consumption	17 mW
Phase noise (10 MHz offset)	-106 dBc/Hz at the ~95 GHz

410-GHz Signal Generation in 45-nm CMOS



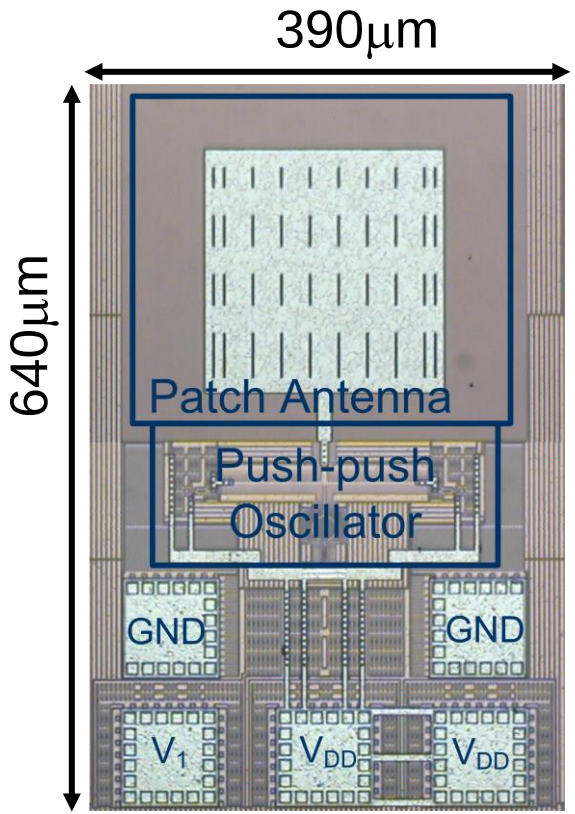
- Fundamental oscillation at 205 GHz.
- 2-Push for frequency doubling.
- How to measure??
- Need an on-chip antenna.

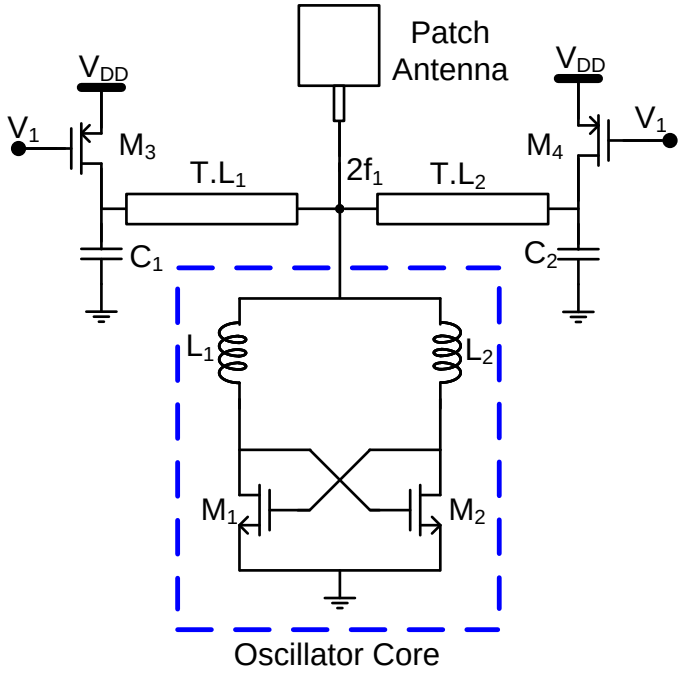


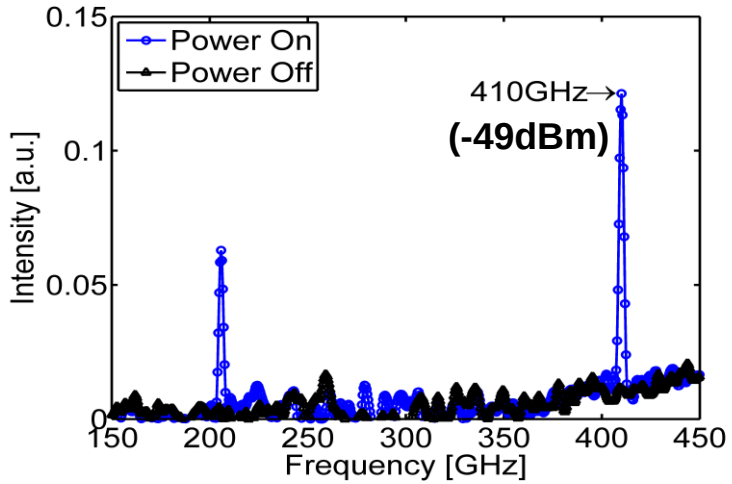


410-GHz Signal Generation in 45-nm CMOS

2008

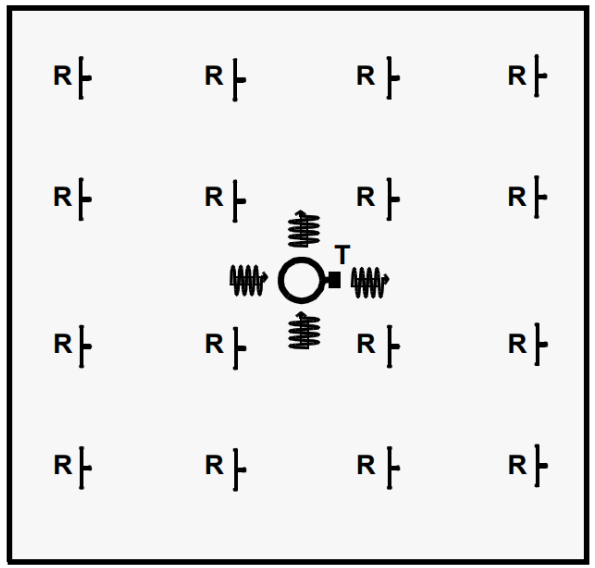




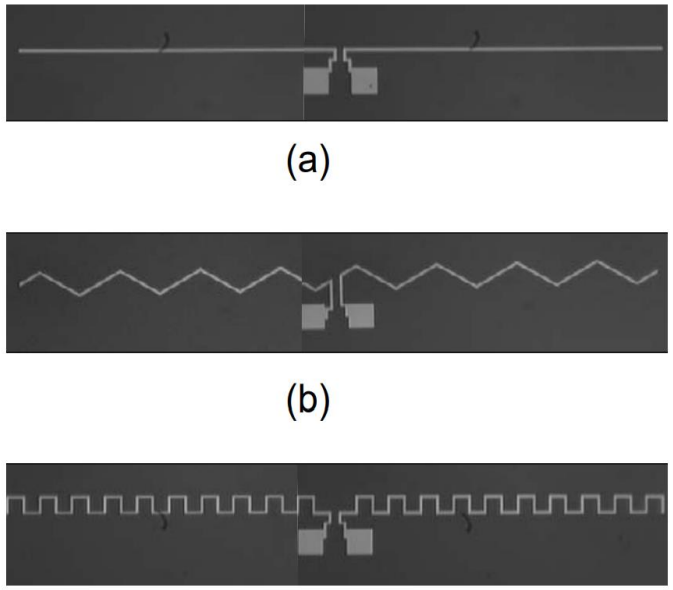


- 1st Tapeout: No bond pad opening.
- 2nd Tapeout: No signal. Model intended for operation at frequencies less than 10 GHz. HFSS is extensively used.
- 3rd Tapeout: Multiple versions with antennas tuned at varying frequencies. (~10 nW of power)
- 4th Tapeout: Optimized the circuit at 390 GHz to achieve 2 μW. (Bigger core transistors and metal oxide metal bypass capacitors)

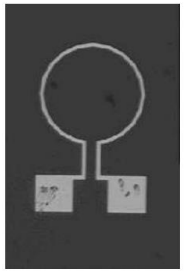
On-chip Wireless Interconnection for Clock Distribution



R=Receiver
T=Transmitter (a)



(a) (b) (c)

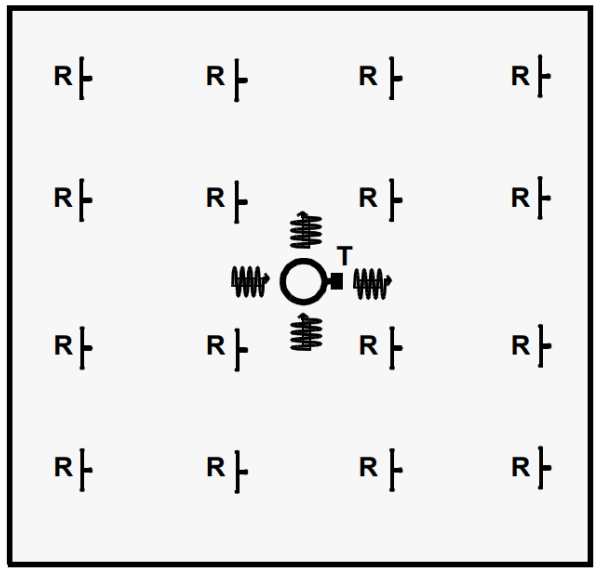


(d)

1996-2004

- Clock frequency was expected to be multi-GHz and skew tolerance tighter.
- Chip size is expected to increase to over 2 cm x 2 cm. Need to match the increasing latency to satisfy the decreasing skew tolerance.
- Power consumption of clock distribution was increasing.
- Reduce the latency by distributing the signal with the speed of light limited delay instead of RC limited delay.
- Investigate if power consumption can be reduced.

On-chip Wireless Interconnection for Clock Distribution



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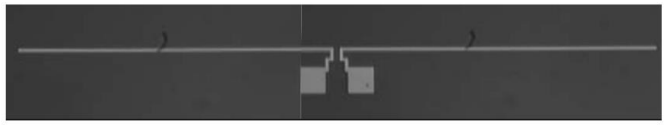
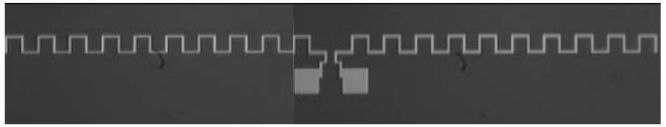
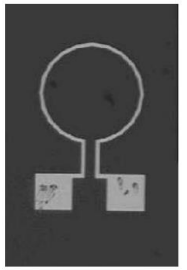


(a)

(b)



(c)



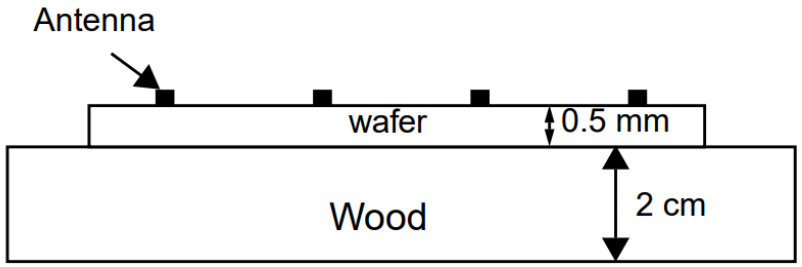
(d)

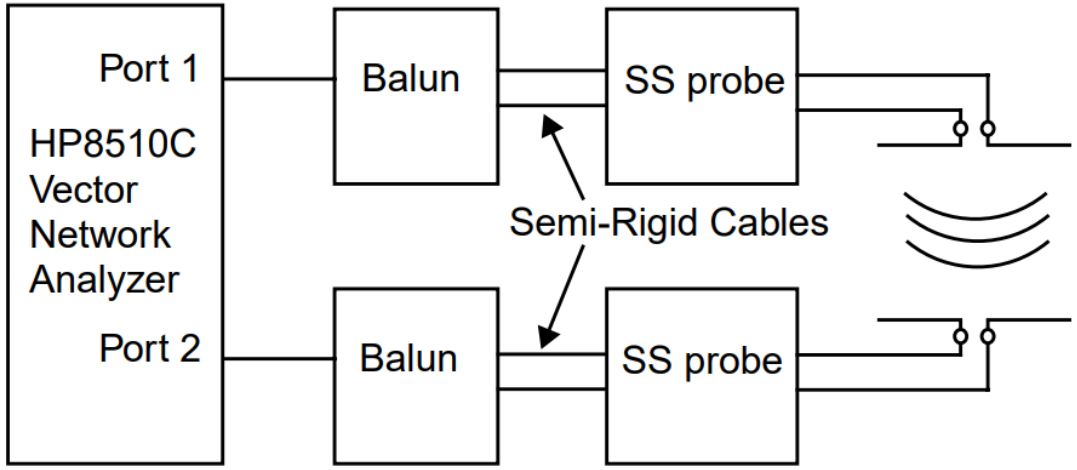
1996-2004

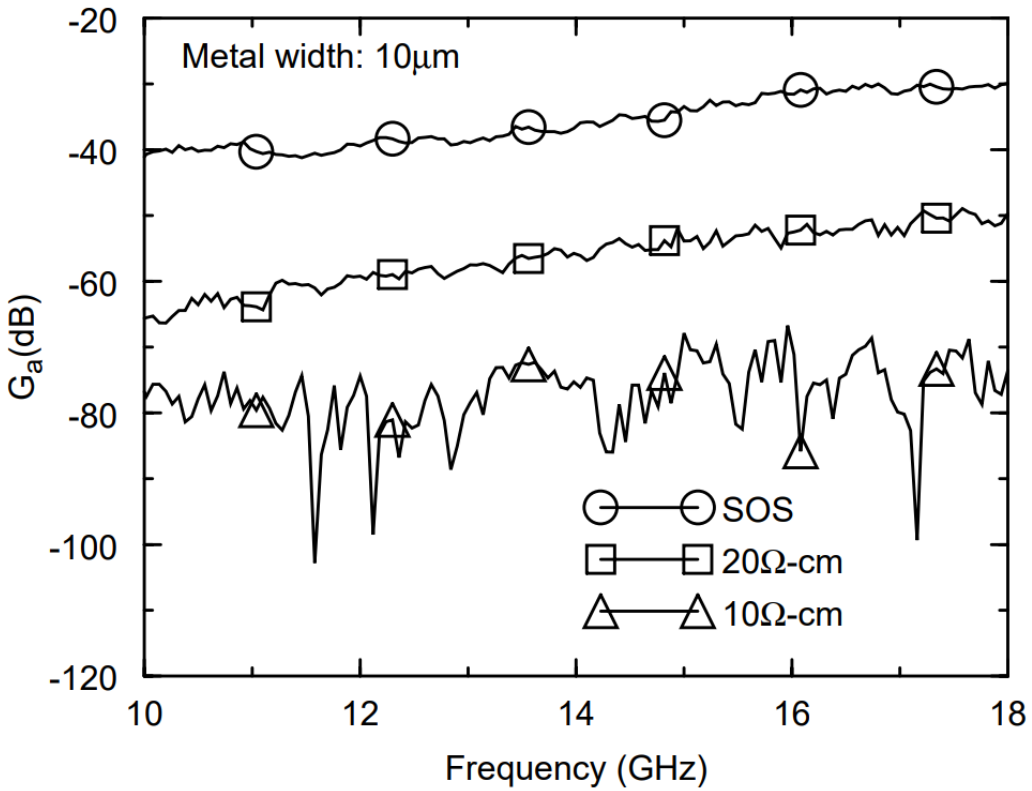
- RFCMOS is struggling to meet the requirements for the 900-MHz cellular applications. Can you build the necessary circuits?
- Can you integrate sufficiently efficient antennas?
- Can you propagate signals within an IC with so many devices and interconnects?
- Can we overcome the interference to the circuits in an IC as well as to the clock by the circuits in an IC?

On-chip Wireless Interconnection for Clock Distribution

2-cm separation
2-mm long zig-zag dipole
200-μm diameter loop
10-μm metal width

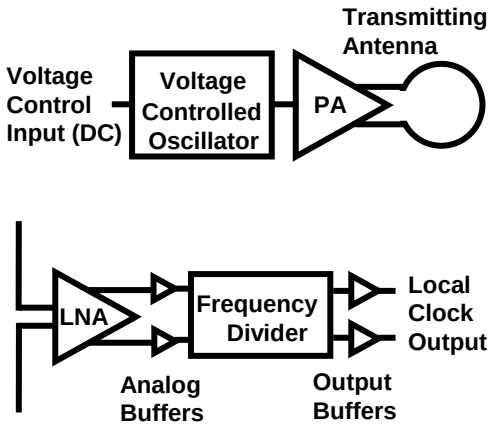


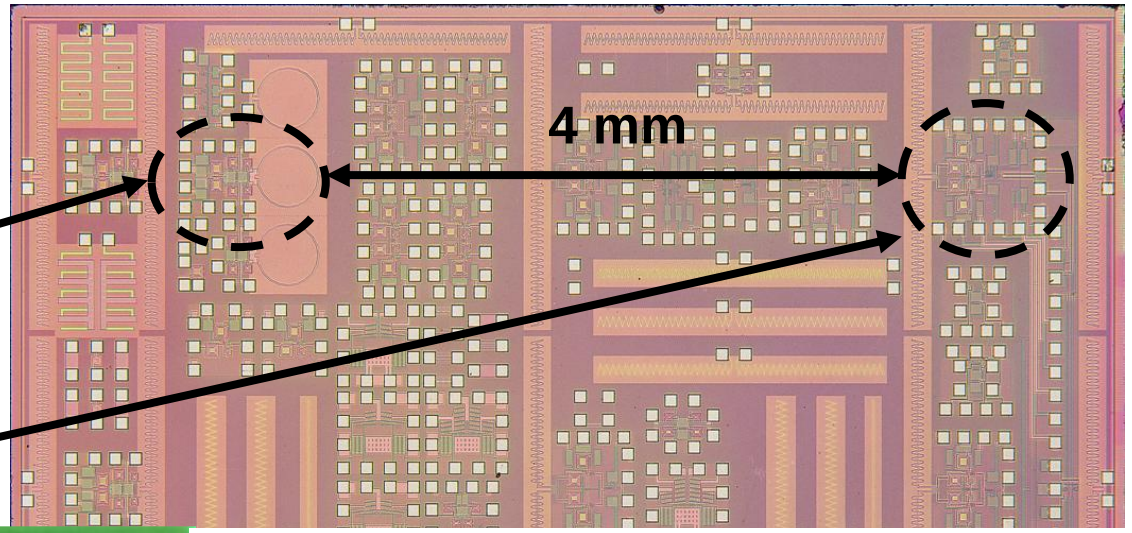


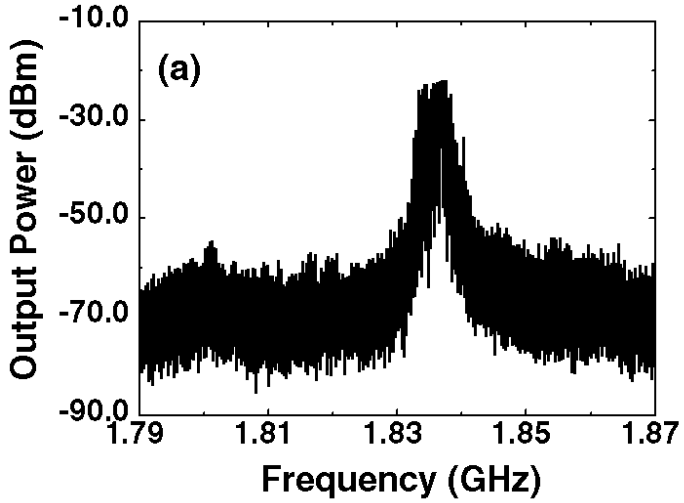


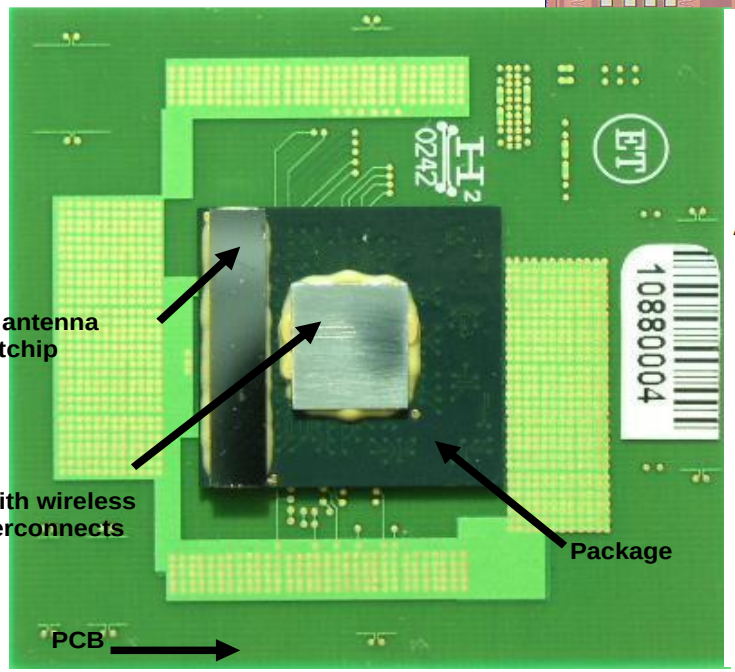
$$G_a = \frac{|S_{21}|^2}{\left(1-|S_{11}|^2\right)\left(1-|S_{22}|^2\right)} = G_t G_r \left(\frac{\lambda}{4\pi R}\right)^2 e^{-2\alpha R}$$

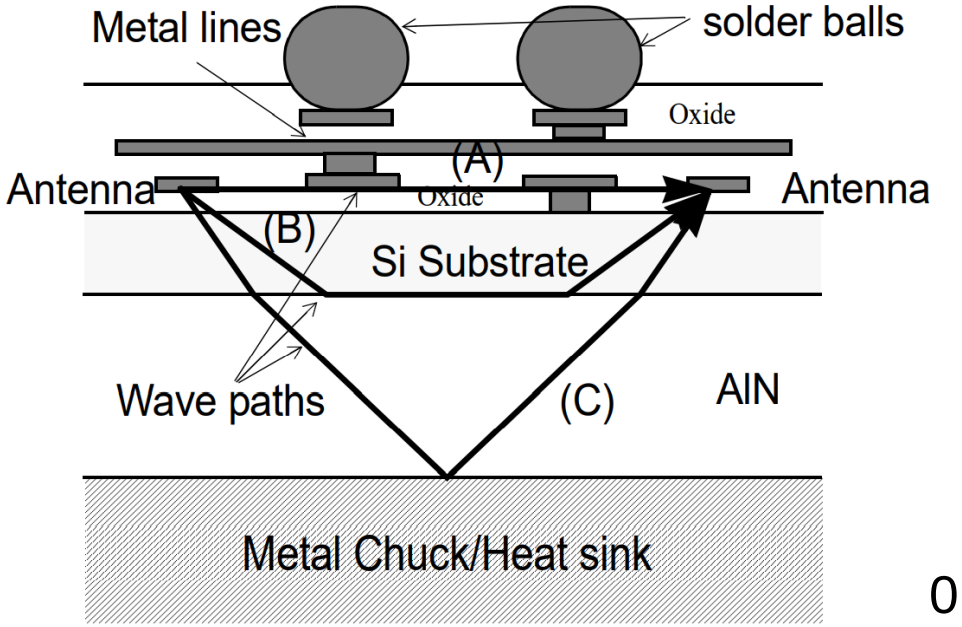
On-chip Wireless Interconnection for Clock Distribution

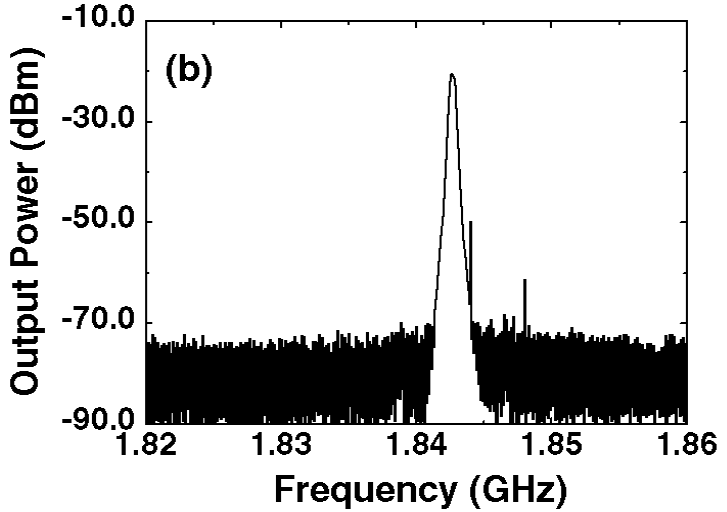






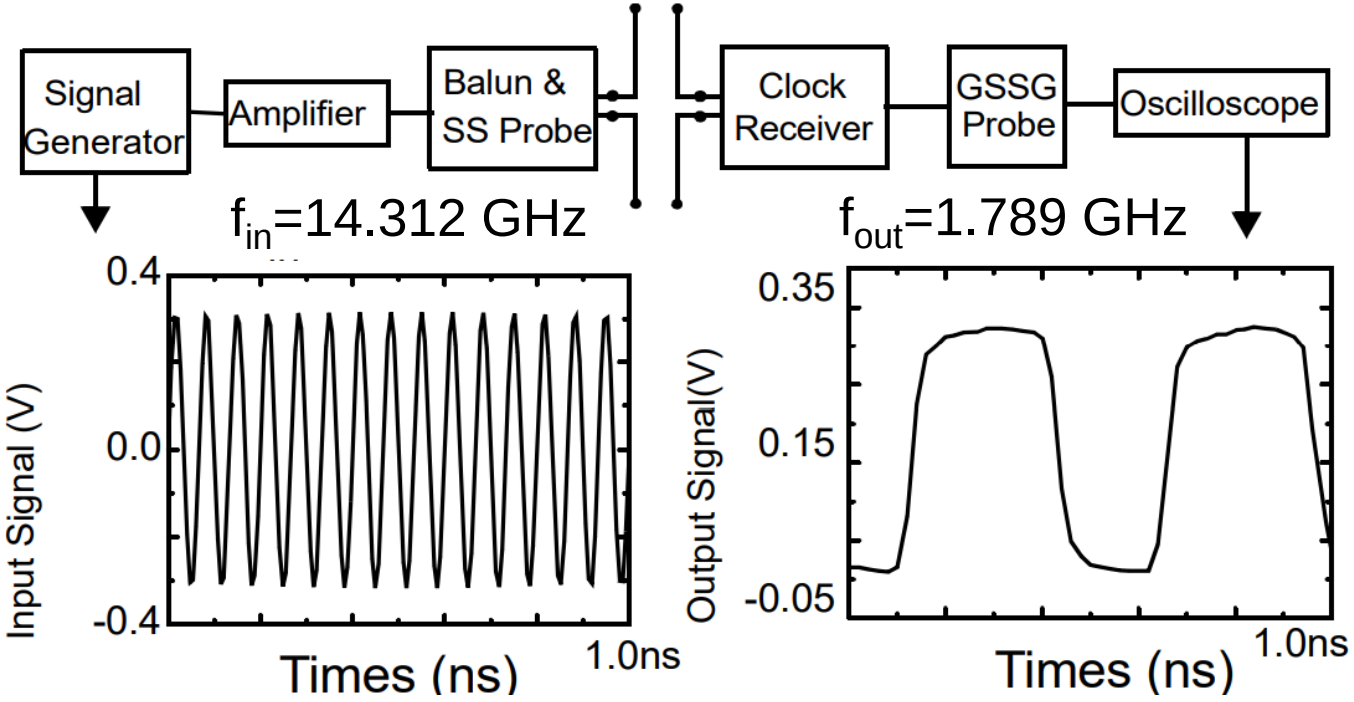


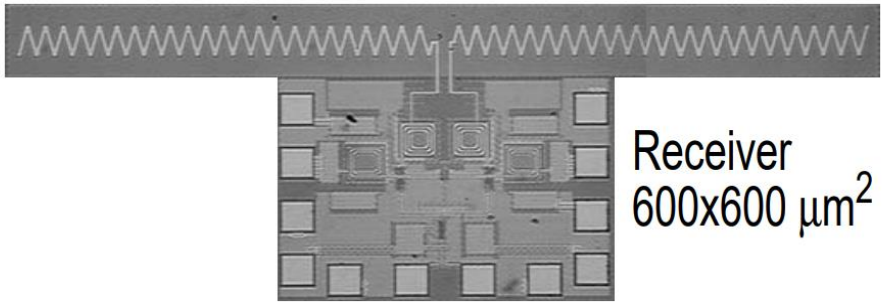


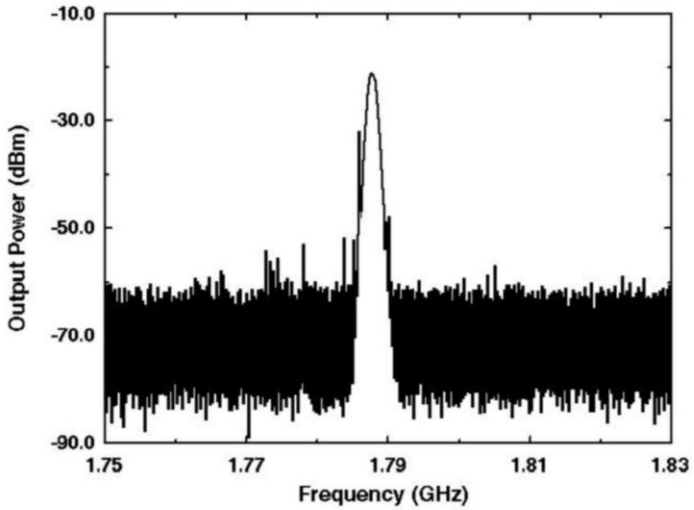


0.180-μm UMC CMOS

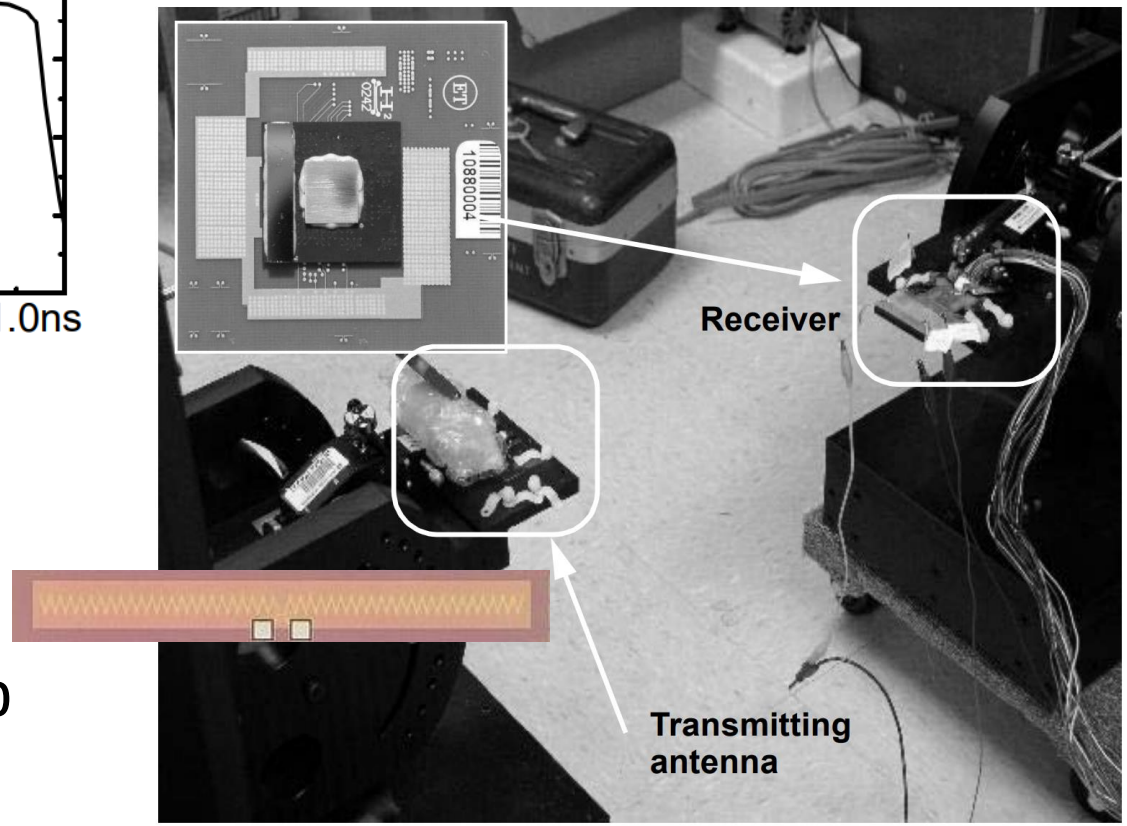
On-chip Wireless Interconnection for Clock Distribution



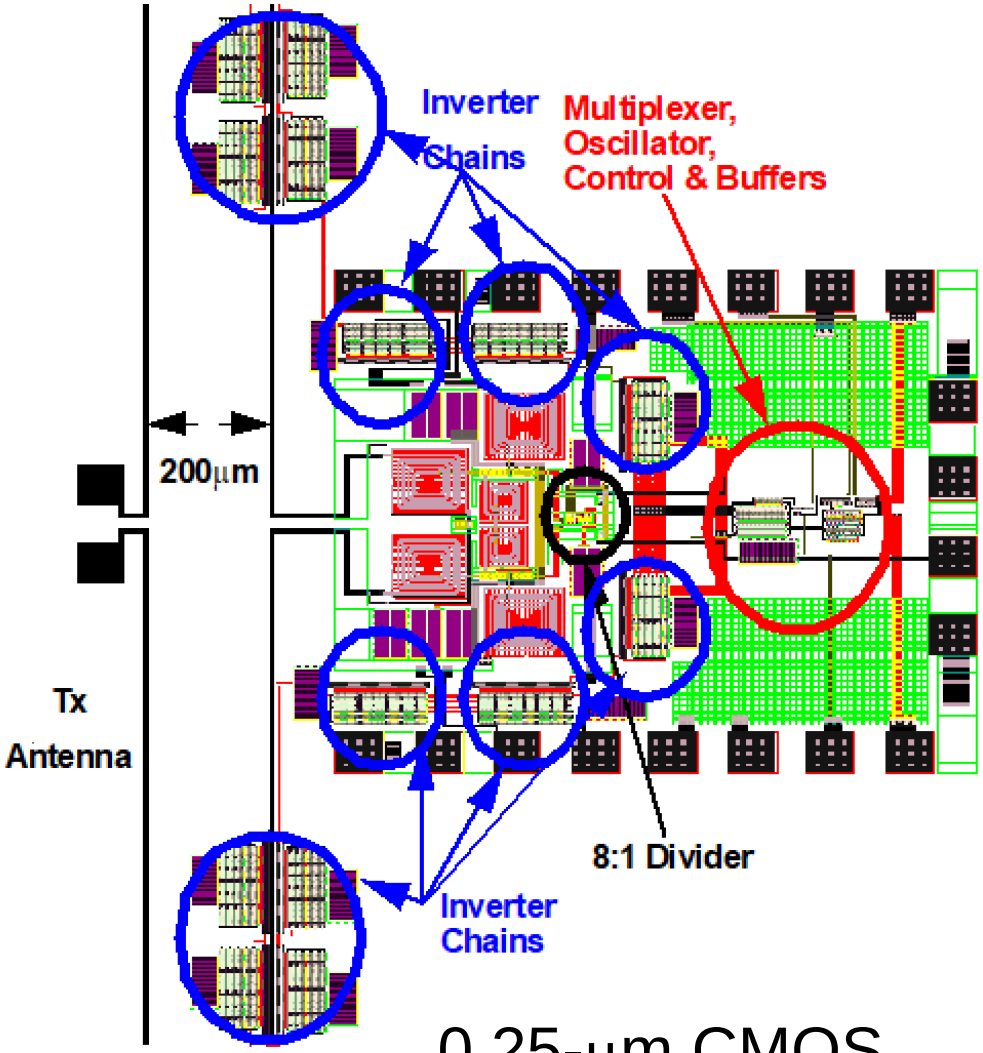




- Communication over free space using CMOS circuits with on-chip antennas.



On-chip Wireless Interconnection for Clock Distribution



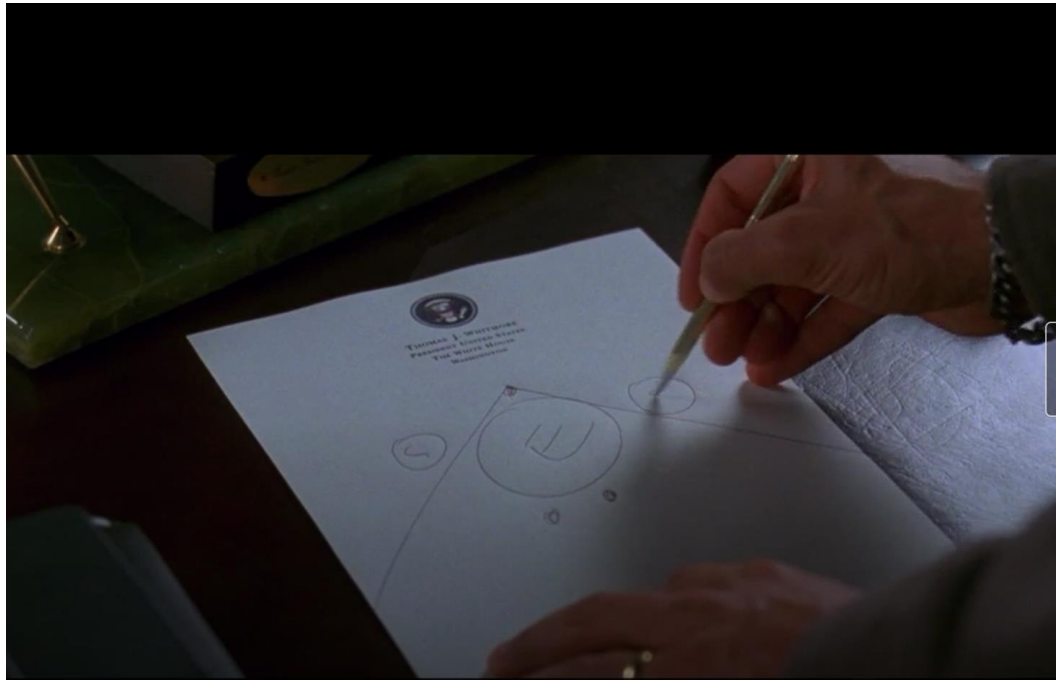
0.25-μm CMOS

Measured clock jitter and SNR

Input to Noise Generators		VCO	Received Clock	
Transmit Power to Antenna		15 dBm	15 dBm	17.5 dBm
Noise Condition	Quiet	0.57% 26.4 dB	0.57% 26.4 dB	0.41% 29.3 dB
	A	0.91% 22.4 dB	0.98% 21.7 dB	0.59% 26.1 dB
	B	1.05% 21.1 dB	0.96% 21.9 dB	0.76% 23.9 dB
	C	1.37% 18.8 dB	3.20% 11.4 dB	1.83% 16.3 dB
	D	2.72% 12.8 dB	no lock (N/A)	3.63% 10.3 dB

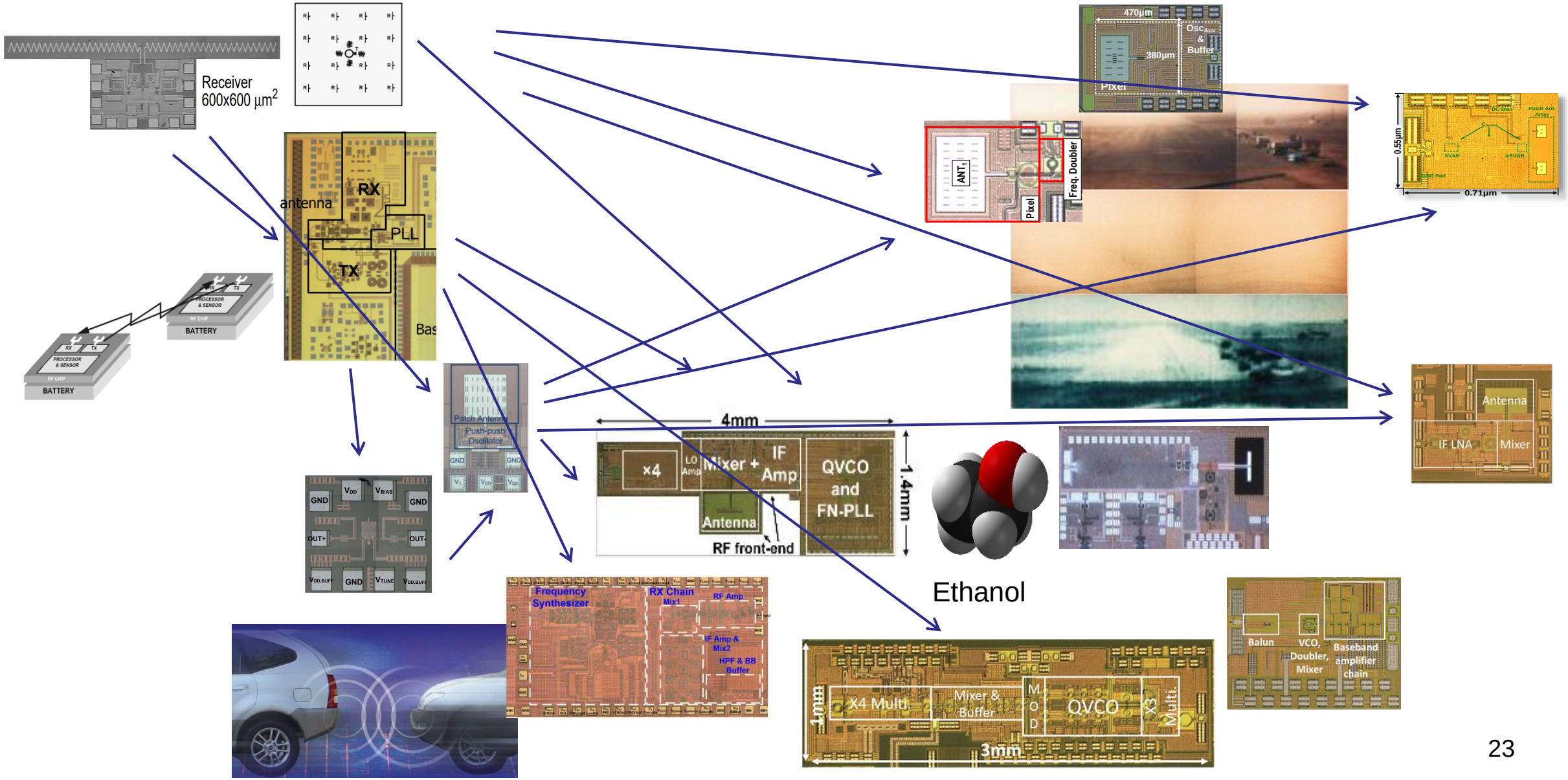
Enables		Noise Condition	
E1	E2	Label	Description
0	0	A	Small inverter chains on one side switching
0	1	B	All small inverter chains switching
1	0	C	Small and large inverter chains on one side switching
1	1	D	All inverter chains switching

Use of Wireless Clock Distribution



- Demonstrated the on-chip wireless clock.
- Research thread on using wireless communication in network on chip applications.
- Not aware of anybody using this on the Earth.
- On-chip wireless interconnection much easier than anybody has thought!!

Impact of Not Planned For



Conclusion

- **Failure in planning**
  - **Failure in understanding the difficulties**
- **Success**
  - **Progress toward goals**
  - **Unexpected learning**
  - **New research directions**
- **Not planned for is necessary for successful research**
- **More open to trying out new ideas and keep asking whether the perceived limitations are fundamental or not.**