Readiness for Custom/Advanced Semiconductor Packaging: SAMSUNG DS
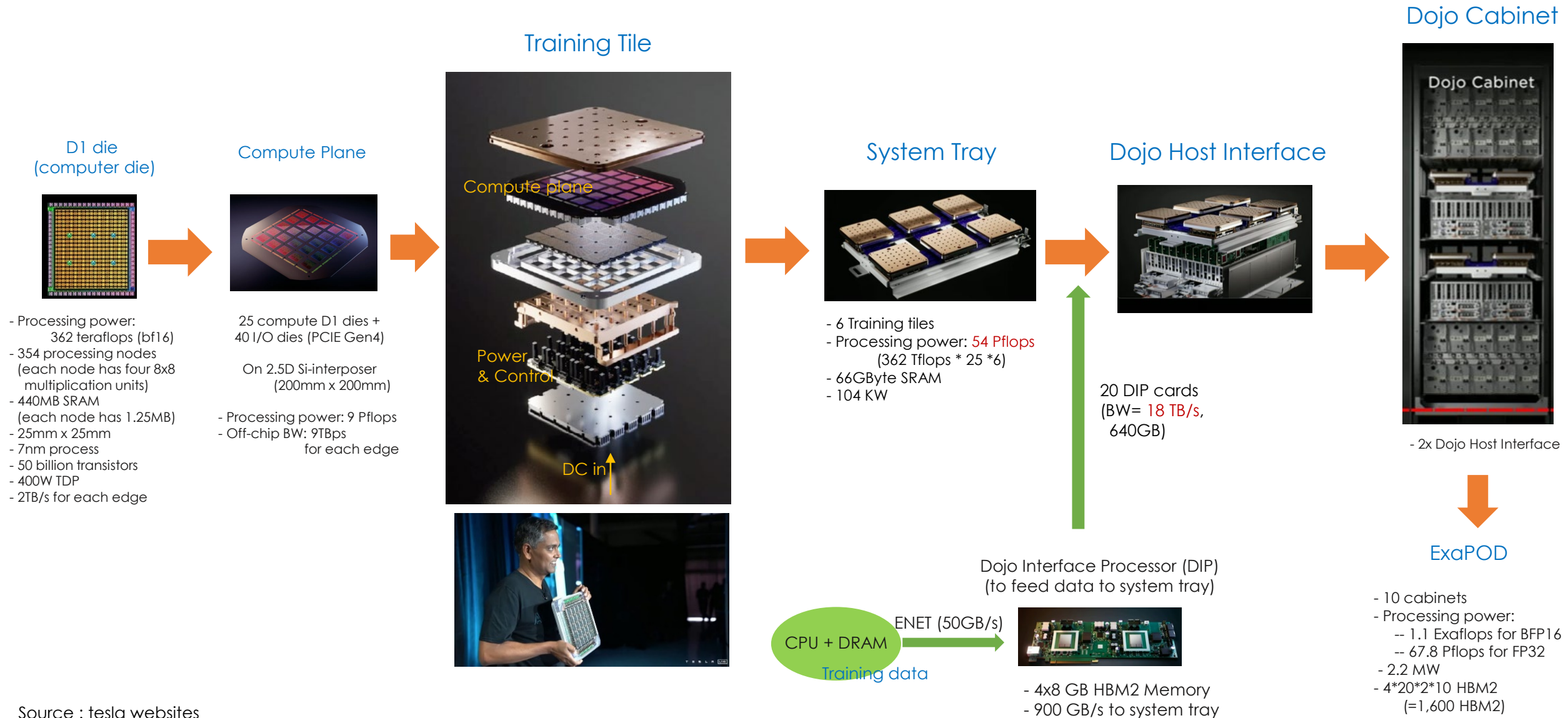
Oct. 25th, 2022

Vincent (Woopoung) Kim

**Packaging Solution Center,
Samsung Device Solution America**
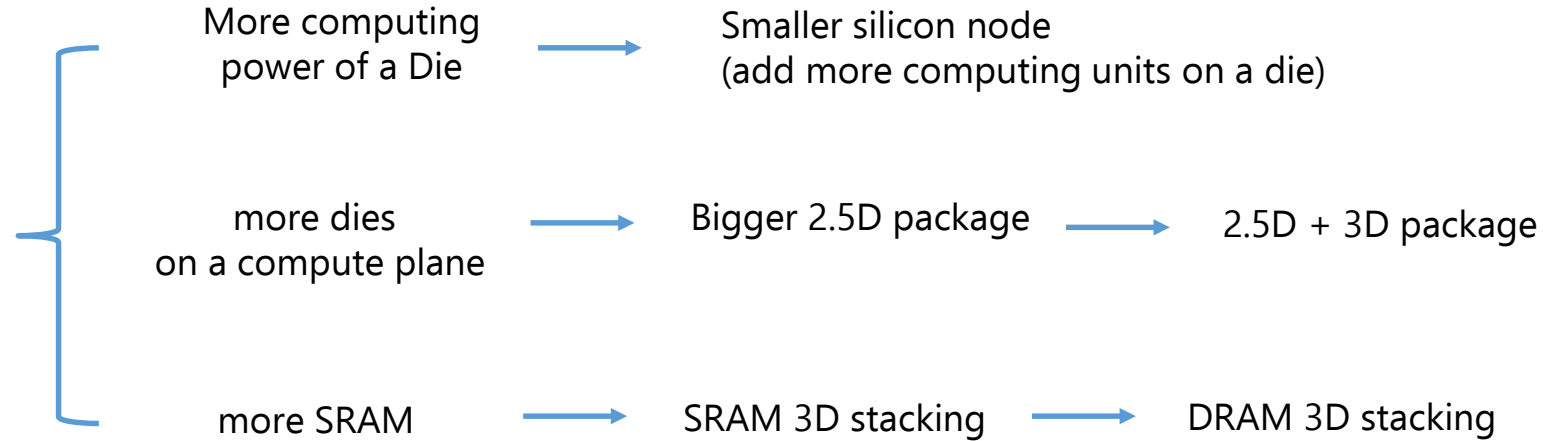
Tesla Dojo Exa-Flop (AI) Super-Computer
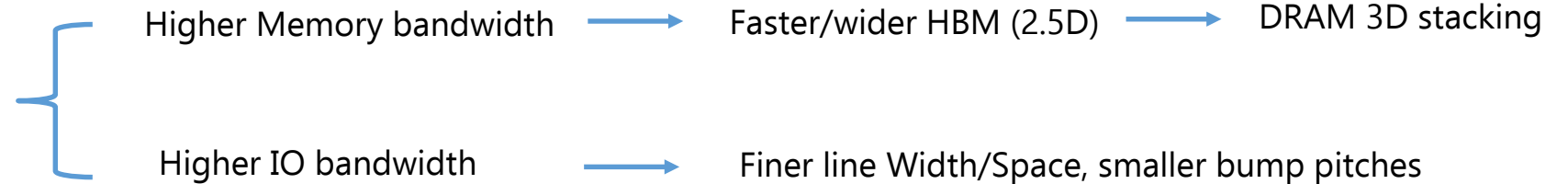
~5th fastest supercomputer (2022)

D1 die (computer die)

- Processing power:
  362 teraflops (bf16)
- 354 processing nodes
  (each node has four 8x8
  multiplication units)
- 440MB SRAM
  (each node has 1.25MB)
- 25mm x 25mm
- 7nm process
- 50 billion transistors
- 400W TDP
- 2TB/s for each edge

Compute Plane

25 compute D1 dies +
40 I/O dies (PCIE Gen4)

On 2.5D Si-interposer
(200mm x 200mm)

- Processing power: 9 Pflops
- Off-chip BW: 9TBps
  for each edge

Training Tile

Compute plane

Power & Control

DC in

System Tray

- 6 Training tiles
- Processing power: 54 Pflops
  (362 Tflops * 25 *6)
- 66GByte SRAM
- 104 KW

Dojo Host Interface

20 DIP cards
(BW= 18 TB/s,
640GB)

Dojo Interface Processor (DIP)
(to feed data to system tray)

CPU + DRAM

ENET (50GB/s)

Training data

- 4x8 GB HBM2 Memory
- 900 GB/s to system tray

Dojo Cabinet

- 2x Dojo Host Interface

ExaPOD

- 10 cabinets
- Processing power:
  -- 1.1 Exaflops for BFP16
  -- 67.8 Pflops for FP32
- 2.2 MW
- 4*20*2*10 HBM2
  (=1,600 HBM2)

Source : tesla websites

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Possible options to improve Dojo's performance

Options for Improvement of computing power

- More computing power of a Die → Smaller silicon node (add more computing units on a die)
- more dies on a compute plane → Bigger 2.5D package → 2.5D + 3D package
- more SRAM → SRAM 3D stacking → DRAM 3D stacking

Options for Improvement of Bandwidth

- Higher Memory bandwidth → Faster/wider HBM (2.5D) → DRAM 3D stacking
- Higher IO bandwidth → Finer line Width/Space, smaller bump pitches

Options for Improvement of Power Consumption

- a Die → Smaller silicon node
- 2.5D package → 3D stacking (by reducing channel capacitance and driver strength)

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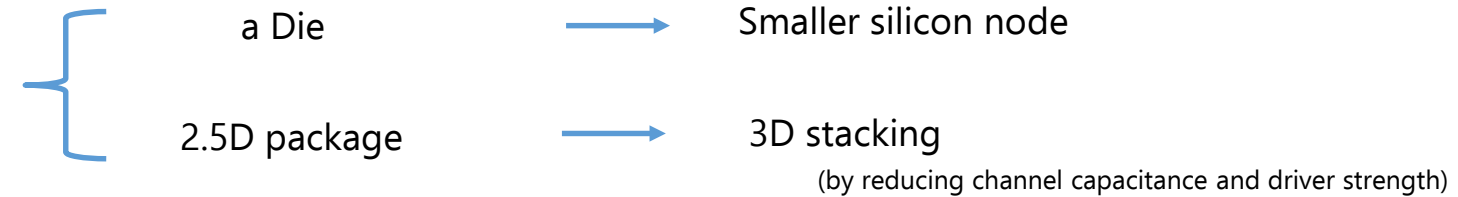
Driving force for Advanced Packaging

Need for
Higher performance
Systems

- Higher computation flops
- Higher Bandwidth
- Lower Power consumption

→

Bigger & Finer packages
2.5D
3D
2.5D + 3D
Fan-out PKG

→

Driving force for
Advanced packaging

⊕ **Advanced package = conventional package + RDL/Si interposer, bridge/TSV stacking**
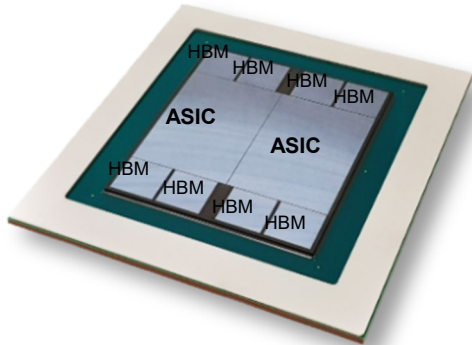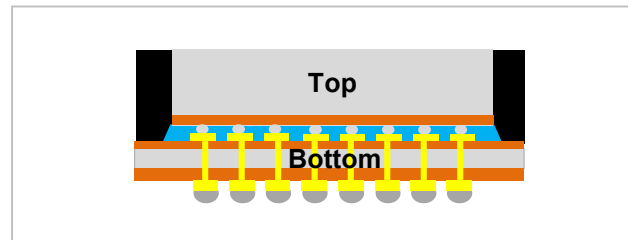 - Package architecture with fine pitch, 3D stack and advanced substrate

Our Advanced Package Scope

⊕ **Advanced package = conventional package + RDL/Si interposer, bridge/TSV stacking**
- Package architecture with fine pitch, 3D stack and advanced substrate
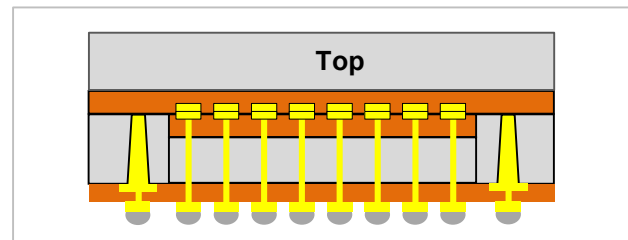
2.5D Package
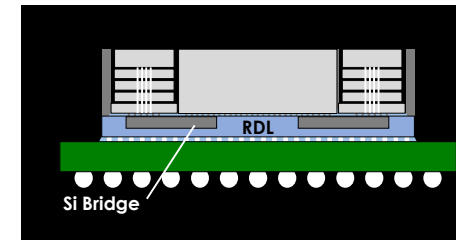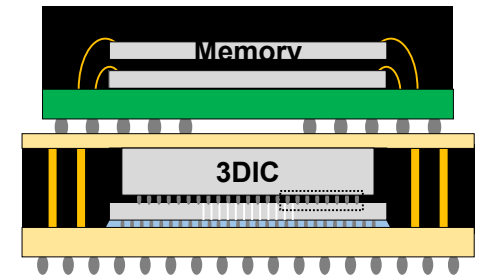- Si-interposer
- SI-bridge + PLP

3D Package

3.5D (2.5D + 3D) Package

Fan-out Package
- FOWLP
- FOPLP

TCB

HCB

SAMSUNG

Nature of Advanced Packaging

Tesla Dojo Super-Computer
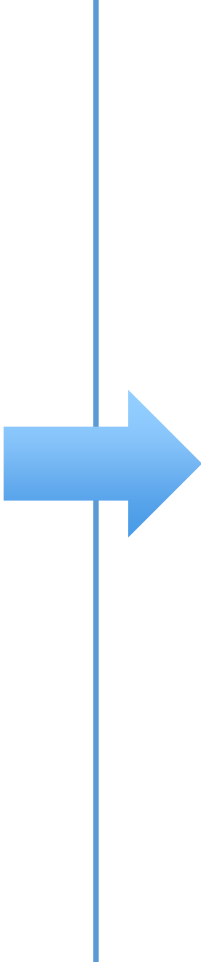
Advanced Packaging

Complex

Complex

Unique

Unique

Custom-made

Custom-made

Unique

Every package is different.

<u>Highlights of Advanced Packaging</u>

Significant system Performance improvement is possible

Unique form-factor design is possible

Can have various chiplet configurations

<u>Lowlights of Advanced Packaging</u>

Difficult to make off-the-shelf products

Would be more expensive

<u>Takes longer to make</u>

SAMSUNG

Custom-made

Advanced PKG = Custom PKG

working with customers closely to make advanced packages

↓

Open/stable/friendly environment to work together with customers

↓

We consider '*Package Foundry Business*'

In the 'Package Foundry Business', customers can configure their packages using multiple dies with their choice.

Summary

- The demand for higher performance drives the development of advanced packages
    - In AI/HPC, 2.5D/3D/3.5D
    - In mobile, FOPKG (FOWLP/FOPLP)

- There are lots of challenges to overcome in advanced packaging to make
    - Bigger & finer packages
    - 2.5D, 3D, 3.5D (2.5D + 3D)

- Advanced Packaging is complex, unique, and custom-made

- In order to support the innovation of customers, we are preparing an open/stable/friendly environment
    - Customers can configure their packages with multi dies

- Are we ready for the advanced/custom semiconductor packages?
    - Yes or no