# III-V MOSFETs for Logic: From Failure to Success and Back?

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**SRC "From Failure to Success" Seminar Series**

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Acknowledgements:

- Students and collaborators: D. Antoniadis, X. Cai, J. Grajal, J. Lin, W. Lu, A. Vardi, X. Zhao
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- Labs at MIT: MTL, EBL, MIT.nano, MRL

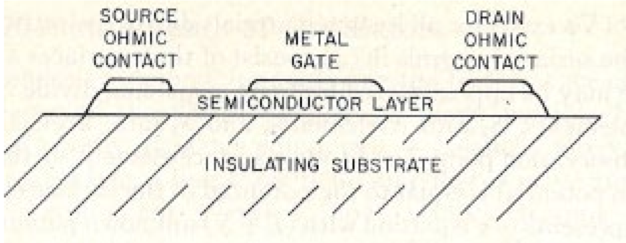
# Contents

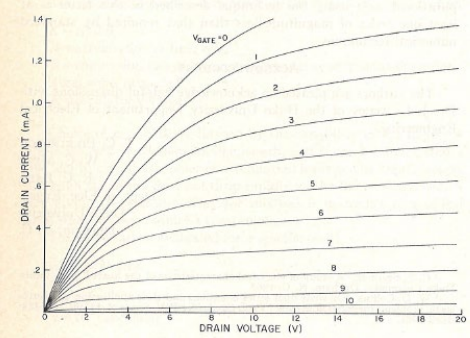
GaAs: the semiconductor of the future
or the quest for III-V logic

1. GaAs MESFETs
2. GaAs and InGaAs HEMTs
3. InGaAs MOSFETs
4. Going forward

# 1. GaAs Metal-Semiconductor Field-Effect Transistor (MESFET)

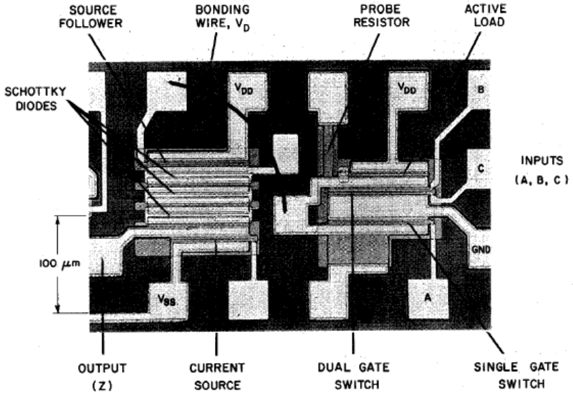
First MESFET



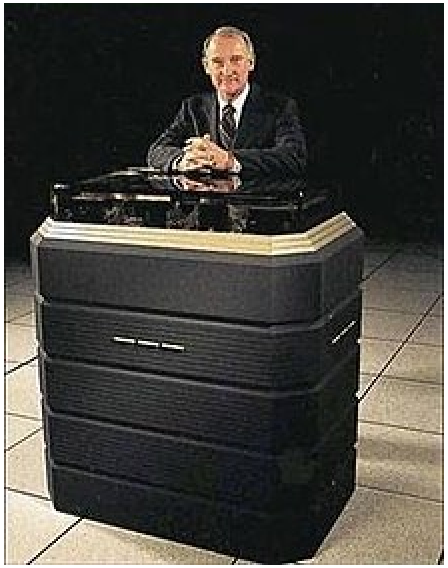


Mead, Proc IEEE 1966

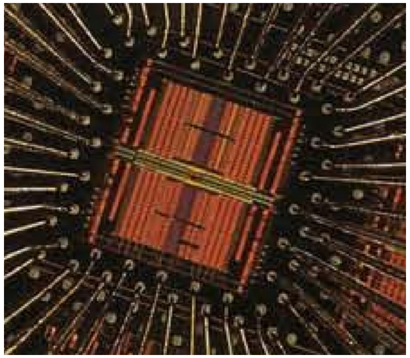
First MESFET IC



Van Tuyl, JSSC 1974

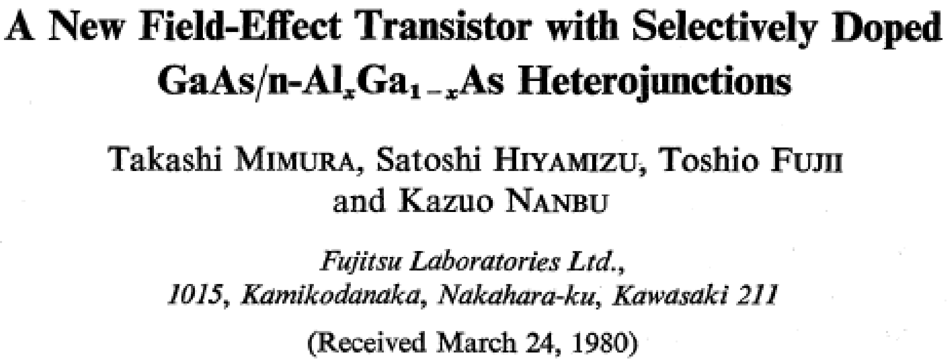


Cray-3 Supercomputer, 1993



GaAs MESFET ICs by GigaBit Logic

# 2. The High Electron Mobility Transistor (HEMT)

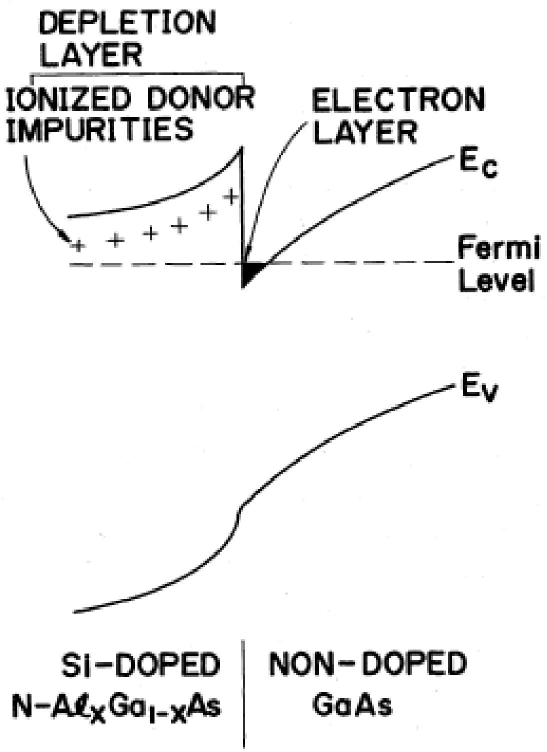


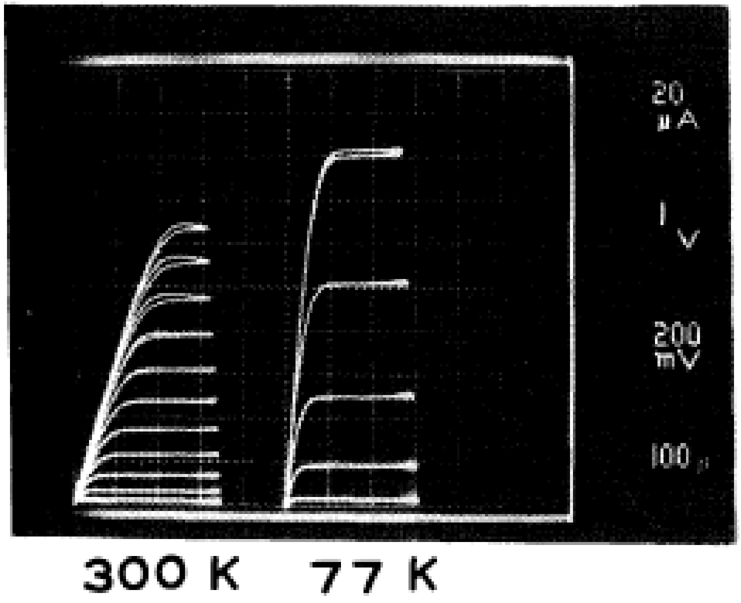
**A New Field-Effect Transistor with Selectively Doped GaAs/n-$Al_xGa_{1-x}As$ Heterojunctions**

Takashi MIMURA, Satoshi HIYAMIZU, Toshio FUJII
and Kazuo NANBU

*Fujitsu Laboratories Ltd.,*
*1015, Kamikodanaka, Nakahara-ku, Kawasaki 211*

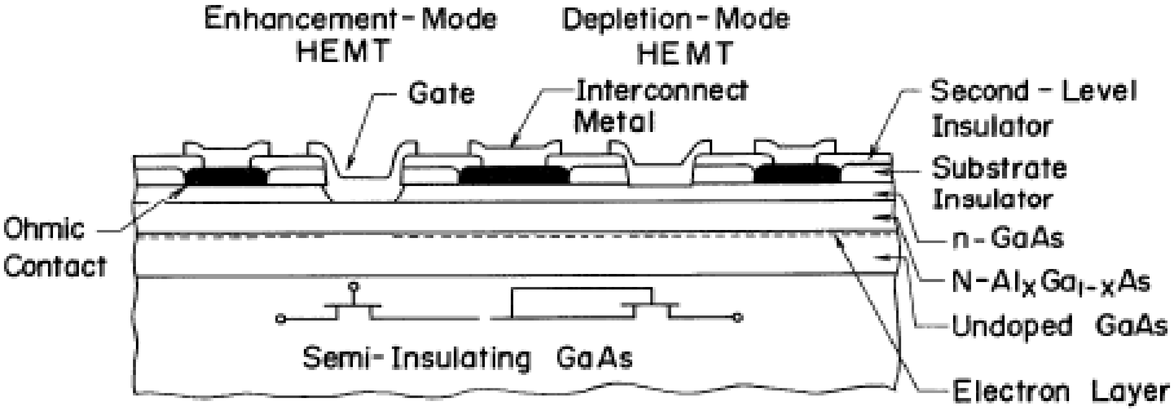
(Received March 24, 1980)



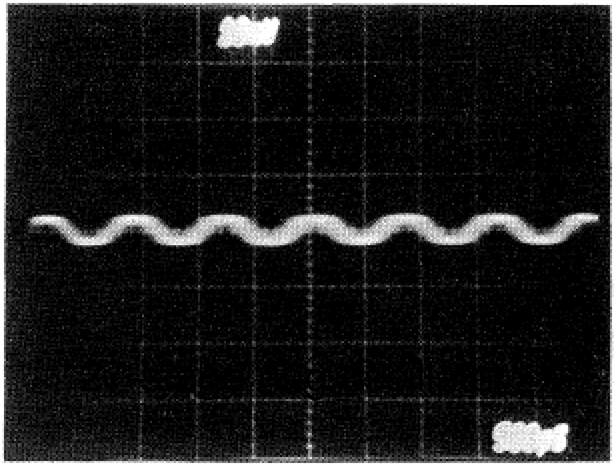


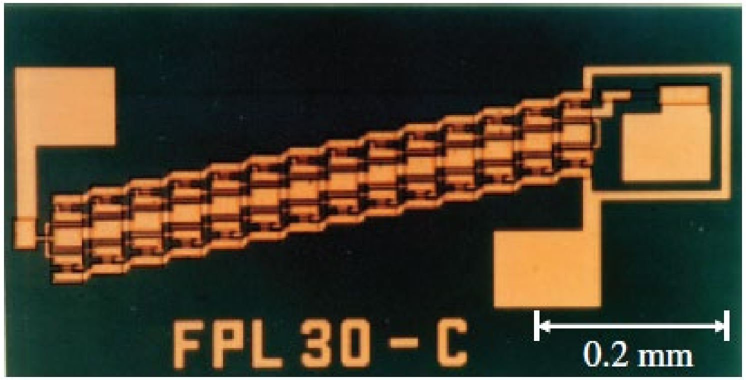
Mimura, JJAPL 1980

# First HEMT IC



E/D logic



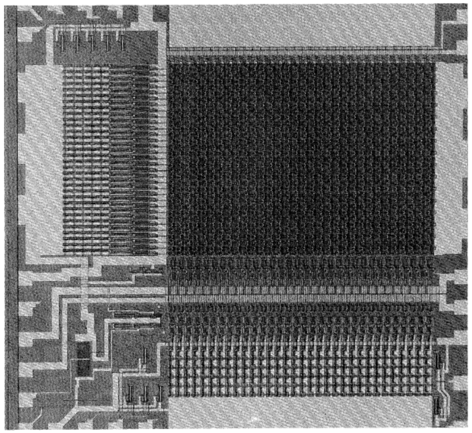


*"The switching delay of 17.1 ps is the lowest of all the semiconductor logic technologies reported thus far."*

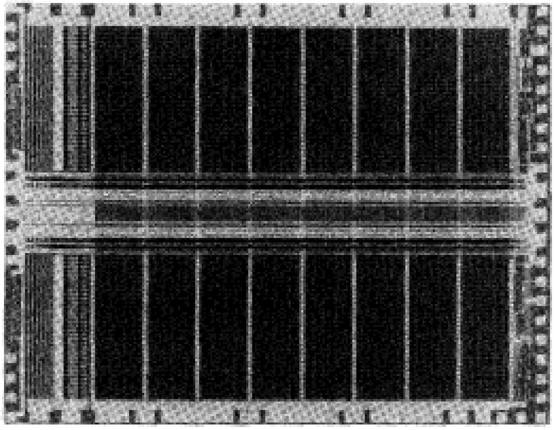
Mimura, JJAPL 1981

*"HEMT technology is presenting new possibilities for high-speed low-power very-large-scale-integration."*

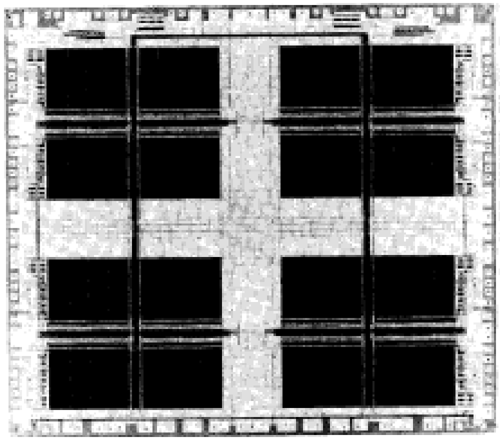
# HEMT ICs ride Moore's Law



1 Kb SRAM



16 Kb SRAM



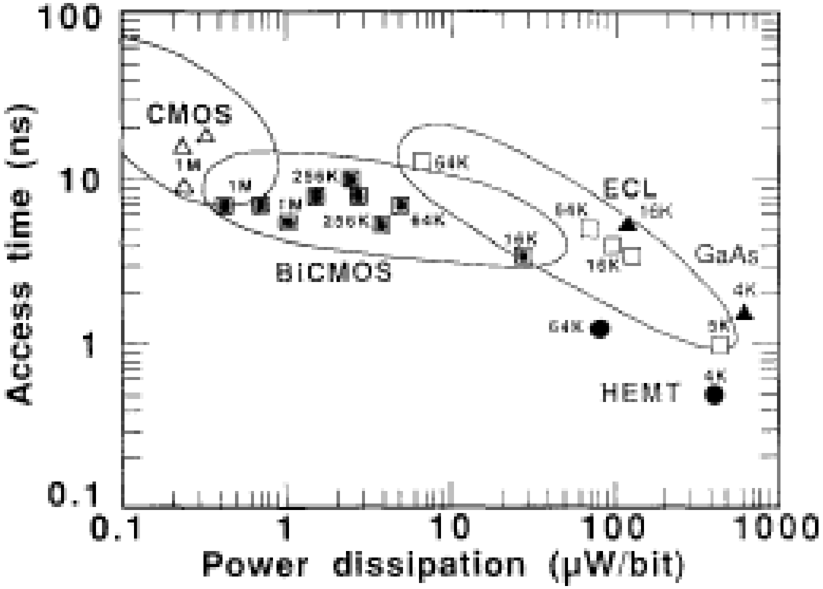
64 Kb SRAM

1984: 1 Kb SRAM (7,244 HEMTs, 8.7 mm$^2$)

1984: 4 Kb SRAM (26,864 HEMTs, 21 mm$^2$)

1987: 16 Kb SRAM (107,519 HEMTs, 24 mm$^2$)

1991: 64 Kb SRAM (>462,000 HEMTs, 48 mm$^2$)



Watanabe, TED 1987

Suzuki, JSSC 1991

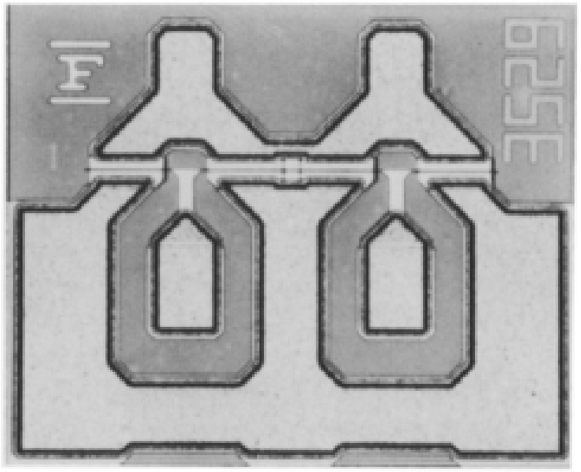
Abe, JSSC 1991

Abe, JVST1987

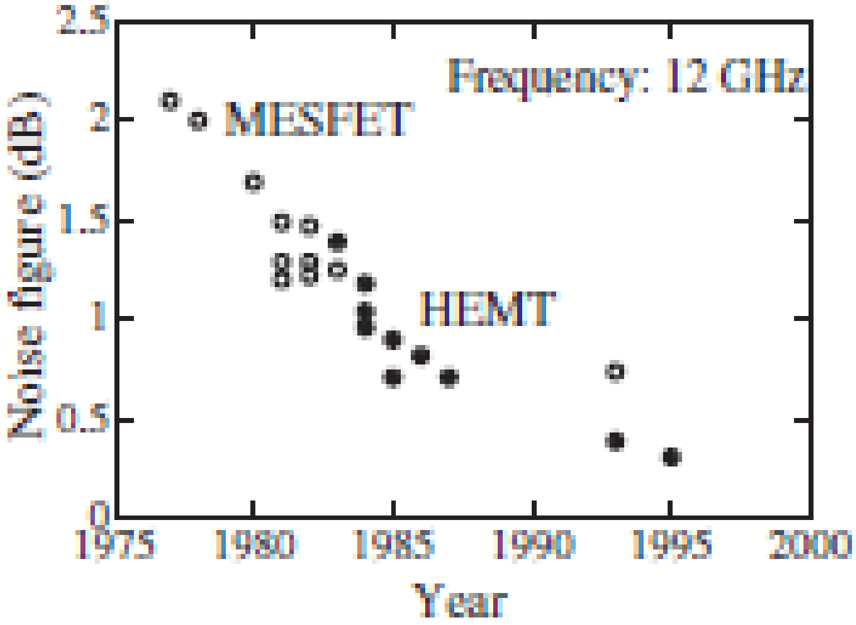
# HEMT Low-Noise Amplifier

First mass-market product (1987):

0.25 µm GaAs HEMTs for LNA of Direct Broadcasting Satellite receiver



Mimura, Surf Sci 1990

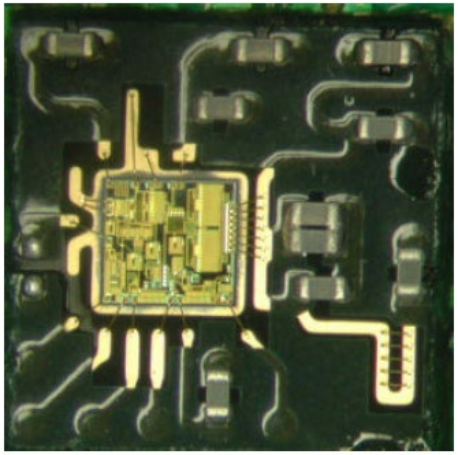


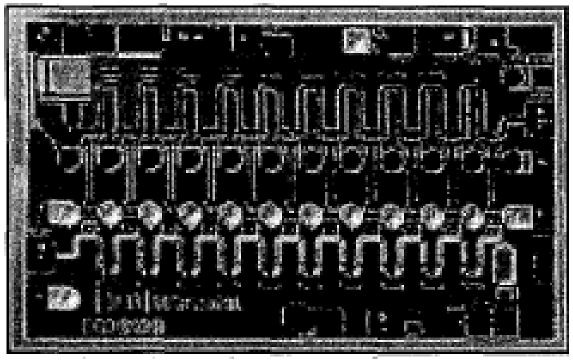
By 1988, world wide production of HEMT receivers: 20 million/year

# GaAs HEMT Electronics

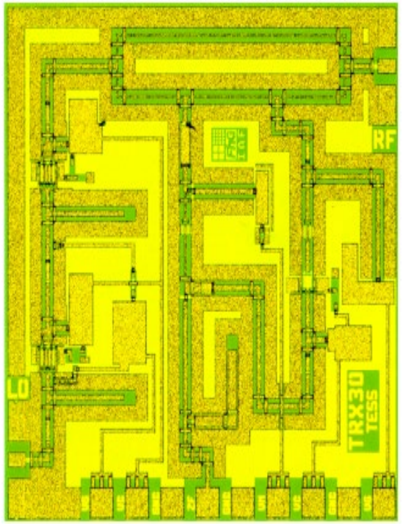
**TriQuint and Skyworks Power iPhone 5**

UMTS-LTE PA module
Chow, MTT-S 2008

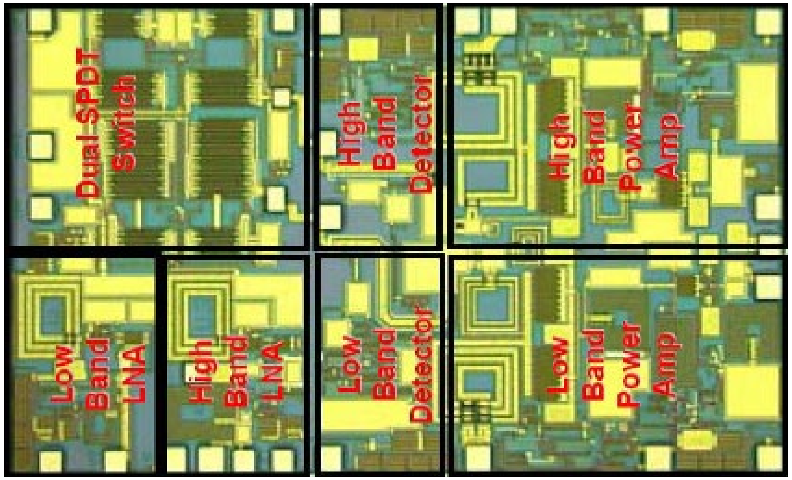




40 Gb/s modulator driver
Carroll, MTT-S 2002

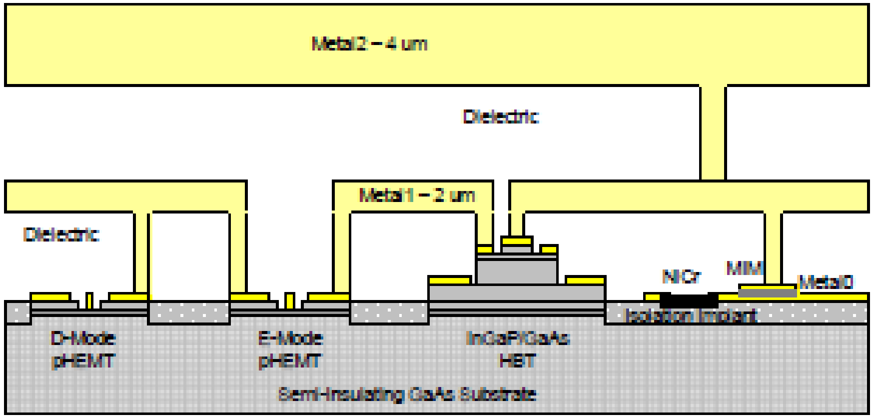


77 GHz transceiver
Tessmann, GaAs IC 1999



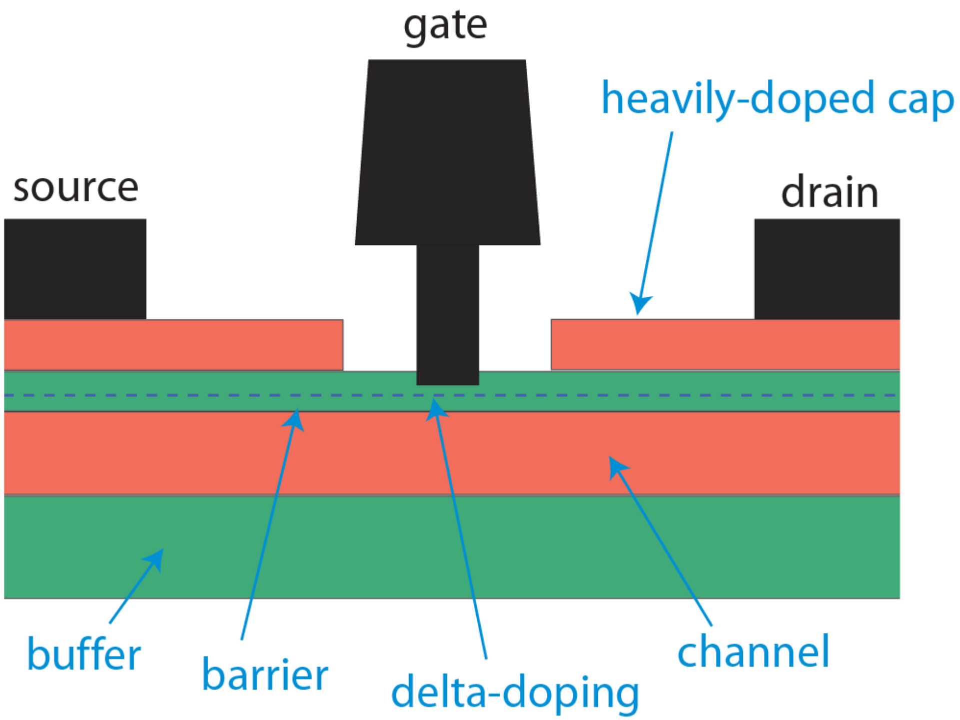
Single-chip WLAN MMIC, Morkner, RFIC 2007

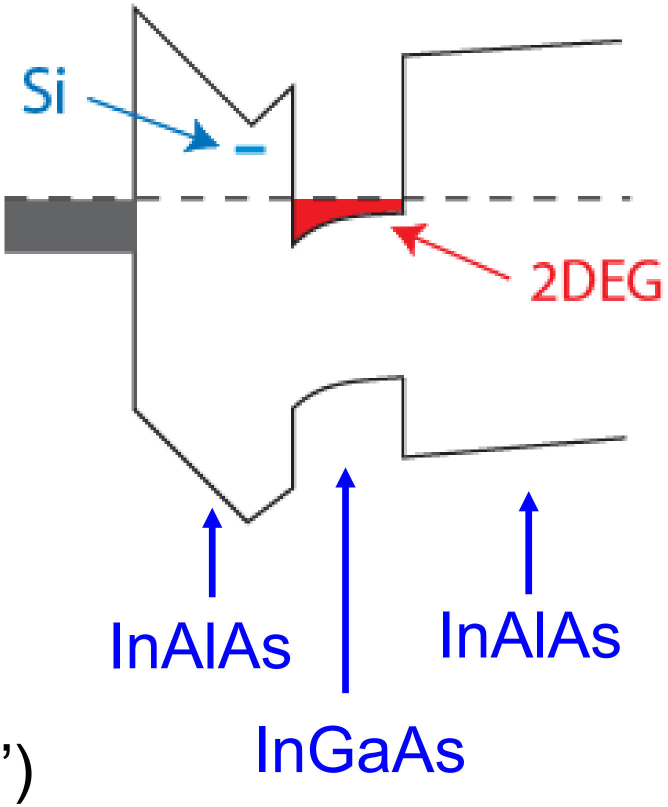
Bipolar/E-D PHEMT process



Henderson, Mantech 2007

# InGaAs Quantum-Well HEMT

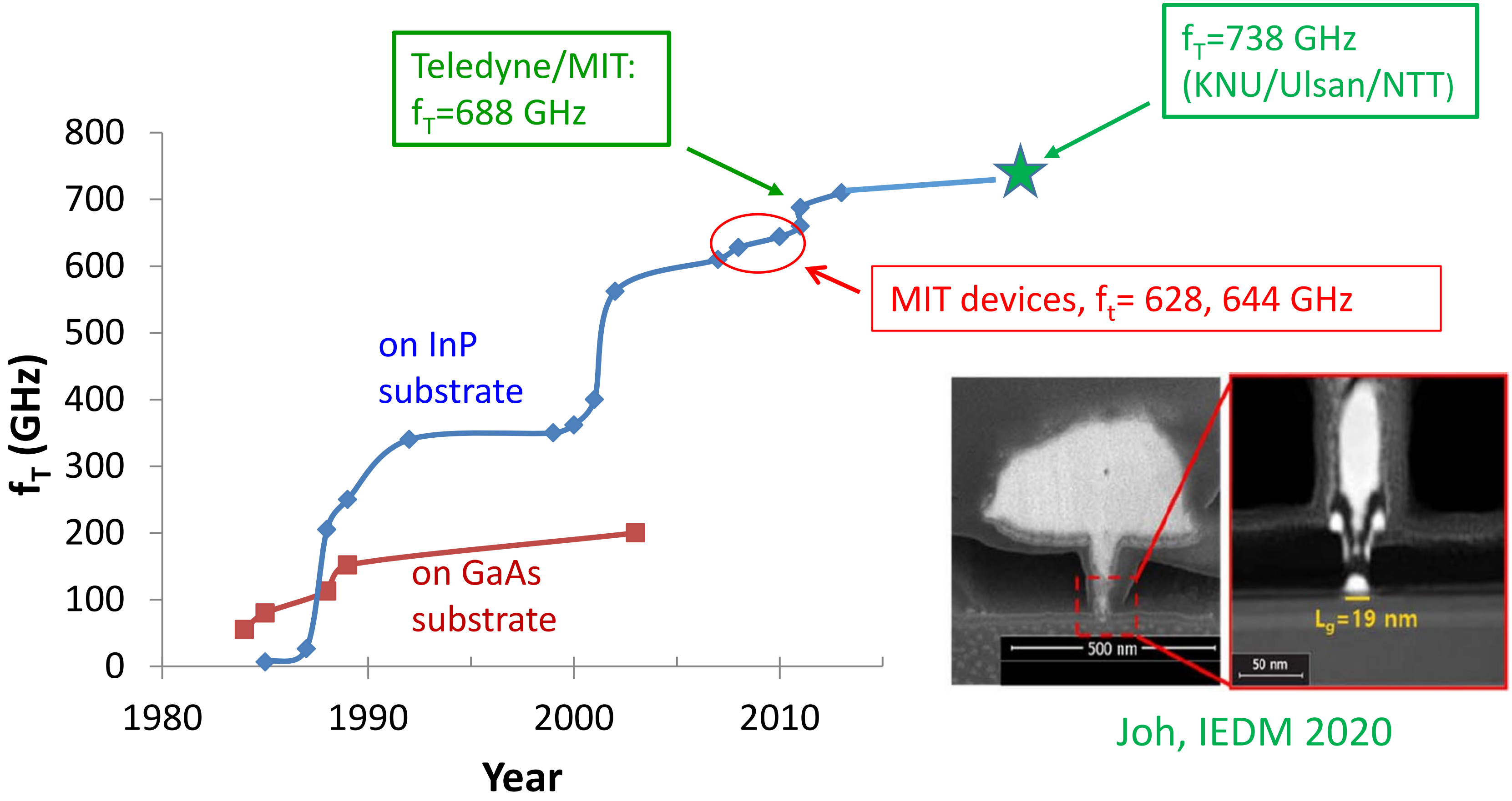




Key features:

- InP lattice constant ("InP HEMT")
- Quantum-well channel
- Delta doping

# InGaAs HEMT: $f_t$ record vs. time


Teledyne/MIT: $f_T$=688 GHz

$f_T$=738 GHz (KNU/Ulsan/NTT)

MIT devices, $f_t$= 628, 644 GHz

on InP substrate

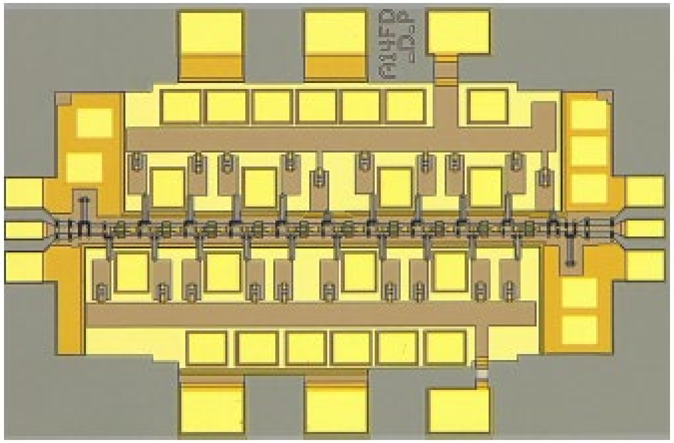
on GaAs substrate

Joh, IEDM 2020

- Highest $f_T$ of any FET on any material system
- Little progress in last 10 years → InGaAs HEMT at scaling limit

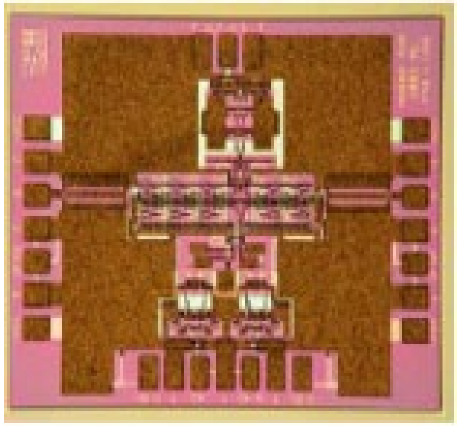
# InGaAs HEMTs: circuit demonstrations

10-stage 670 GHz LNA

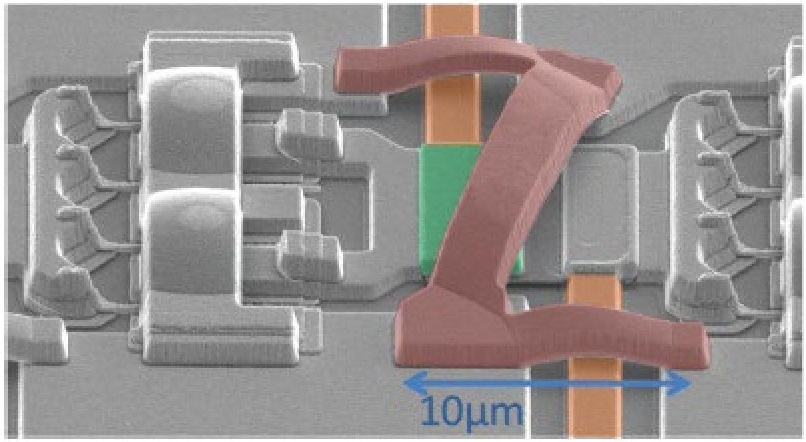


Leong, IPRM 2012

80 Gb/s multiplexer IC

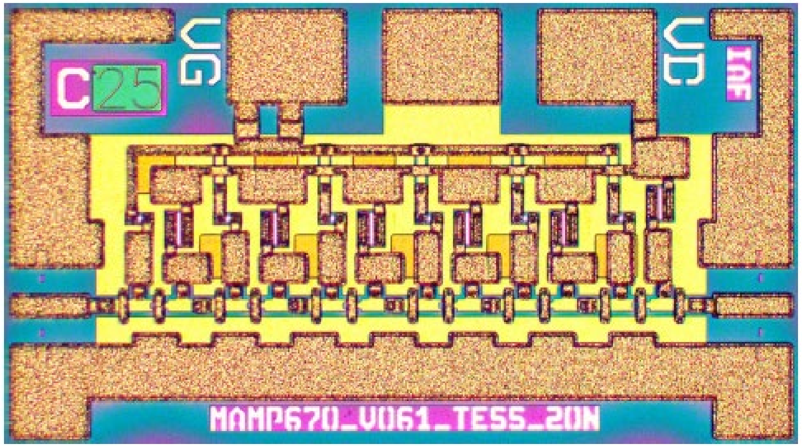


Wurfl, GAAS 2004



Sarkozy, IPRM 2013

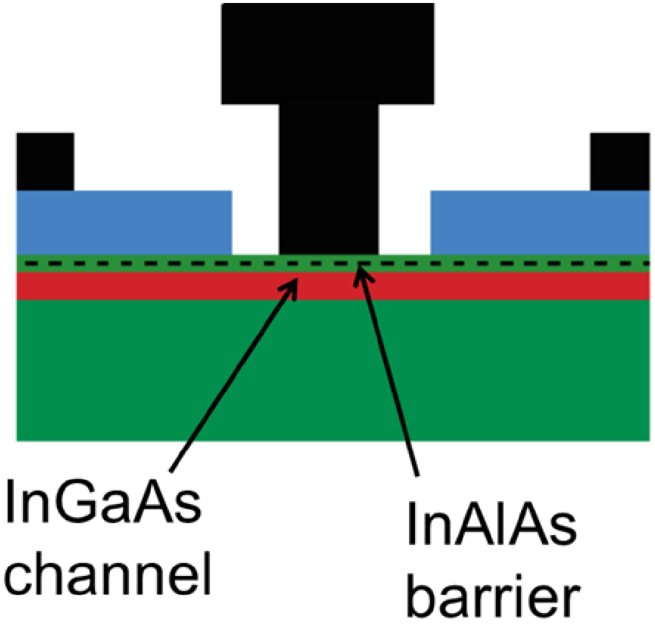
6-stage 600 GHz LNA

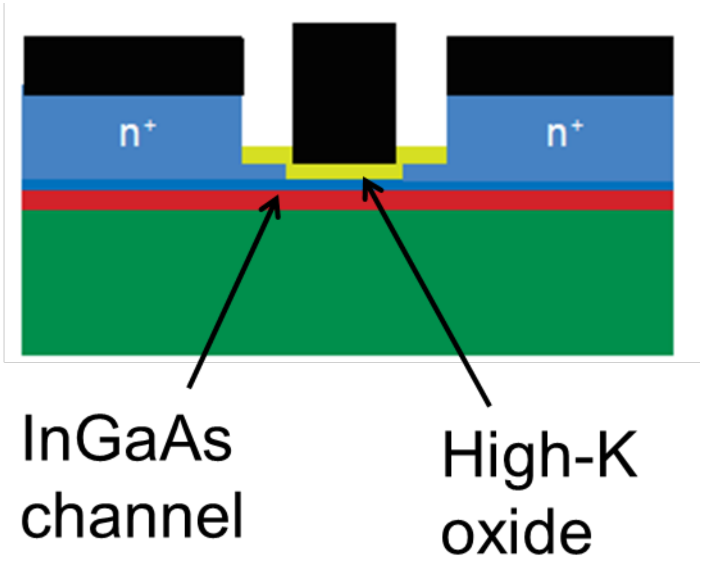


Tessmann, CSICS 2012

# 3. InGaAs HEMT vs. MOSFET

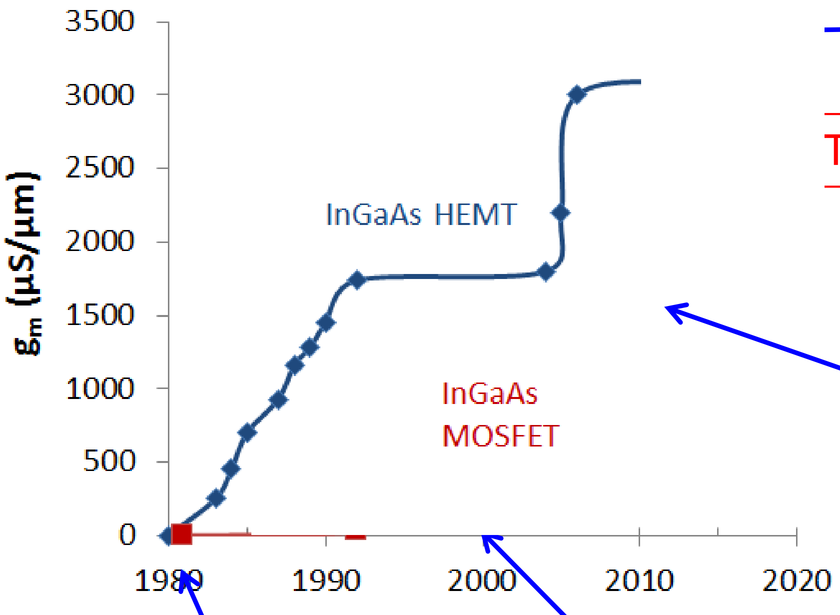
HEMT not suitable for logic: too much gate leakage current



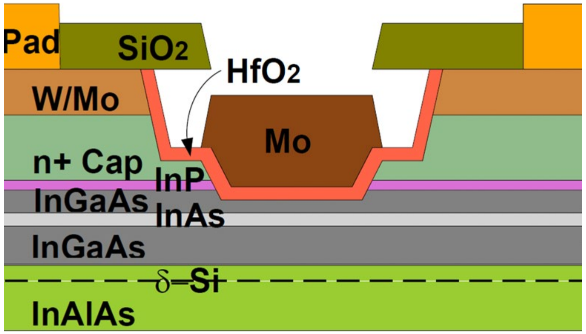


MOSFET incorporates gate oxide → gate leakage suppressed

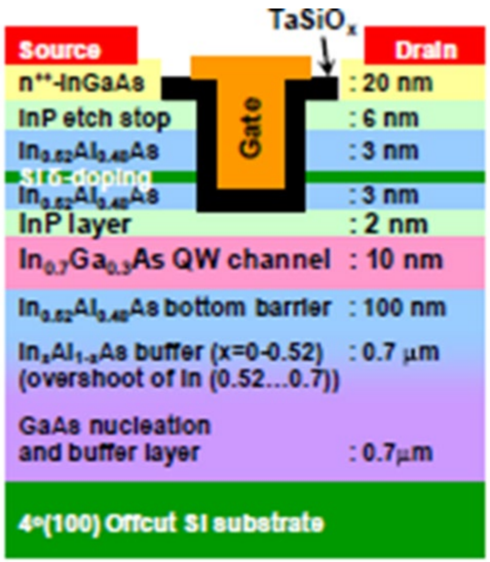
# Historical evolution: InGaAs MOSFETs vs. HEMTs

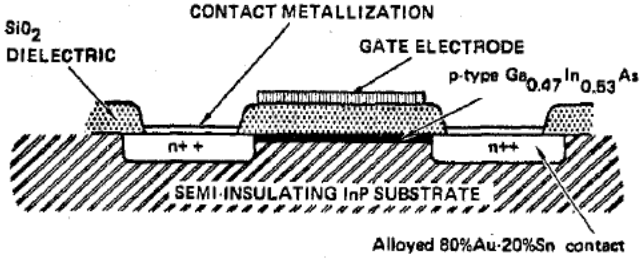


T devices

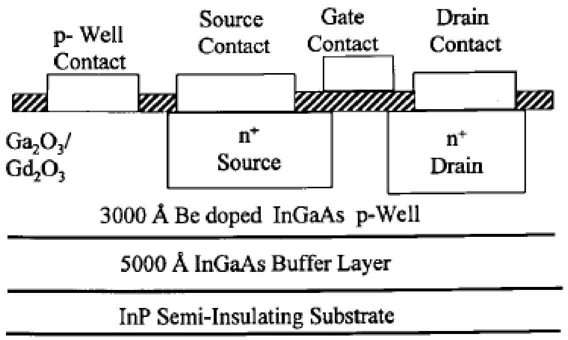


Lin, IEDM 2013





Wieder, EDL 1981



Ren, EDL 1998

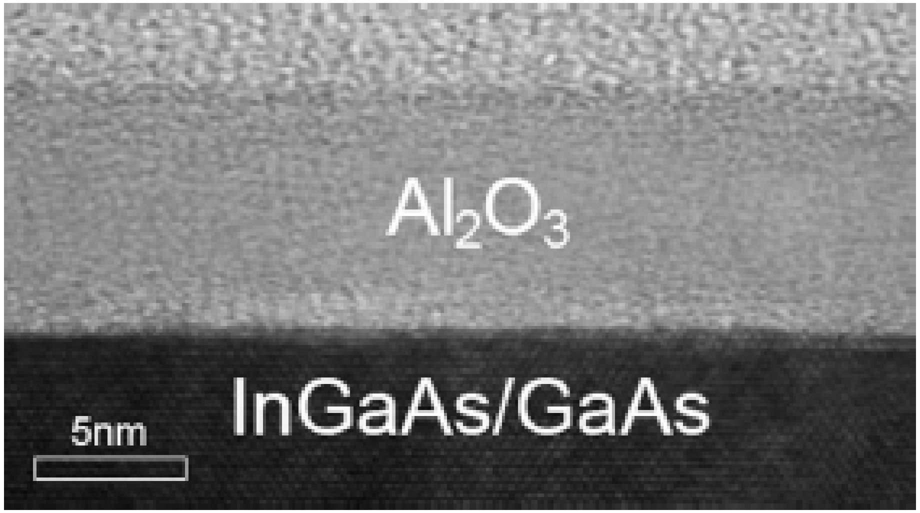
Radosavljevic, IEDM 2009

Progress reflects improvements in oxide/III-V interface

# What made the difference?
# Atomic Layer Deposition (ALD) of oxide

ALD eliminates surface oxides that pin Fermi level

→ "Self cleaning"



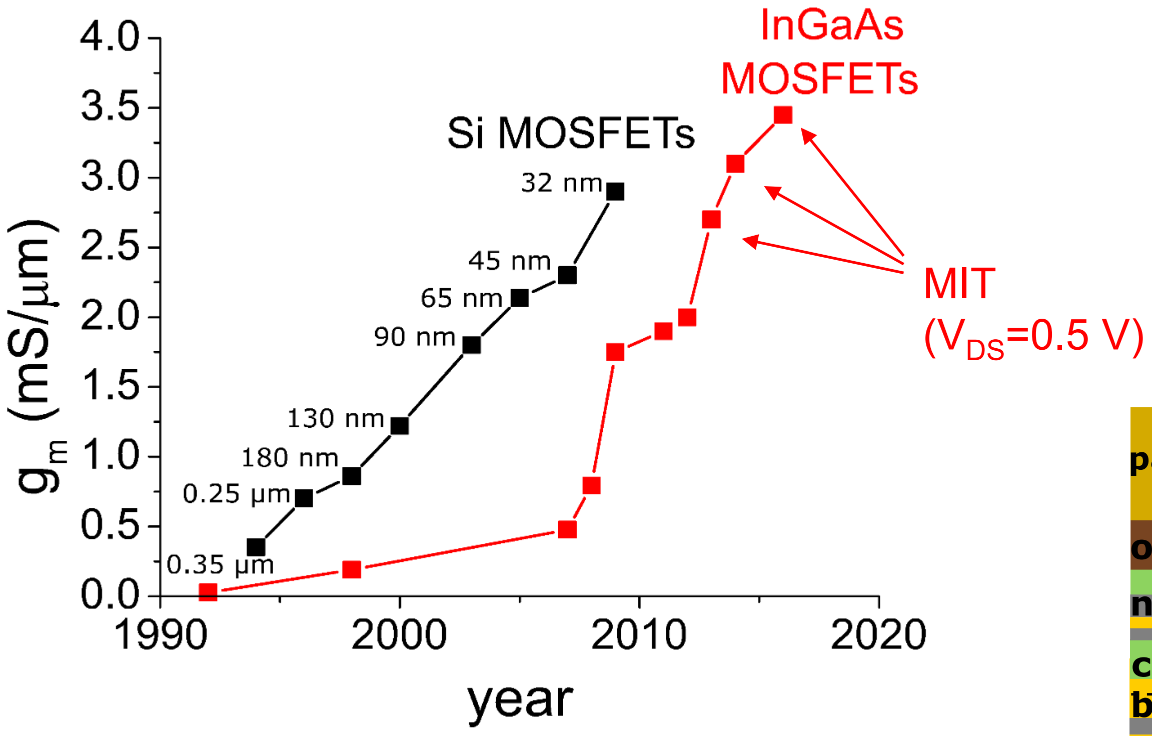
Huang, APL 2005

← Clean, smooth interface without surface oxides

- First observed with $Al_2O_3$, then with other high-K dielectrics
- First seen in GaAs, then in other III-Vs

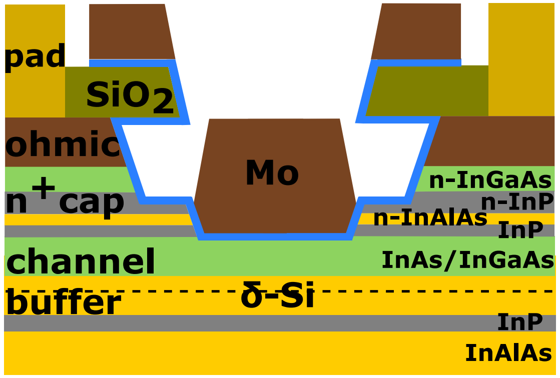
# Transconductance of Planar Si vs. InGaAs MOSFETs

n-MOSFETs in Intel's nodes at nominal voltage



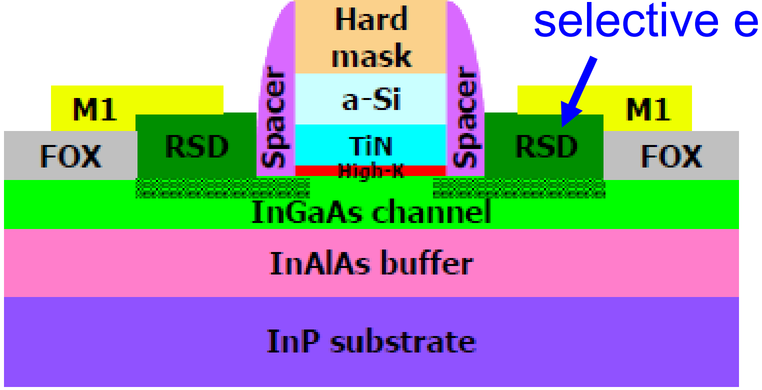
- InGaAs exceeds Si
- Rapid recent progress

*"Comparisons always fraught with danger…"*



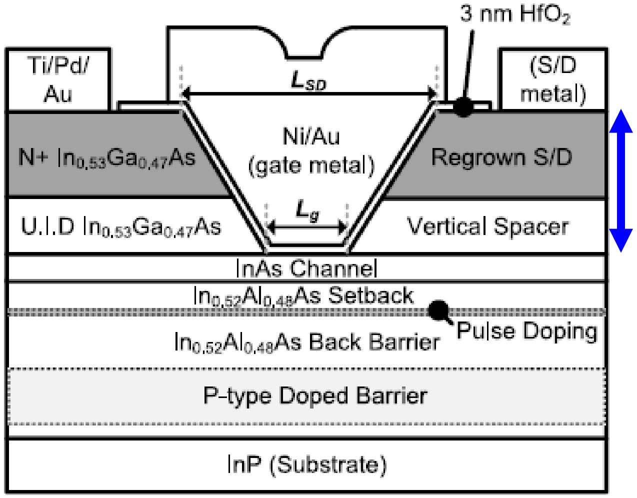
Lin,
IEDM 2014
EDL 2016

# Self-aligned Planar InGaAs MOSFETs



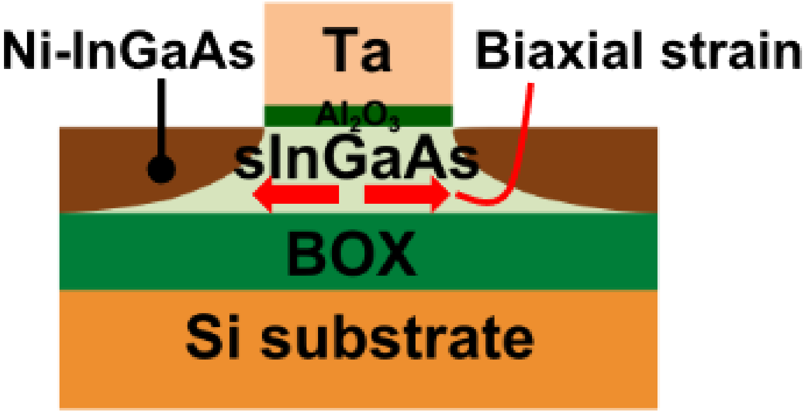
implanted Si + selective epi

Sun, IEDM 2013, 2014 (IBM)

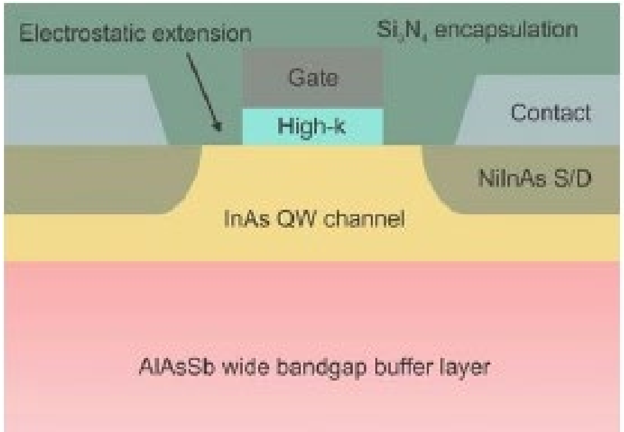


selective MOCVD

Huang, IEDM 2014 (UCSB)



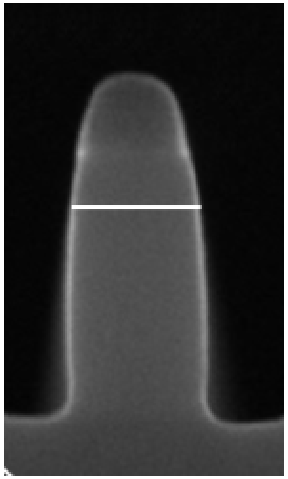
Kim, VLSI 2012 (U Tokyo)



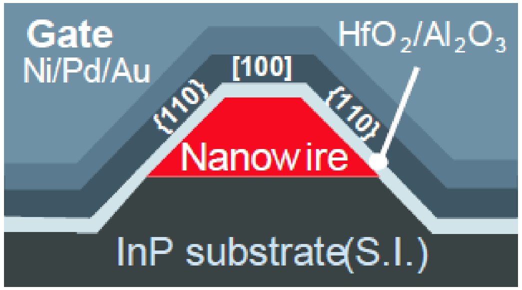
reacted NiInAs

Chang, IEDM 2013 (TSMC)

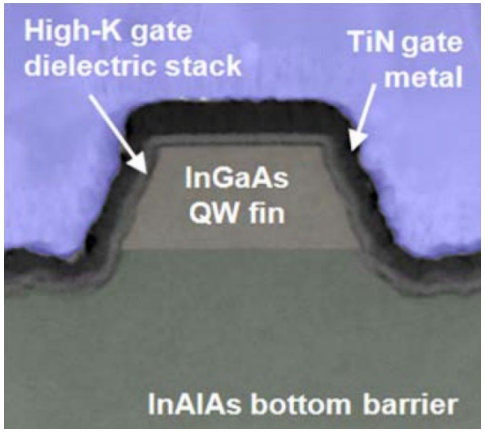
# InGaAs FinFETs



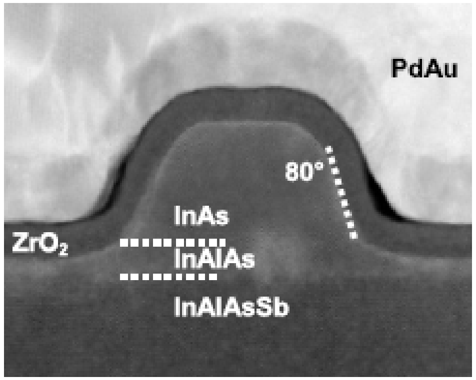
Kim, IEDM 2013 (Sematech)



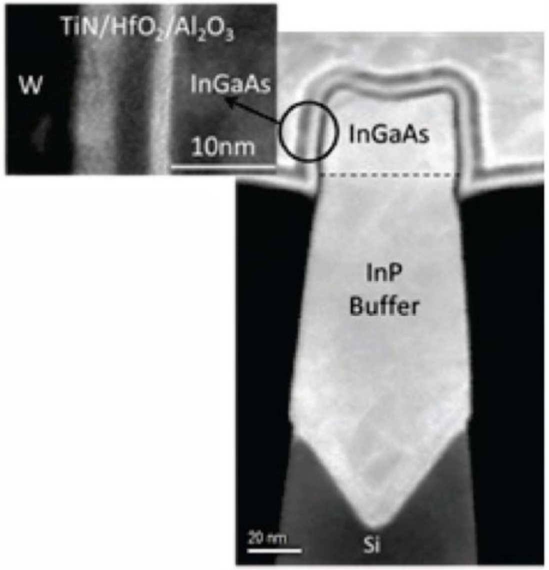
Zora IEDM 2016 (Lund U)



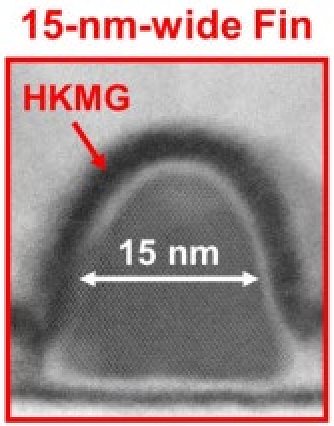
Radosavljevic, IEDM 2011 (Intel)



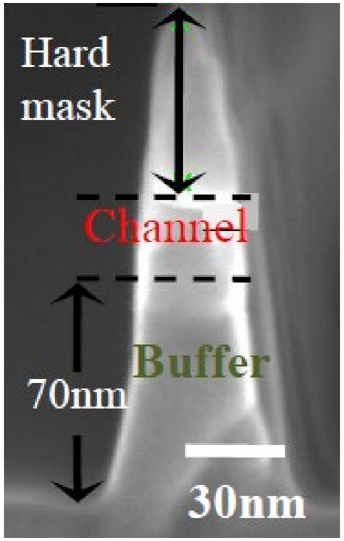
Oxland, EDL 2016 (TSMC)



Waldron VLSI 2014 (IMEC)



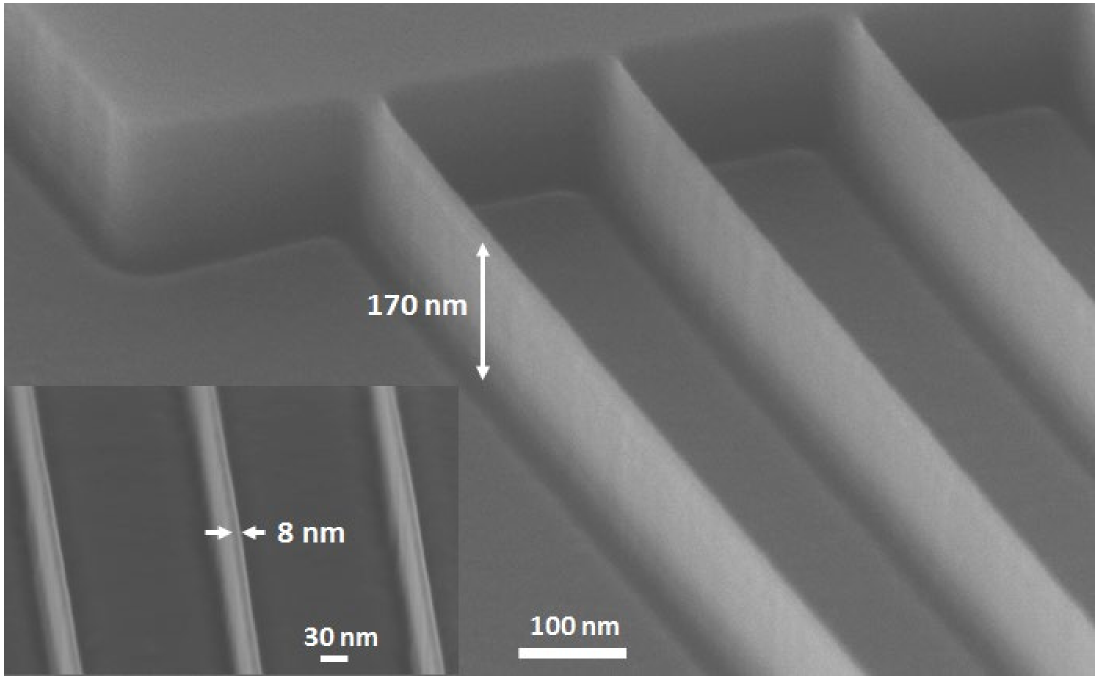
Djara, EDL 2016 (IBM)

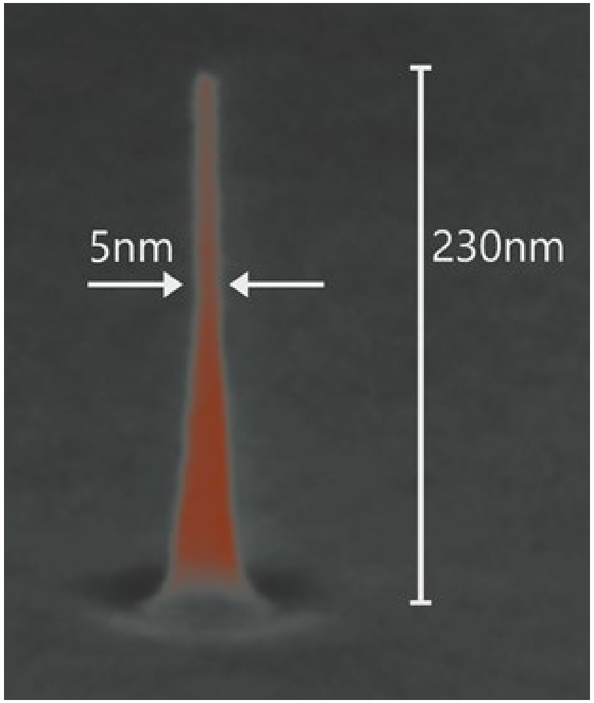


Thathachary, VLSI 2015 (Penn St.)

# Nanoscale 3D Etching of InGaAs

Top-down approach using $BCl_3/SiCl_4/Ar$ RIE + digital etch





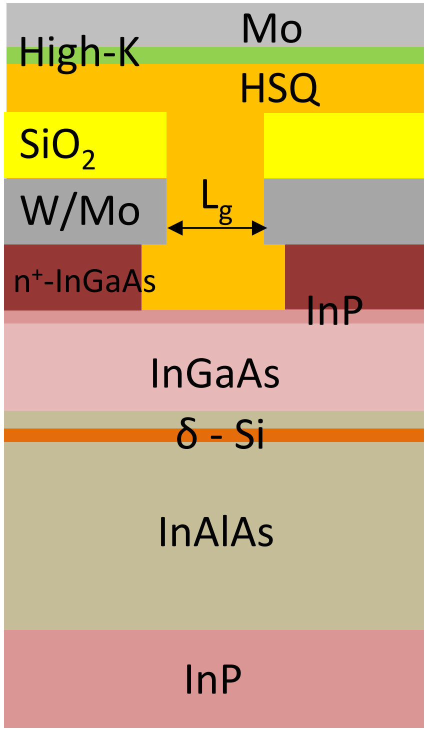
Vardi,
VLSI 2016,
EDL 2016,
IEDM 2017

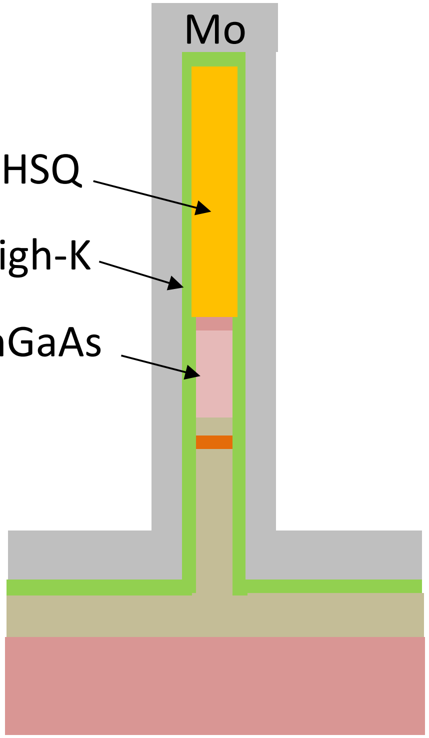
- Sub-10 nm fin width
- Aspect ratio > 20
- Vertical sidewalls

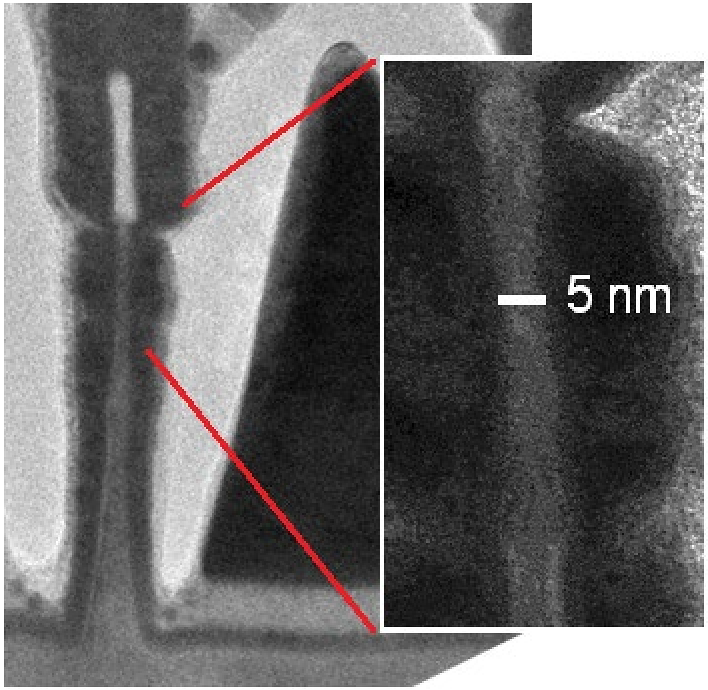
D=5 nm
Aspect Ratio > 40

Lu, EDL 2017

# MIT’s Nanoscale InGaAs FinFETs





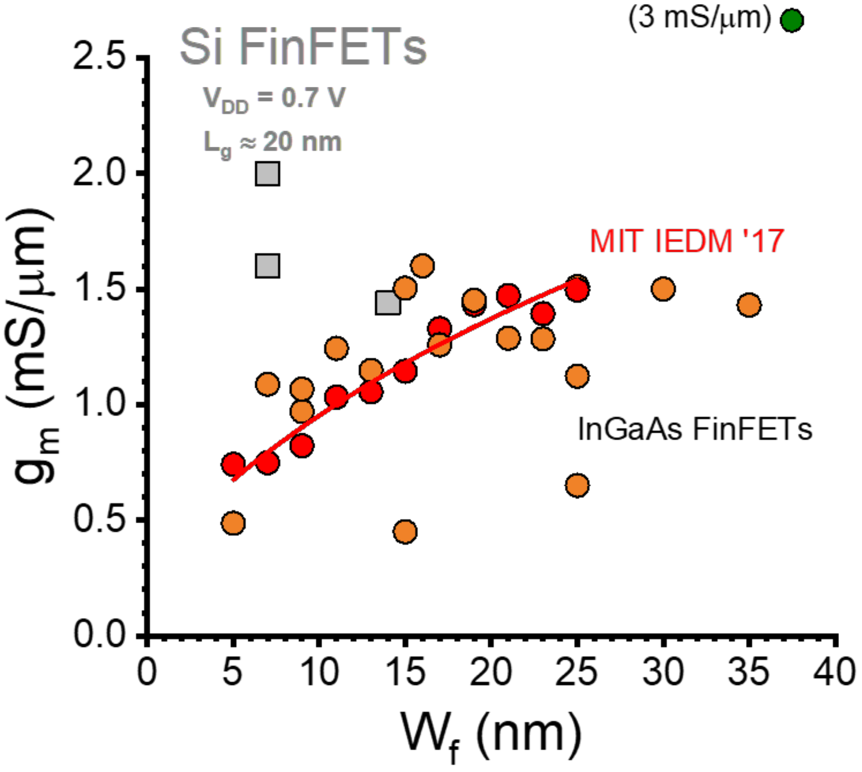


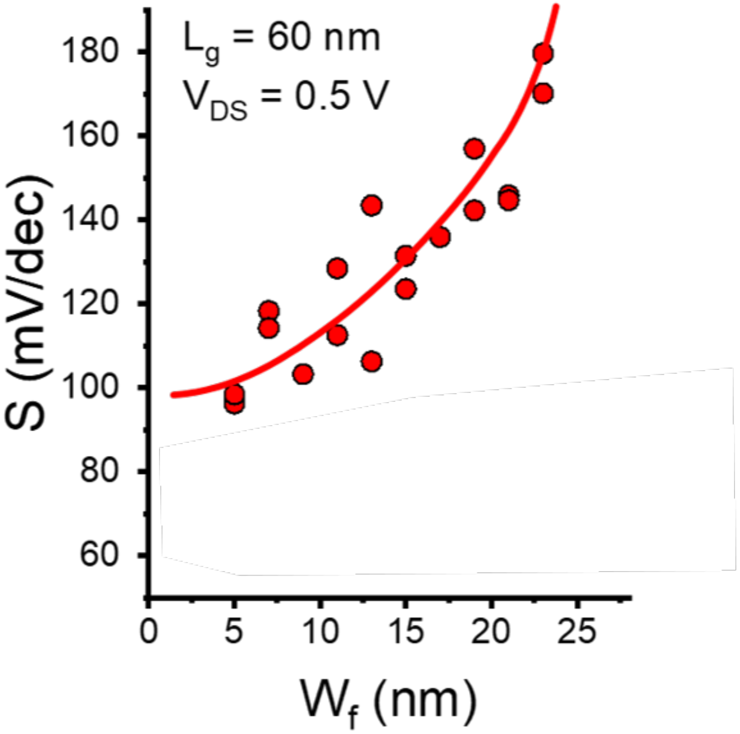
Vardi, IEDM 2017

- Si-compatible process
- Contact-first, gate-last process
- Fin etch mask left in place → double-gate MOSFET

# Fin-Width Scaling of InGaAs FinFETs

Vardi, IEDM 2017

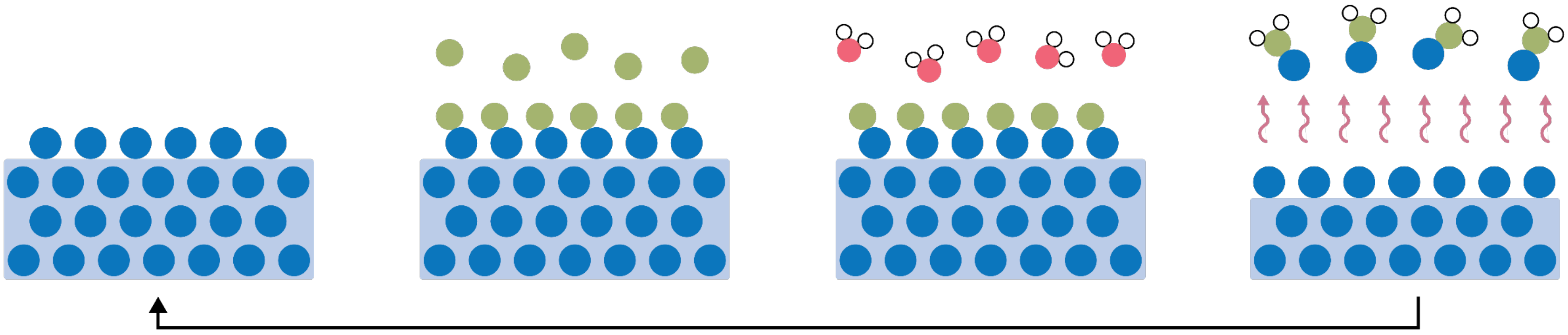




- Poor $W_f$ scaling of $g_m$ and S
- $g_m$ well below that of Si FinFETs

# Thermal Atomic Layer Etching

Gentle etching process: gas-phase, plasma free



InGaAs

HF-py:

fluorination

DMAC:

ligand exchange

Thermal release

@ 300°C

- HF-pyridine: fluorinates surface
- DMAC (dimethyl-aluminum chloride): etches surface
- Isotropic

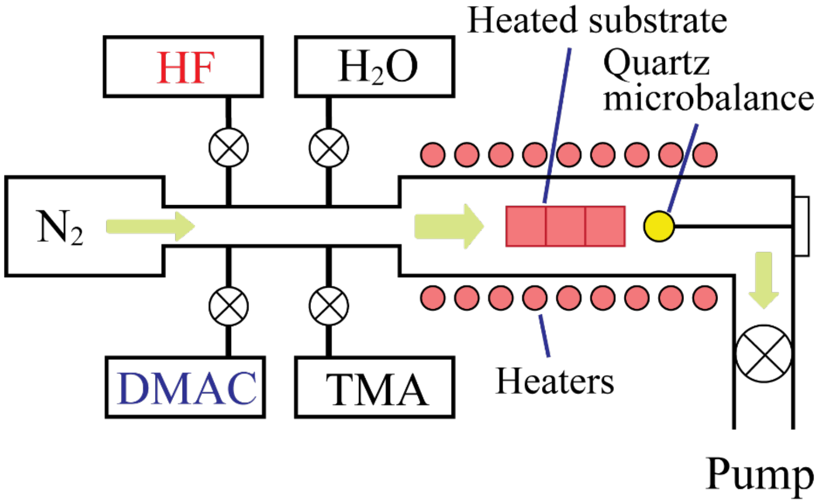
Lu, IEDM 2018, NanoLett 2019

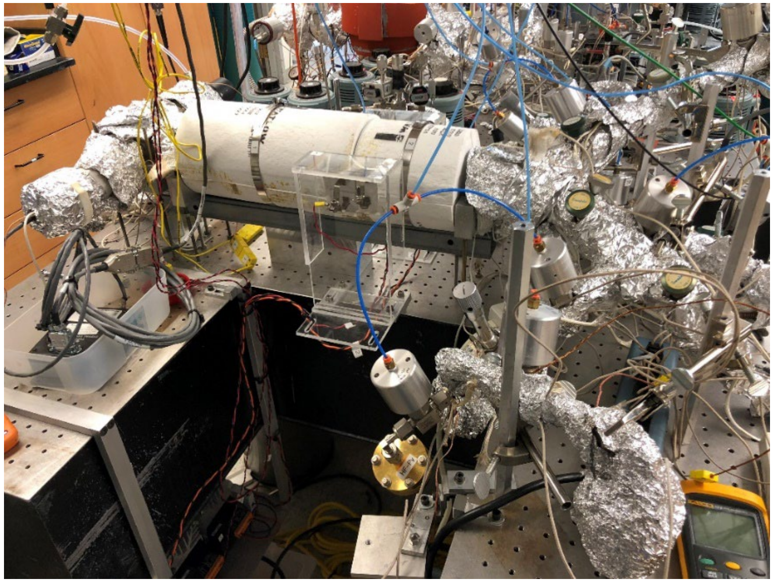
Collaboration with S. George (U. Colorado, Boulder)

# *In-situ* Thermal Atomic Layer Etching + Atomic Layer Deposition

Thermal ALE ≈ inverse of ALD

Can be done in the same reactor:



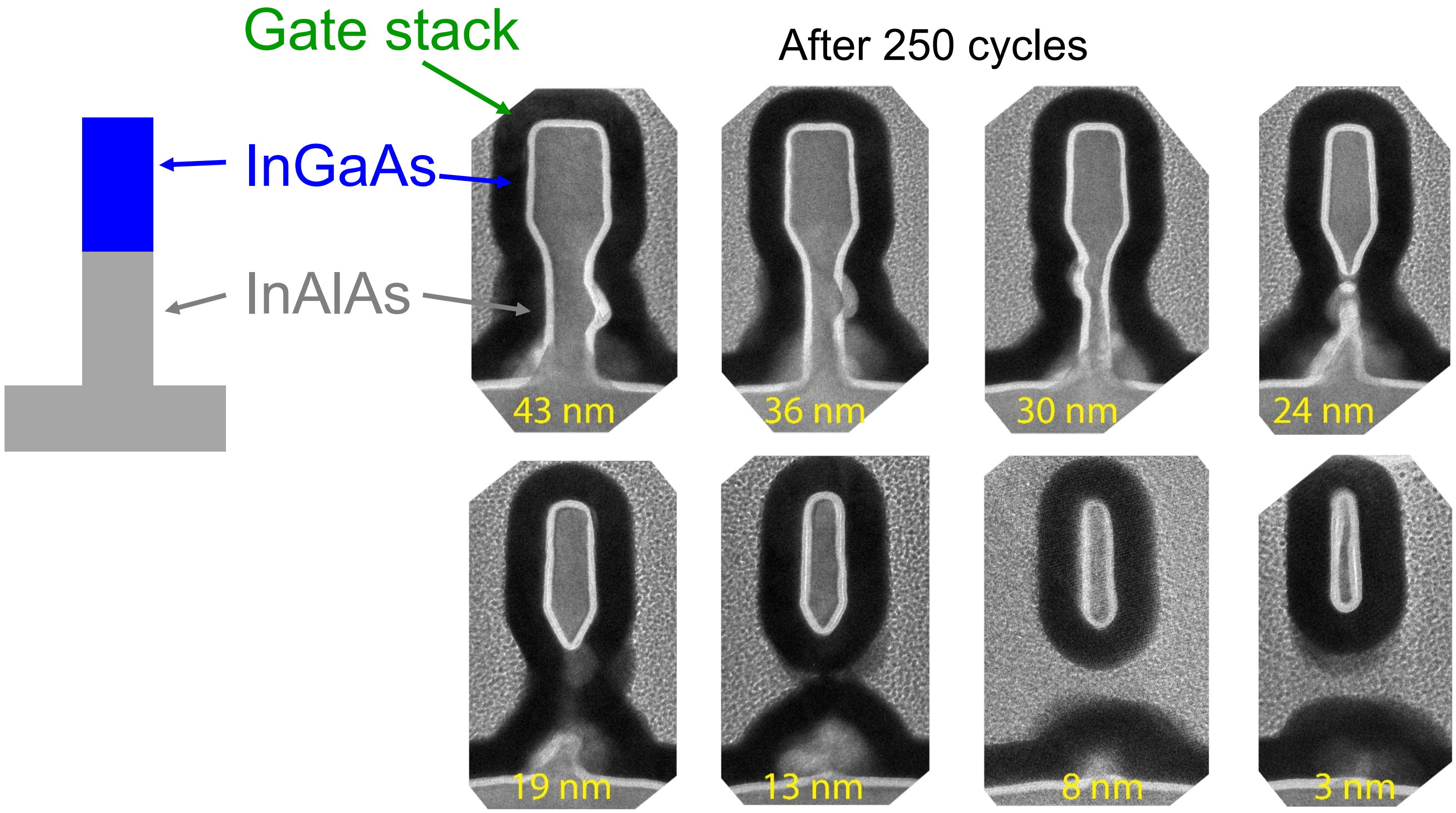


S. George (U. Colorado, Boulder)

Lu, IEDM 2018, NanoLett 2019

# Suspended InGaAs Fins by TALE+ALD

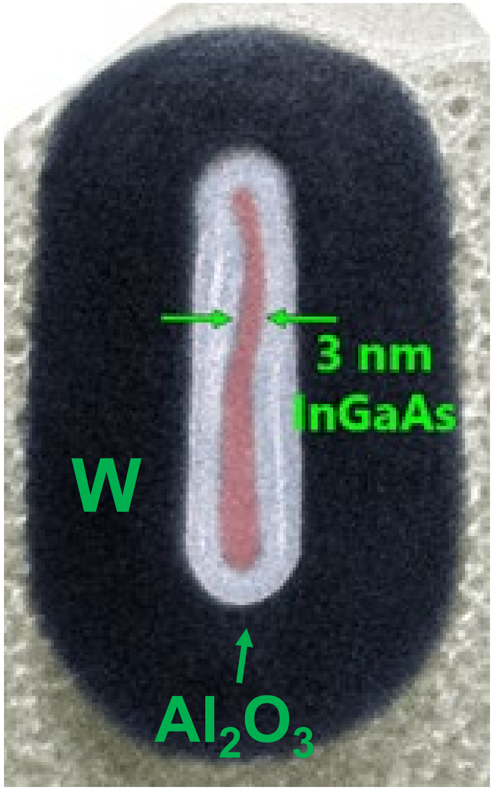
InAlAs etches faster than InGaAs → suspended fins!


After 250 cycles

Fins undercut below ~20 nm

Lu, IEDM 2018, NanoLett 2019

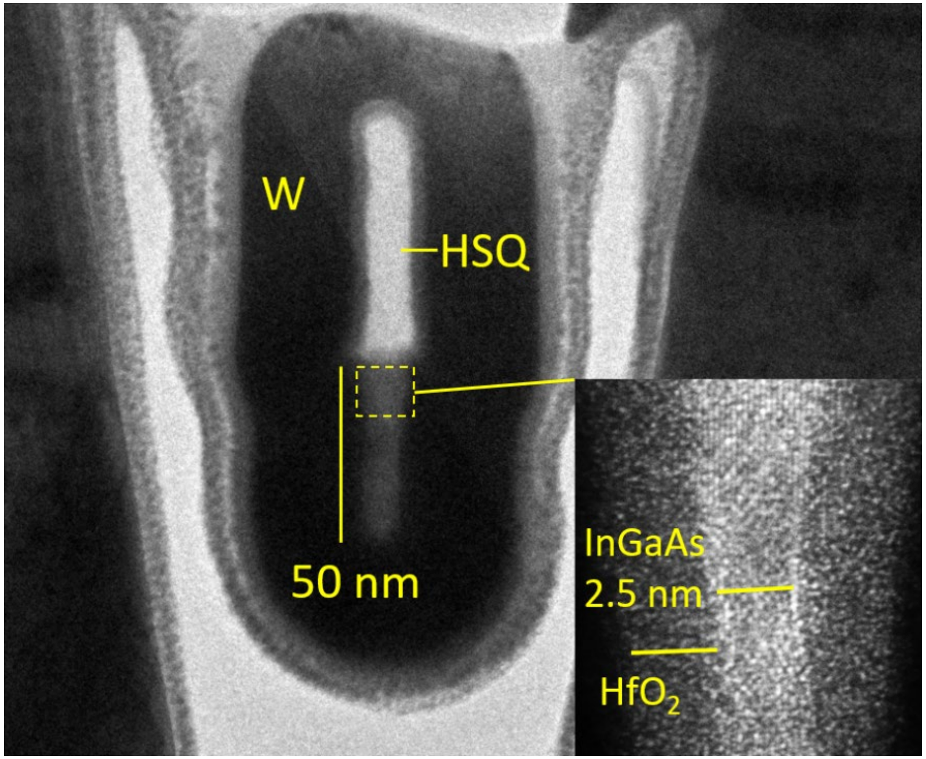
# Suspended InGaAs Fins by TALE+ALD



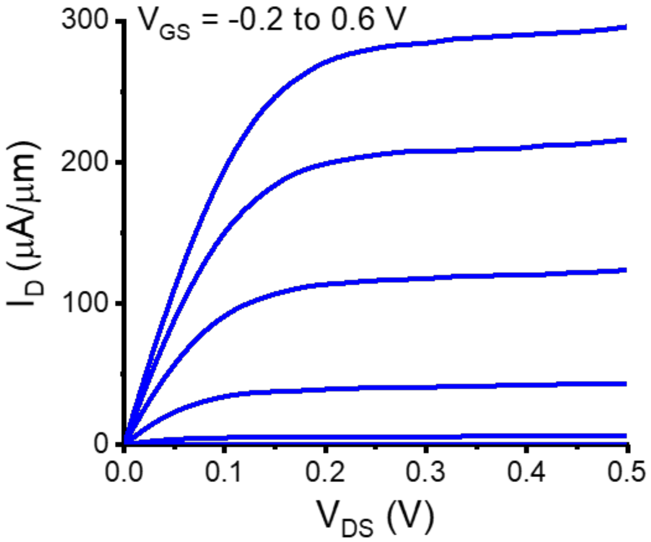
Lu, IEDM 2018,
NanoLett 2019

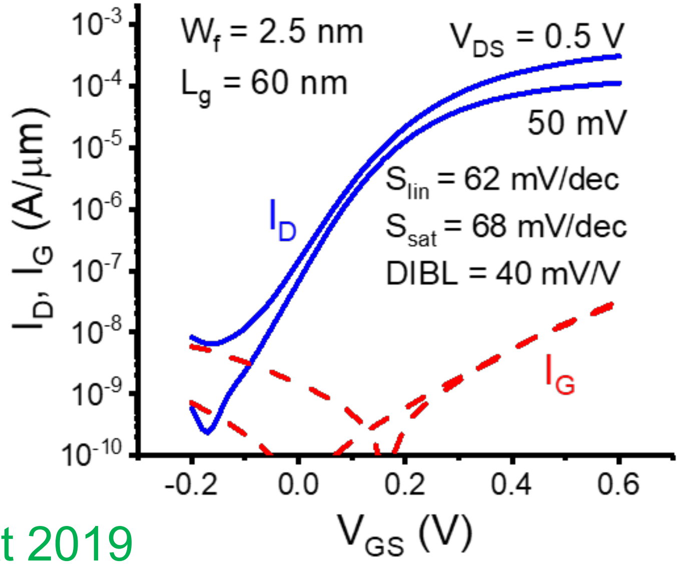
3 nm wide suspended InGaAs fin

# Suspended InGaAs FinFET with $W_f$=2.5 nm



InGaAs suspended FinFET, $W_f$=2.5 nm

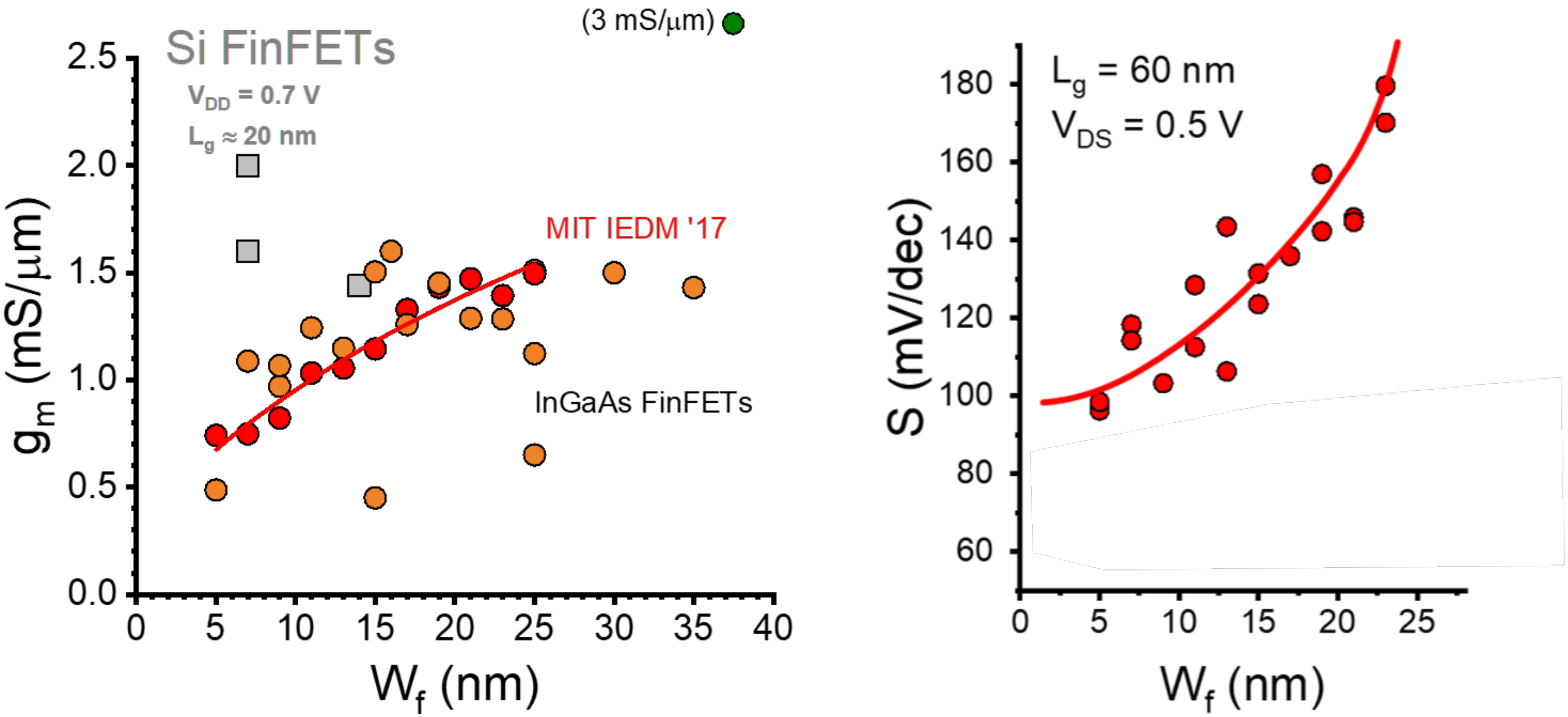




First transistor of any kind in any material system by Thermal ALE

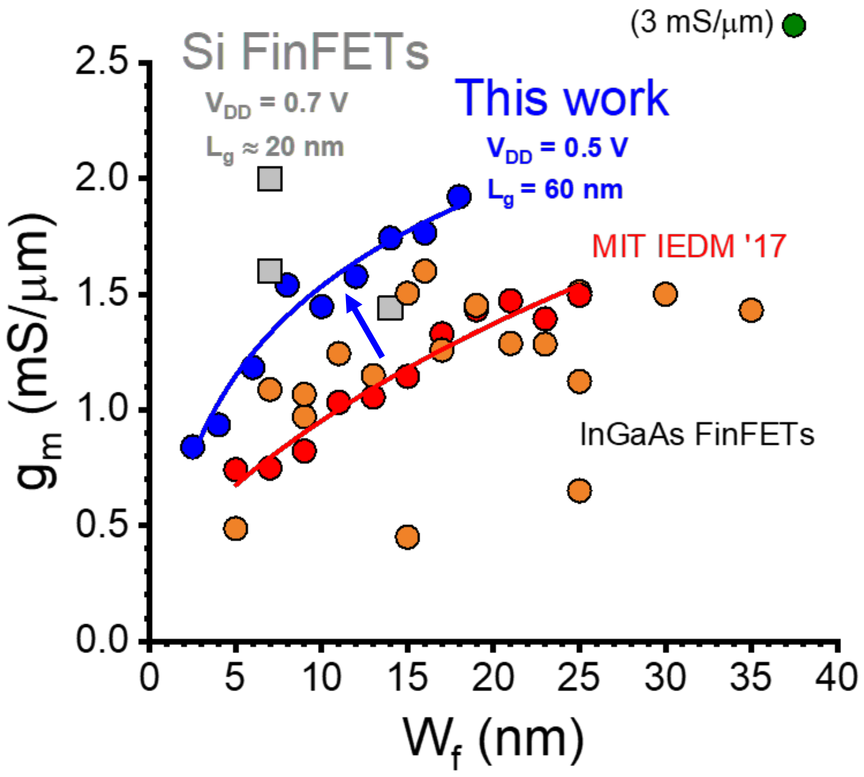
Lu, IEDM 2018, NanoLett 2019

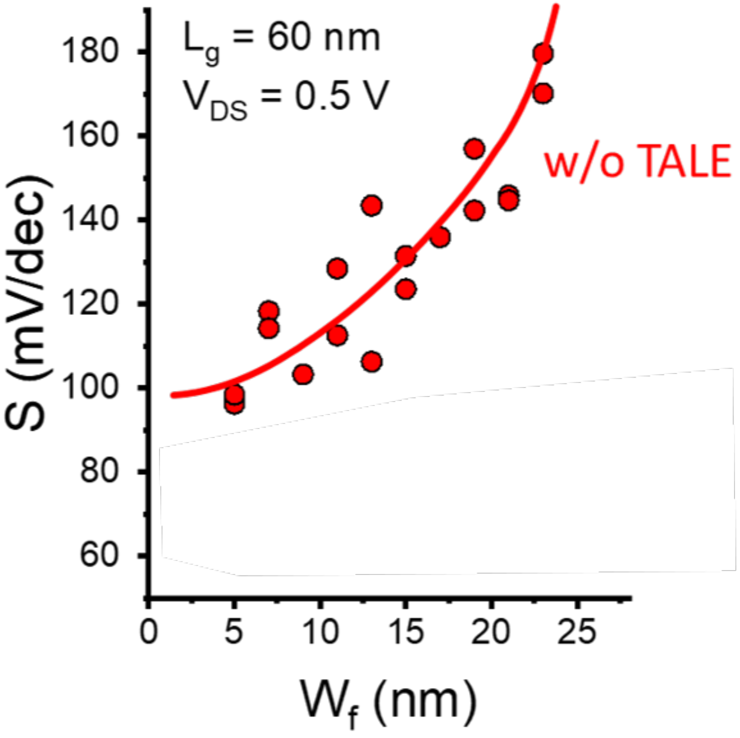
# Key benefits of *in-situ* TALE + ALD



Benchmark with FinFETs made through conventional process on same heterostructure (IEDM 2017)

# Key benefits of *in-situ* TALE + ALD

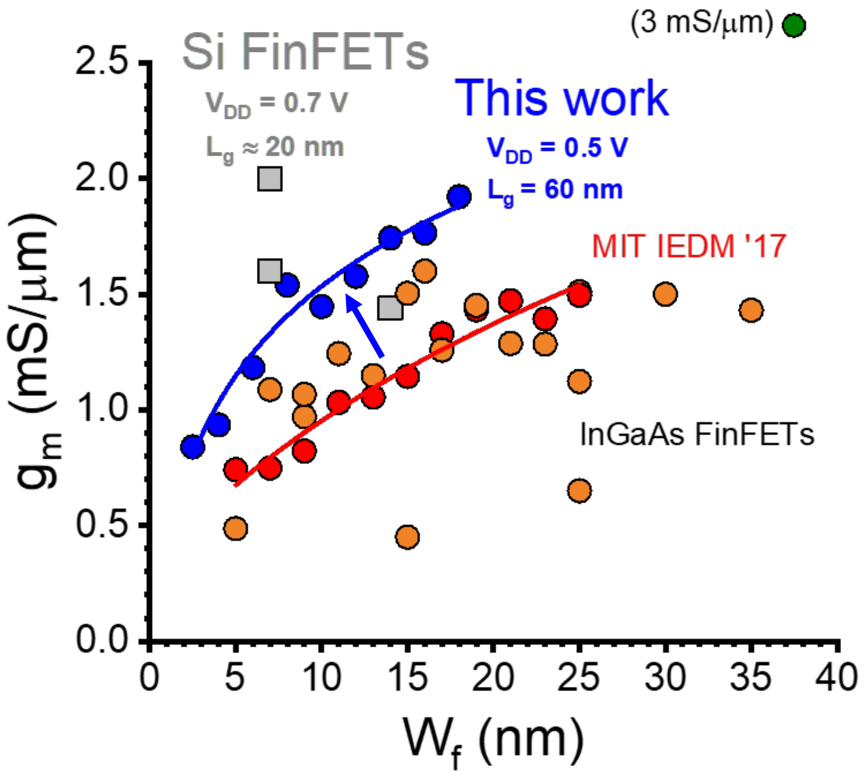


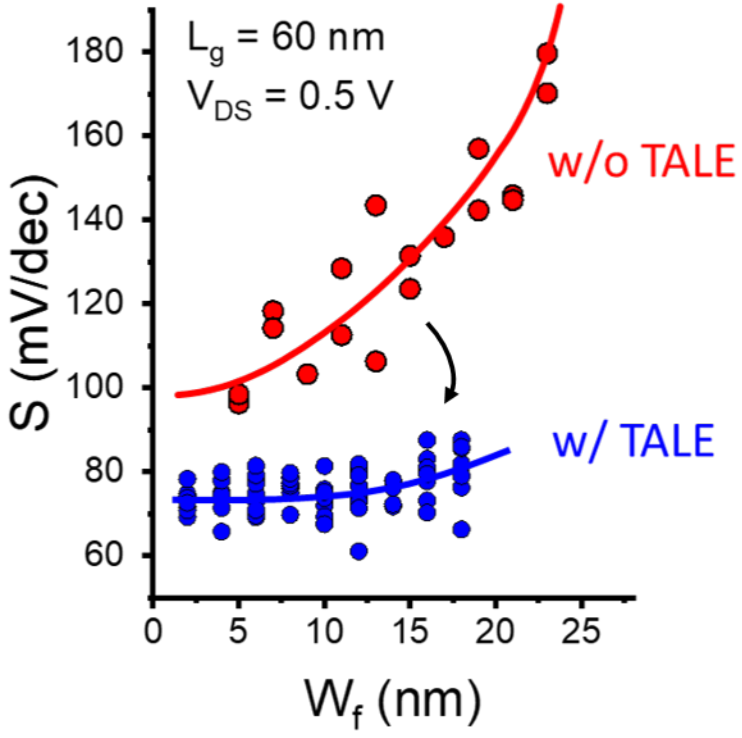


- 60% enhancement in peak transconductance
- Record among InGaAs FinFETs

Lu, IEDM 2018

# Key benefits of *in-situ* TALE + ALD



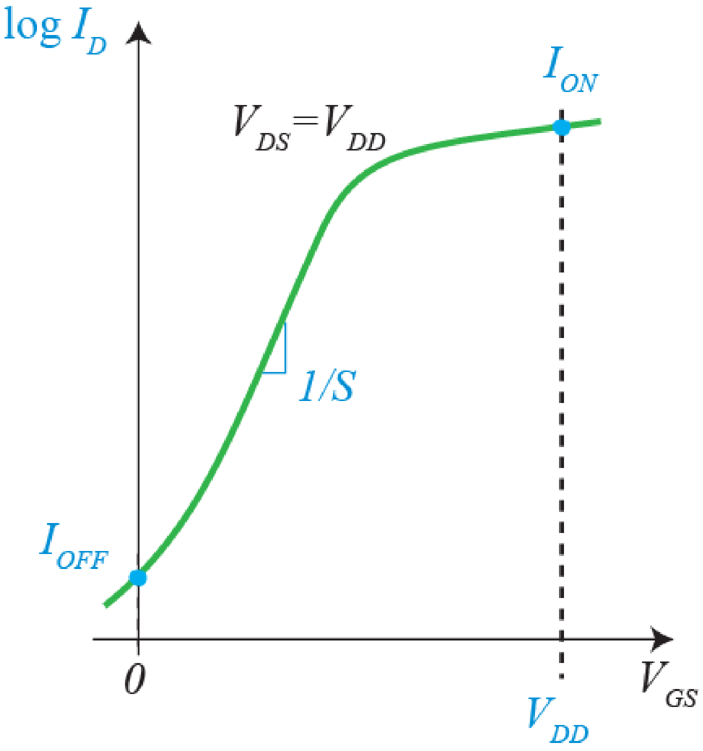


- Significant enhancement in subthreshold swing
- Nearly ideal for all $W_f$

Lu, IEDM 2018

# Many requirements for a successful logic technology

- ON current
- OFF current
- Operating voltage
- Scalability
- Stability
- Manufacturing robustness
- CMOS
- Si compatibility
- …

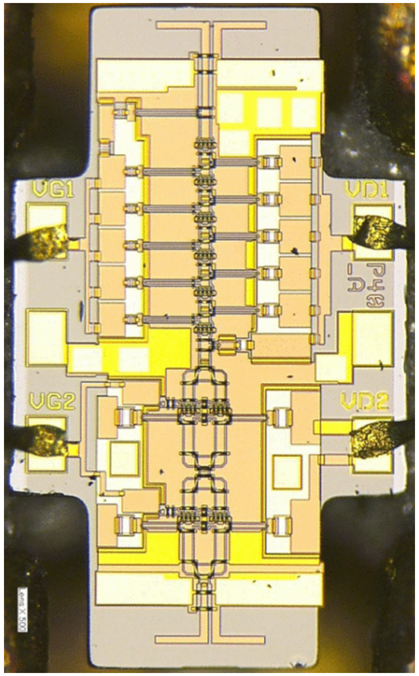


III-V MOSFETs: not worth the trouble for logic

# Going forward

# InGaAs promising for THz, high-speed logic and ultra-low noise applications

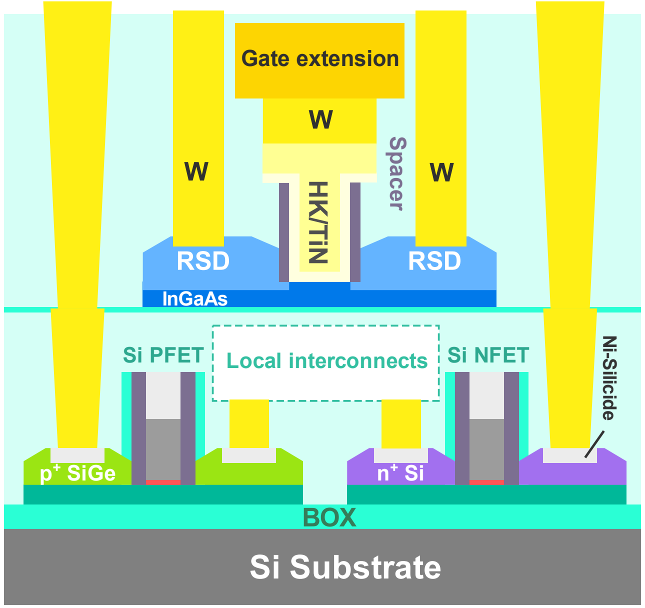
## THz systems



650 GHz PA
(Northrop Grumman)

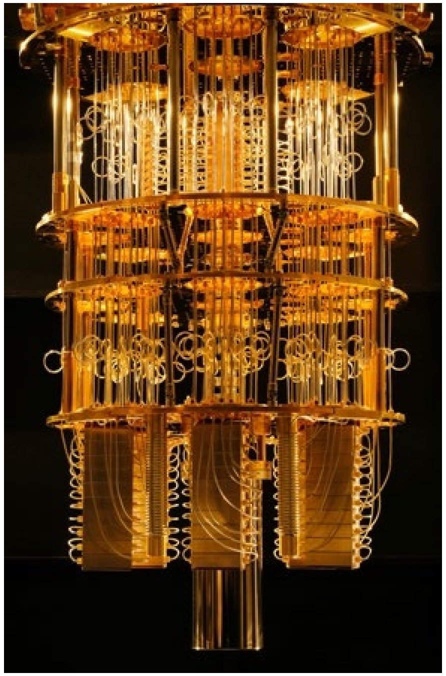
Radisic, TMTT 2012

## Integration with CMOS



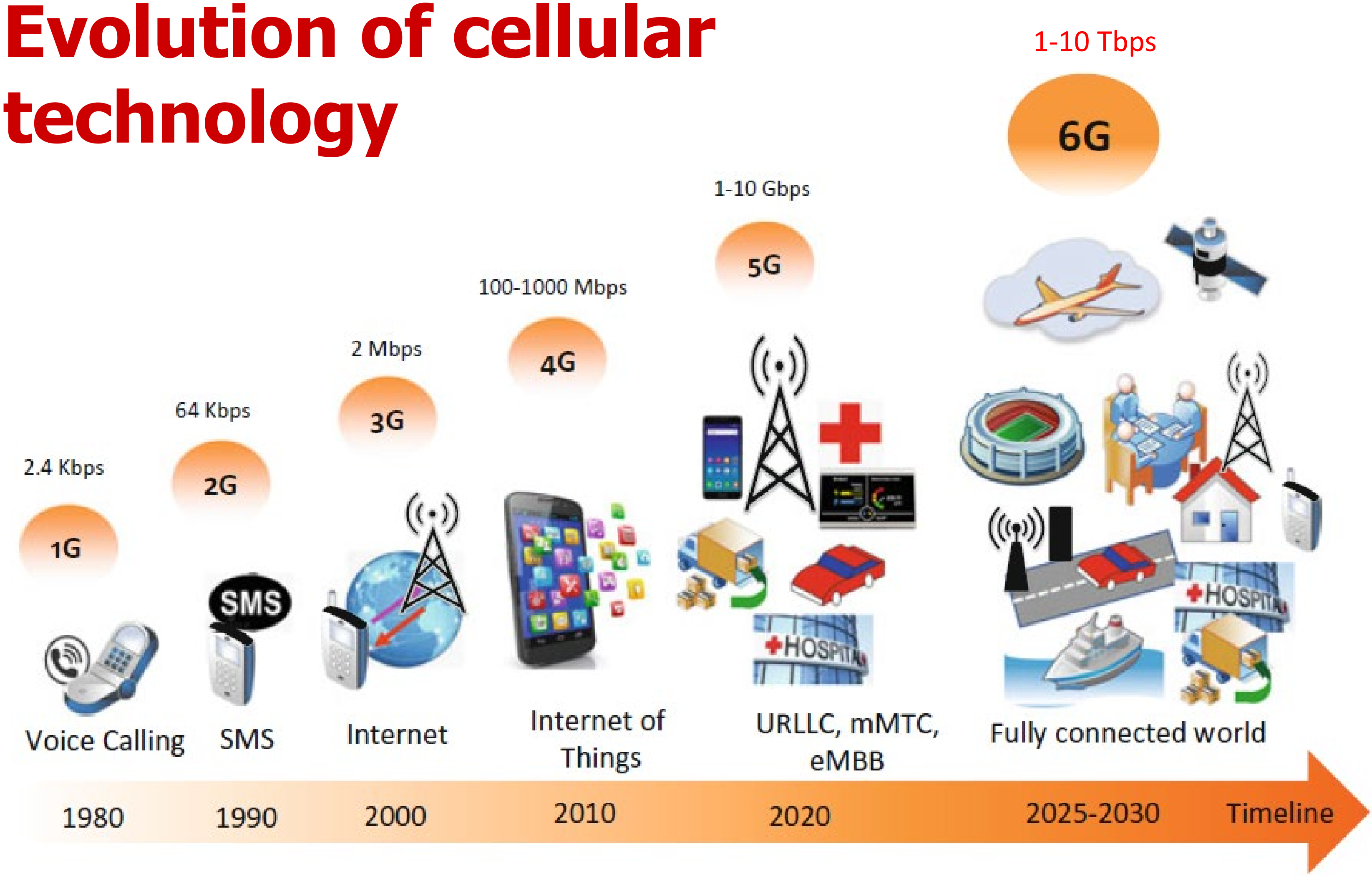
Zota, IEDM 2019

## Quantum computing



https://www.ibm.com/blogs/research/wp-content/uploads/2018/03/IBM-quantum-computer_small.jpg

# Evolution of cellular technology

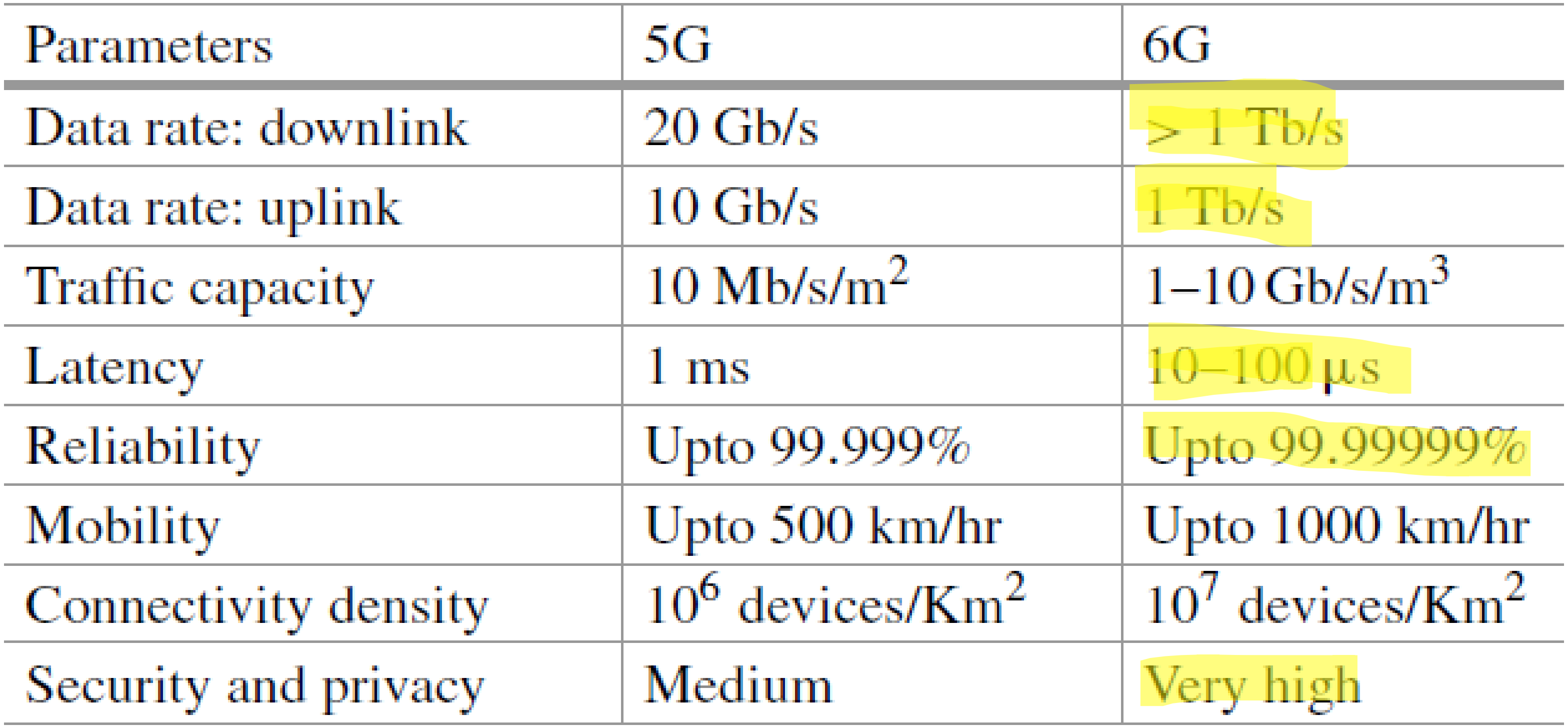


5G → 6G:

from “connected things” to “connected intelligence”

“6G Mobile Networks”, Wu et al. eds, Springer 2021

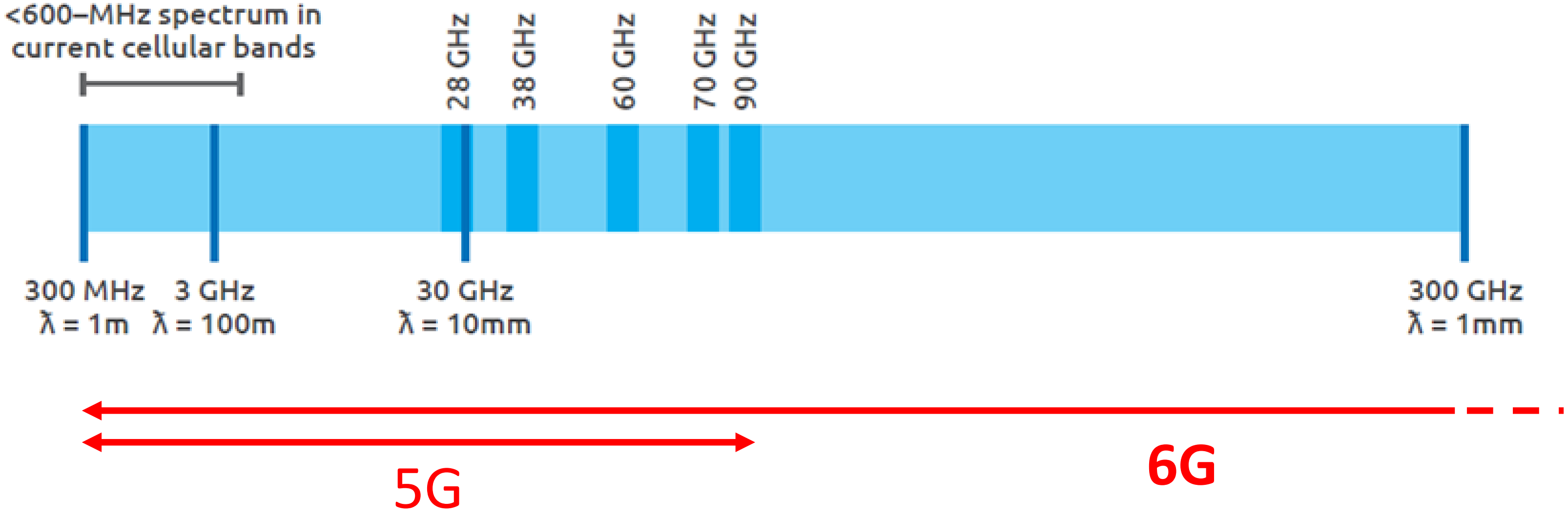
# 5G vs. 6G KPIs



| Parameters | 5G | 6G |
|---|---|---|
| Data rate: downlink | 20 Gb/s | > 1 Tb/s |
| Data rate: uplink | 10 Gb/s | 1 Tb/s |
| Traffic capacity | 10 Mb/s/m$^2$ | 1–10 Gb/s/m$^3$ |
| Latency | 1 ms | 10–100 μs |
| Reliability | Upto 99.999% | Upto 99.99999% |
| Mobility | Upto 500 km/hr | Upto 1000 km/hr |
| Connectivity density | $10^6$ devices/Km$^2$ | $10^7$ devices/Km$^2$ |
| Security and privacy | Medium | Very high |

“6G Mobile Networks”, Wu et al. eds, Springer 2021

# 5G vs. 6G Frequency Bands

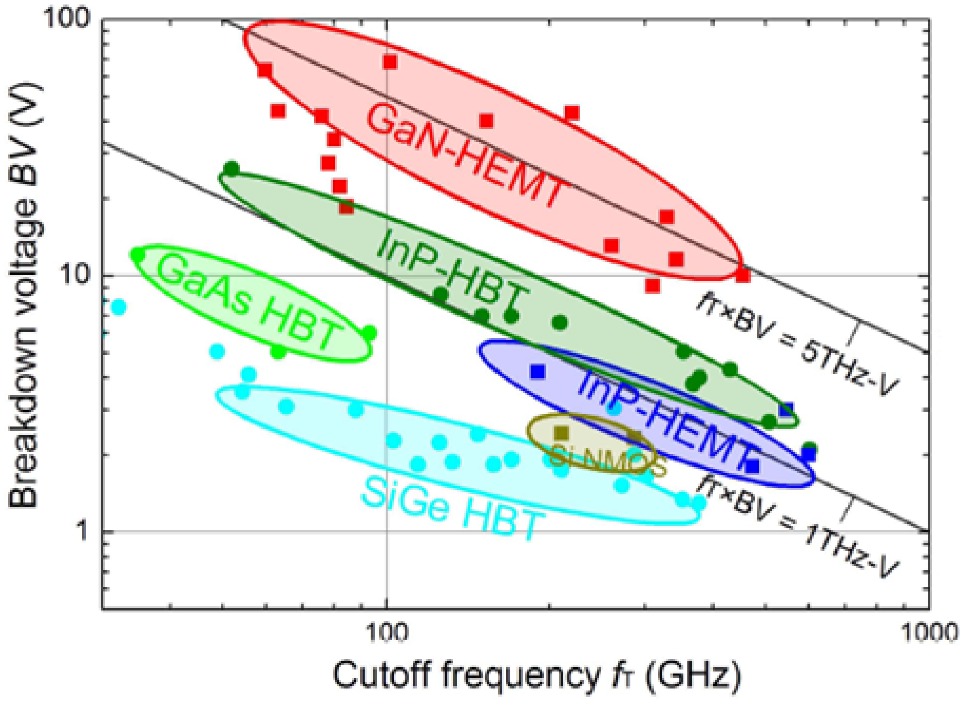


For 6G: need technologies at f >100 GHz

SRC Decadal Plan for Semiconductors 2021

# Semiconductors for mm-wave transistors

Fundamental breakdown voltage-$f_T$ trade-off:



- GaN best for power
- InGaAs (InP) best for high frequency

Shinohara, TED 2013

# From Failure to Success to…?

- GaAs MESFET ✗ for logic
  - → GaAs MESFET microwave systems
  - → GaAs, InGaAs HEMT

- InGaAs HEMT ✗ for logic
  - → InGaAs HEMT for communications, sensing, science
  - → Heterojunction engineering and science
  - → InGaAs MOSFET

- InGaAs MOSFET ✗ for logic
  - → unpinned III-V surface by ALD
  - → in-situ TALE + ALD
  - → nanoscale 3D etching technology of III-Vs
  - → Quantum computing and 6G communications systems?

# Epilogue:

# Kroemer’s Lemma of New Technology

*“The principal applications of any sufficiently new and innovative technology have always been – and will continue to be – applications created by that technology.”*

Kroemer, Rev Mod Phys 2000