In-Line Metrology Challenges for Nanosheet Gate-All-Around Manufacturing

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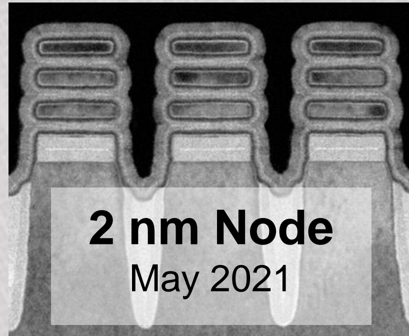
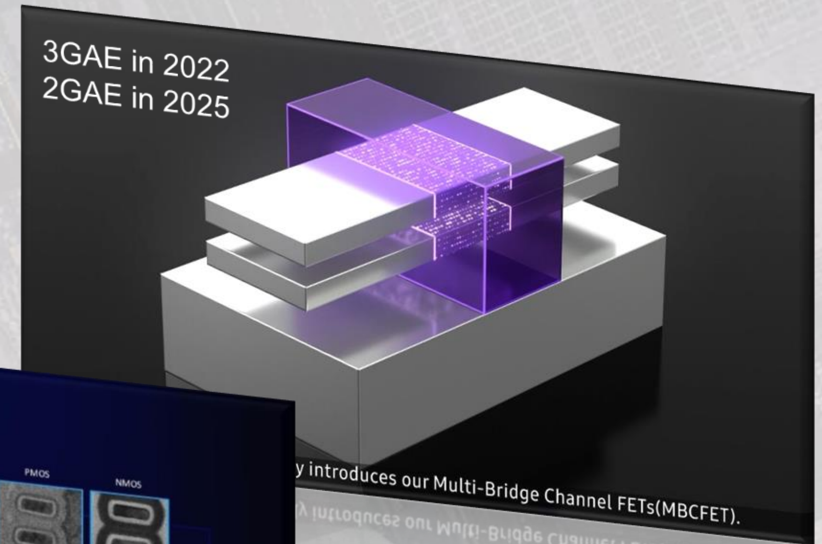
SRC NMP Review – August 4, 2022

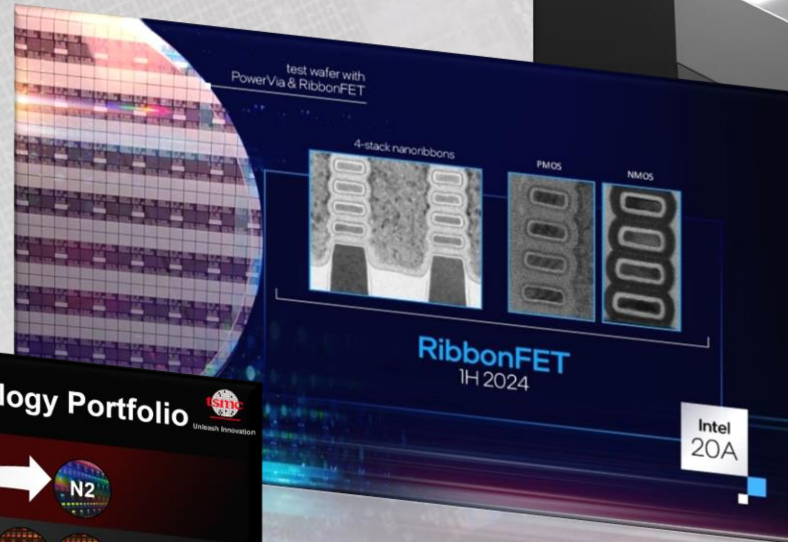
Gate-All-Around Nanosheet FETs

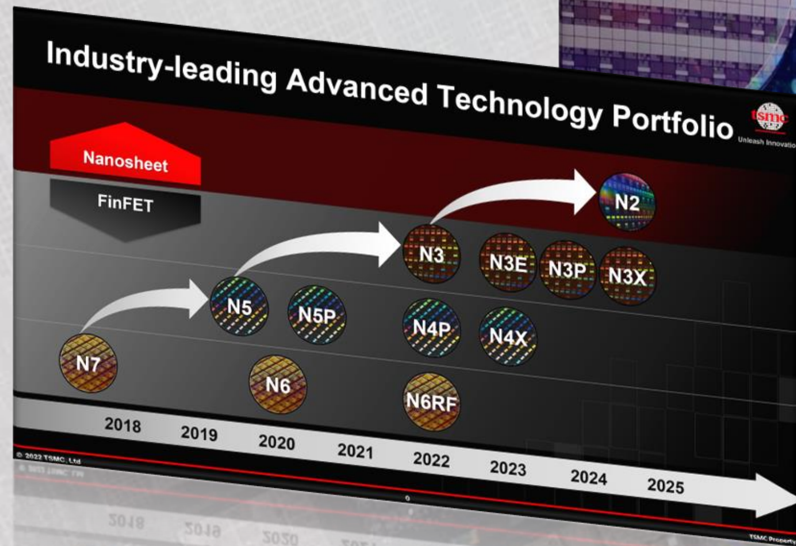
IBM Research Albany



https://research.ibm.com/blog/2-nm-chip







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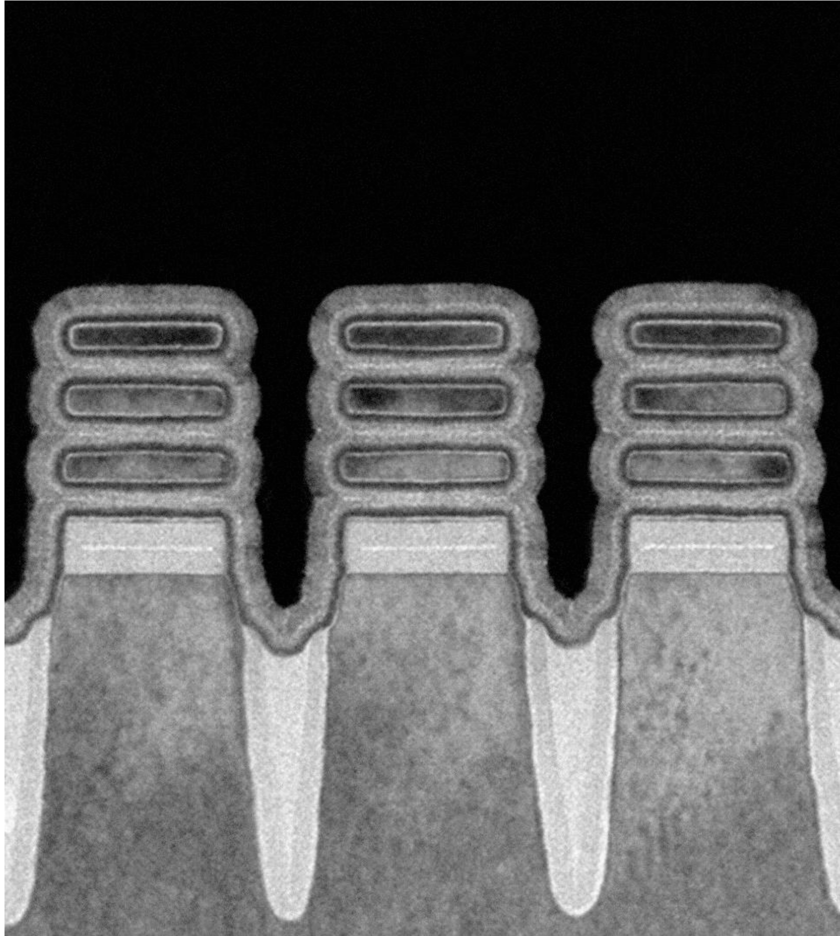
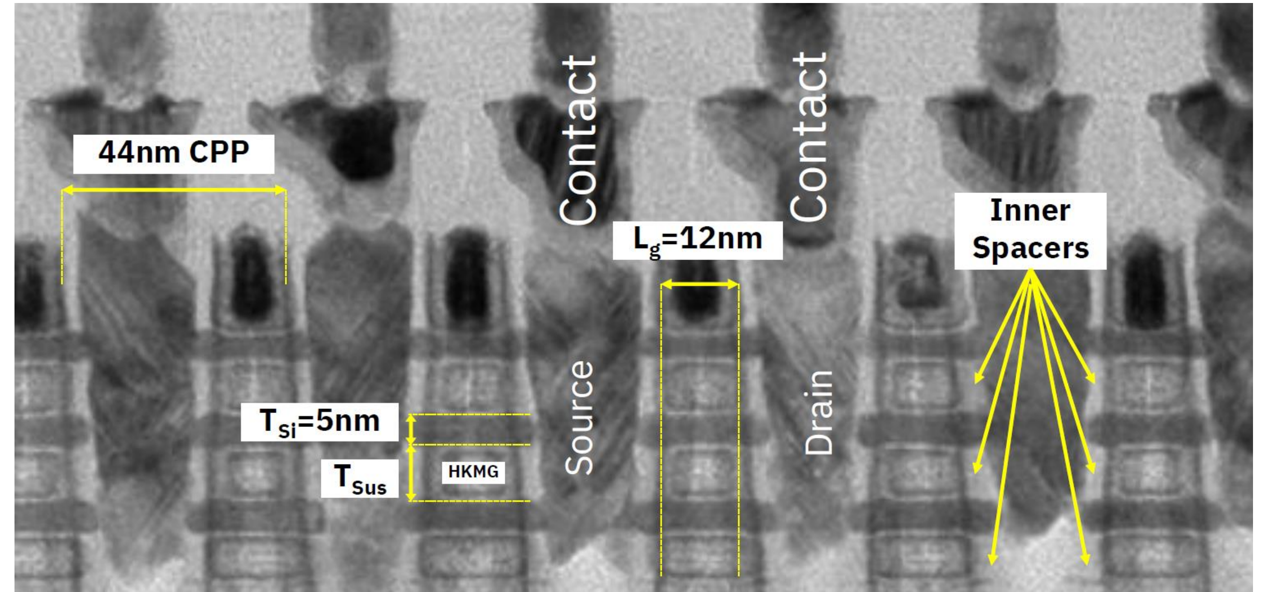
2 nm node – a closer look

Looking into the channel



Looking along the channel



Metrology is key for device performance

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Importance of SRC, and beyond

Collaboration → Connections → Opportunities

Successfully submitted a proposal to the MIT-IBM Watson AI Lab together with MIT Professor Rafael Jaramillo

"*Application of deep learning to expand the use of spectroscopic ellipsometry for semiconductor device manufacturing*"

→ exploring machine learning for ellipsometry to improve sheet-specific nanosheet multilayer stack characterization

→ sample exchange

→ exposure to immediate metrology needs

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Not The Outline

- Overlay Metrology
  - ➢ Pattern to pattern alignment
- Critical Dimension Scanning Electron Microscopy (CDSEM)
  - ➢ Top down, lateral dimensions and edge roughness
- Defect Inspection
  - ➢ Finding and classifying defects

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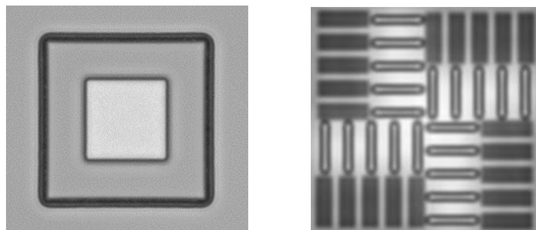
Monitoring Patterning Process

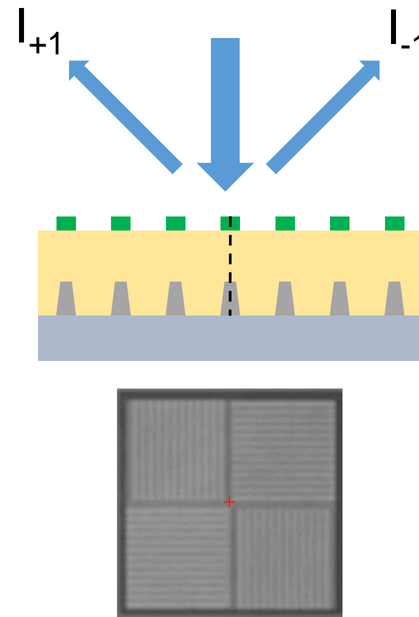
Overlay

Measuring lithographic image placement with respect to prior patterning
→ top (current) layer is patterned resist

Image-based

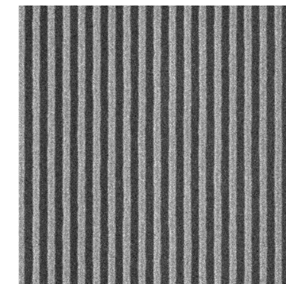


Diffraction-based



CDSEM

Automated SEM measurements with primary electron beam energies as low as 1 keV
→ monitor litho (dose, focus) and etch



CD
LER
LWR
LCDU

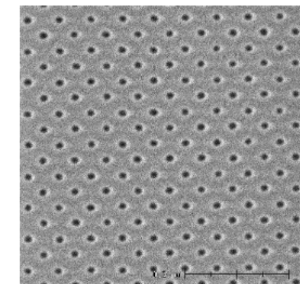
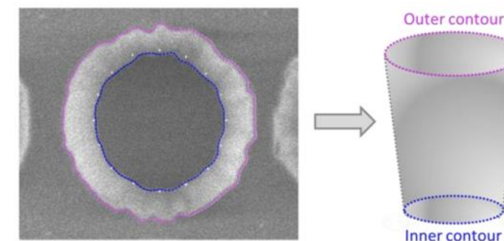
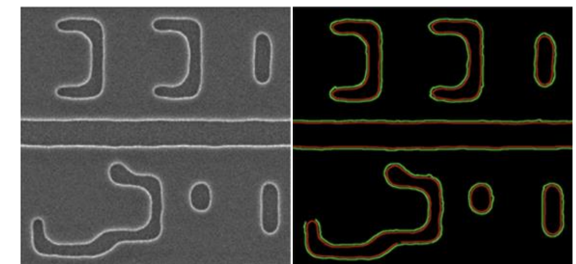


image analysis is a key component



Gratiet et al. SPIE 11611 (2021).



Zhou et al. SPIE 11611 (2021).

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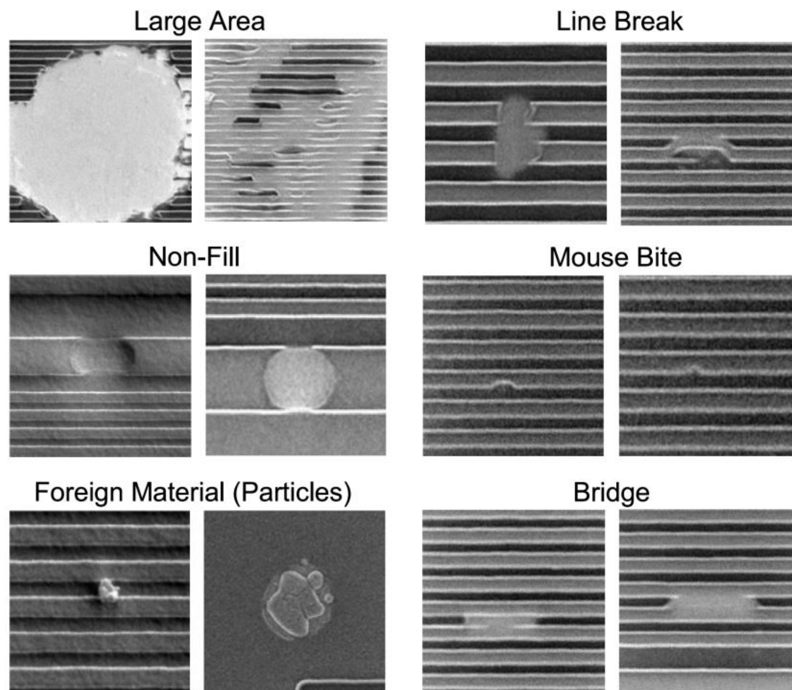
Defect Inspection

Optical or e-beam defect inspection for yield improvements; sensitivity or throughput limited

Find and classify defect, trace origin, improve processes and hence yield

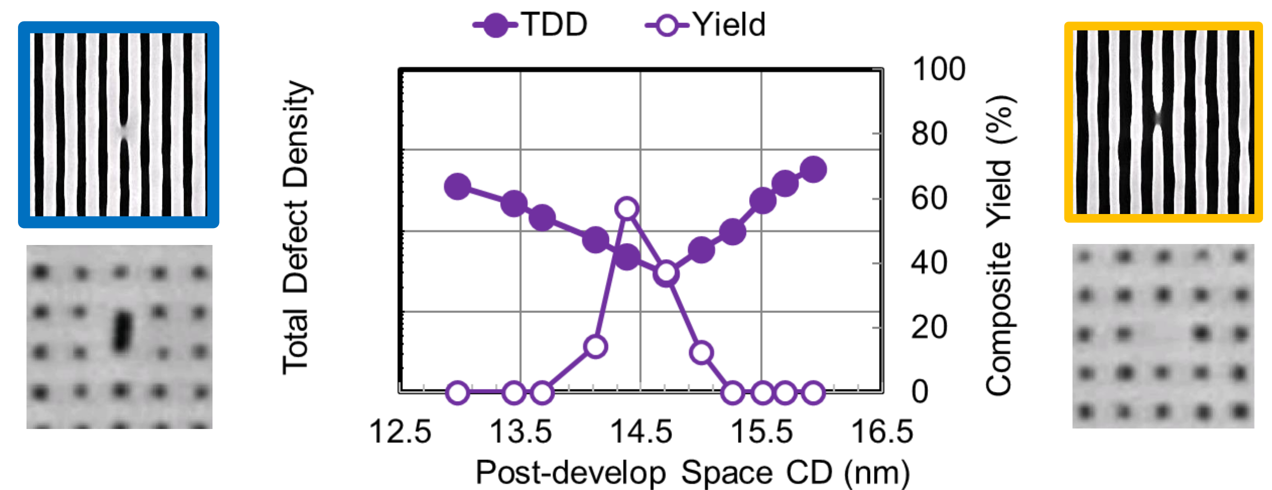


M. Malloy et al. Proc. SPIE 7970, 797006 (2011).

EUV Lithography comes along with stochastic defects

- random line breaks or bridge defect
- random merged or missing contact holes

→ process optimization more complex than in the past
→ Large area scans required to characterize defect density



L. Meli et al. Proc. SPIE 11147, 1114718 (2019).

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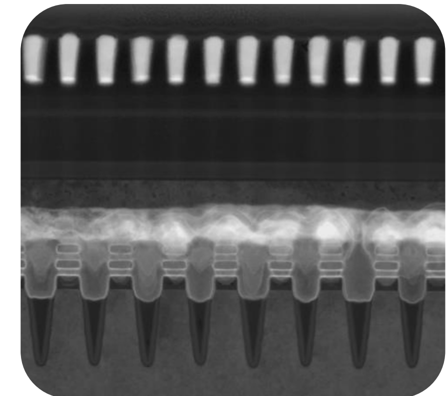
Outline

- Inline Metrology Techniques and Requirements
- Introduction to Nanosheet Manufacturing
- Modules with Key Metrology Steps
  - ➢ NS Stack
  - ➢ Inner Spacer
  - ➢ Channel Release
  - ➢ Gate Stack
  - ➢ BEOL
- Beyond Nanosheets
- Summary and Conclusions



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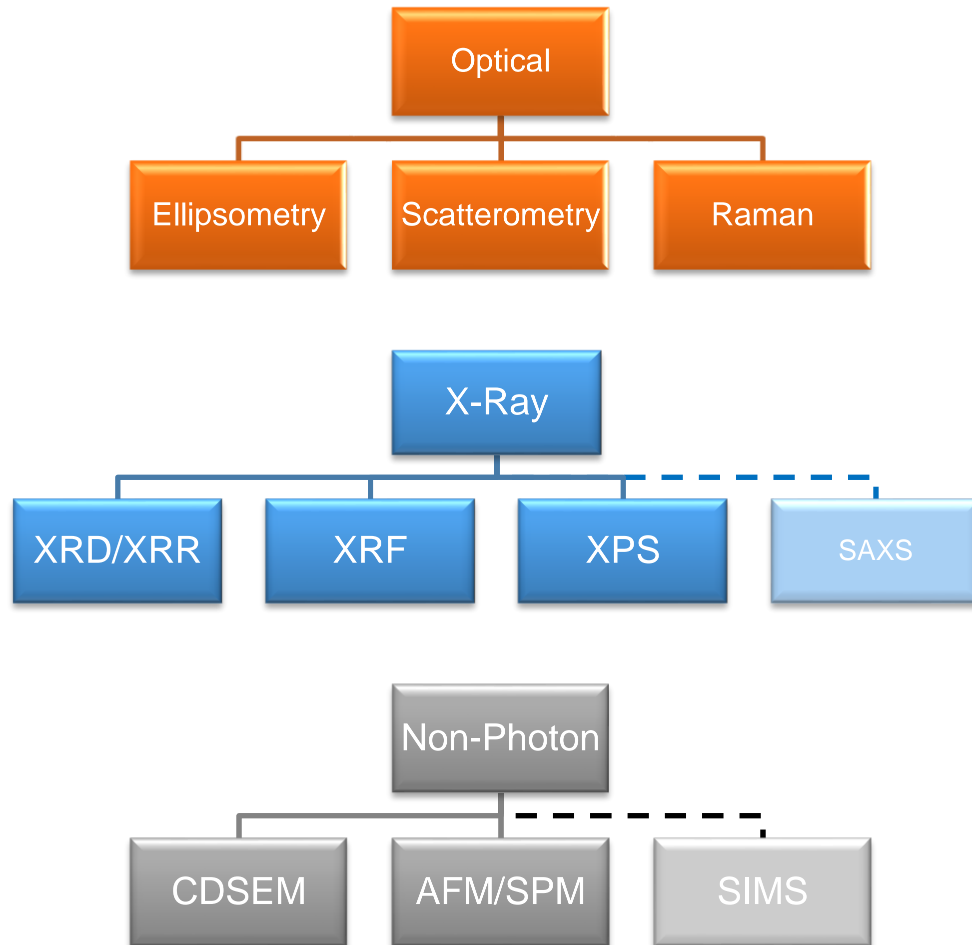
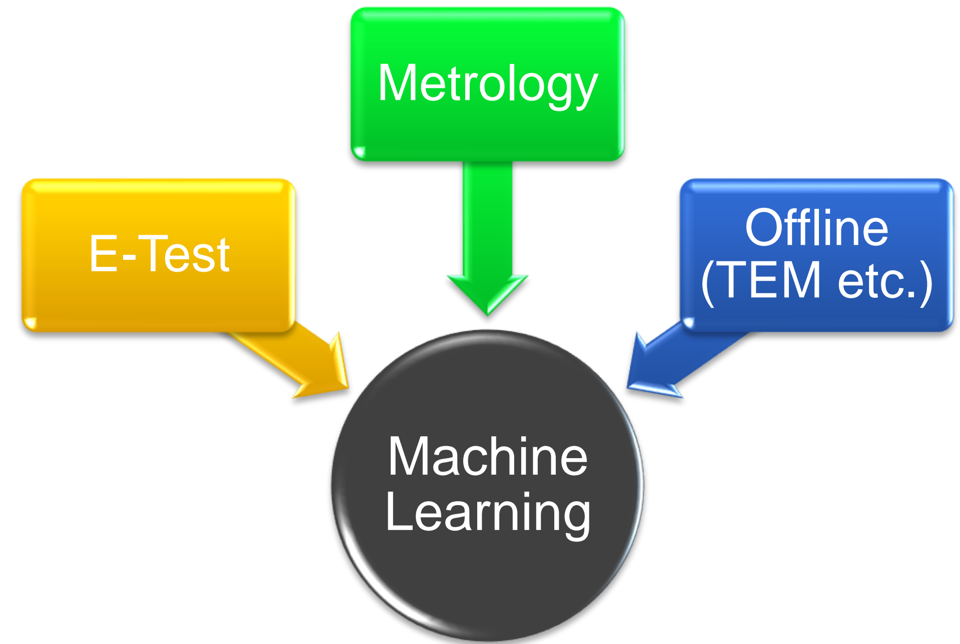
Typical In-Line Metrology Techniques





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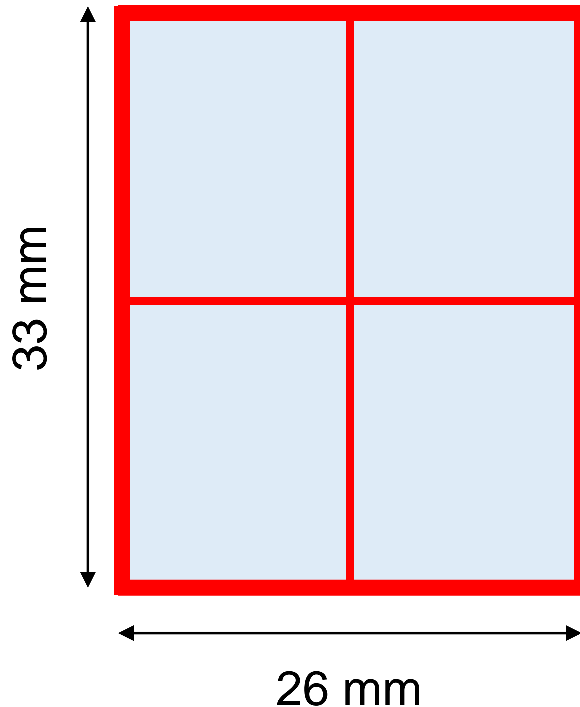
In-line Metrology Requirements



maximum exposure
field size on wafer

Real estate within the exposure field is very expensive

→ scribe lines (dicing streets) may be on the order of 50 to 100 µm and need to fit all essential metrology targets such as:

- Alignment and overlay marks
- Blanket targets (e.g. Ellipsometry)
- Patterned targets (e.g. Scatterometry)
- Others

→ smallest targets are desired (design rule clean, device-like): allows for more targets to be added or more room for chip area

→ in-die metrology desired where possible: no target area required, "measure where it matters"

"Time is Money"

→ Fast MAM and cycle times required ("minutes per wafer")

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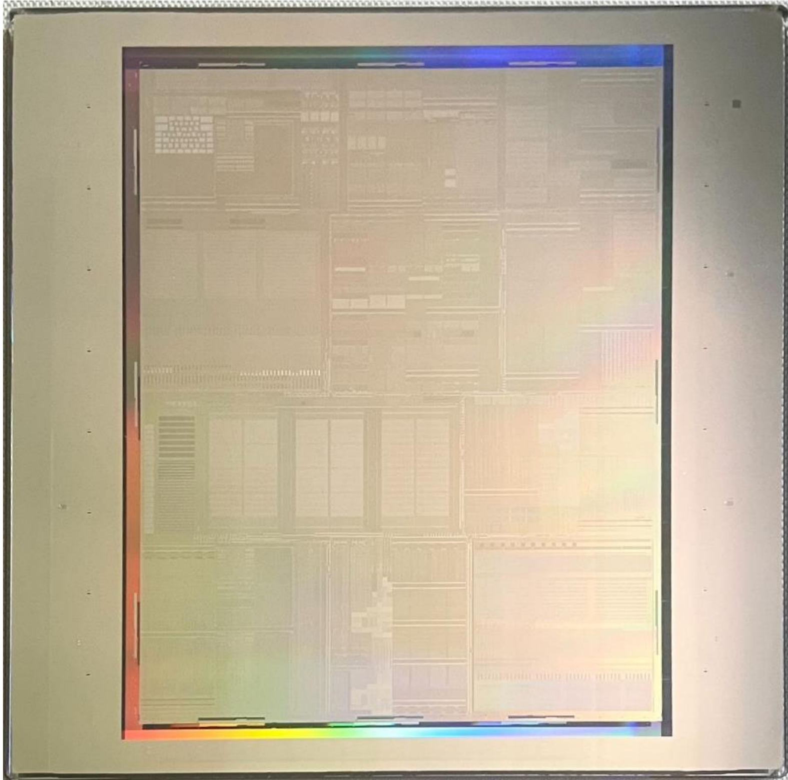
In-line Metrology Requirements



EUV Mask
152 x 152 mm^2 (6 x 6 in^2)

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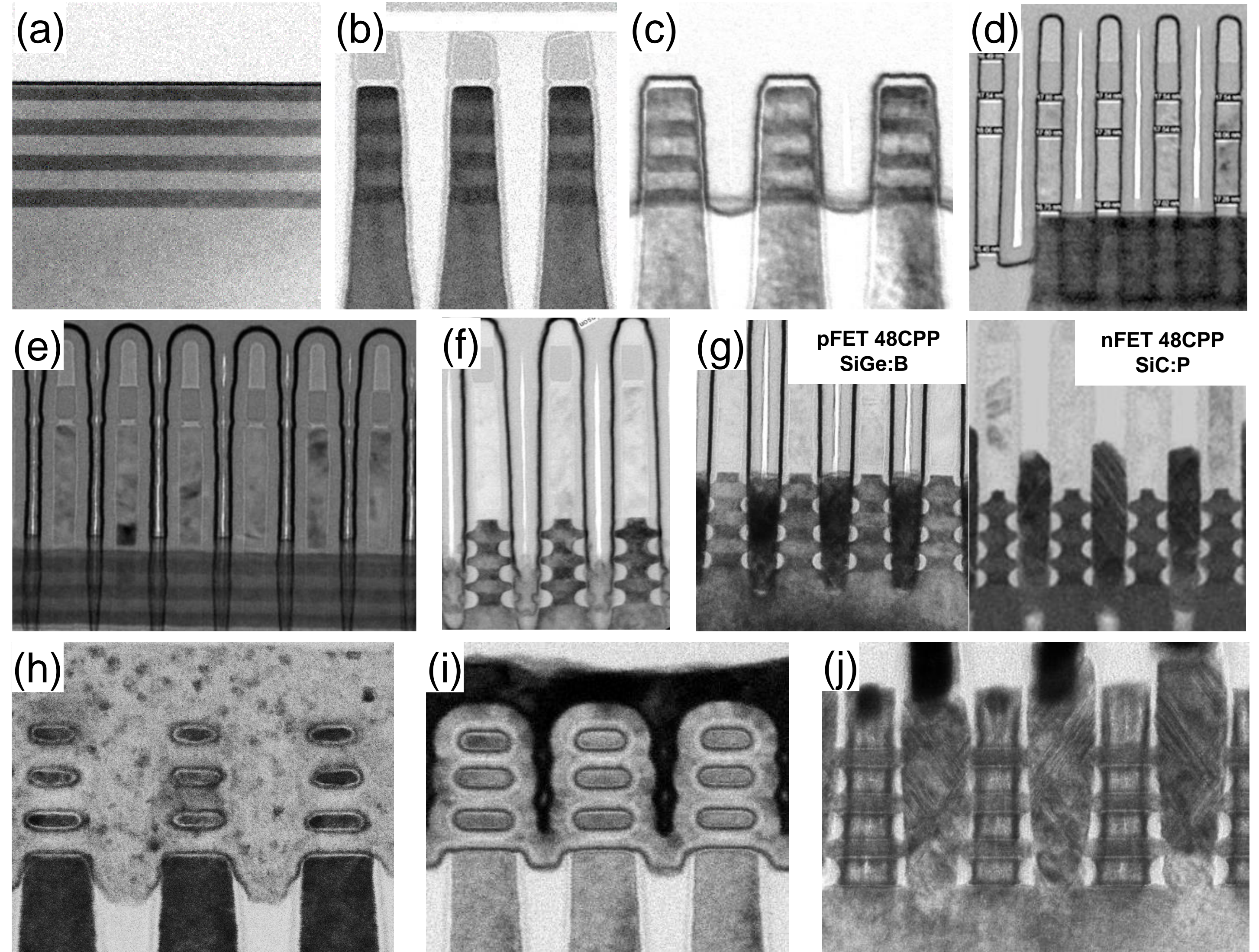
GAA Nanosheet Manufacturing

- Si/SiGe Multilayer Stack (a)
- NS “Fin” Formation (b)
- NS “Fin” Reveal (c)
- Dummy Gate Patterning (d)
- Gate Spacer Deposition (e)
- Fin Recess & Inner Spacer (f)
- Dual S/D Epitaxy (g)
- Channel Release (h)
- Gate-All-Around & Multi-Vt (i)
- MOL/BEOL (j)



N. Loubet et al., VLSI (2017)

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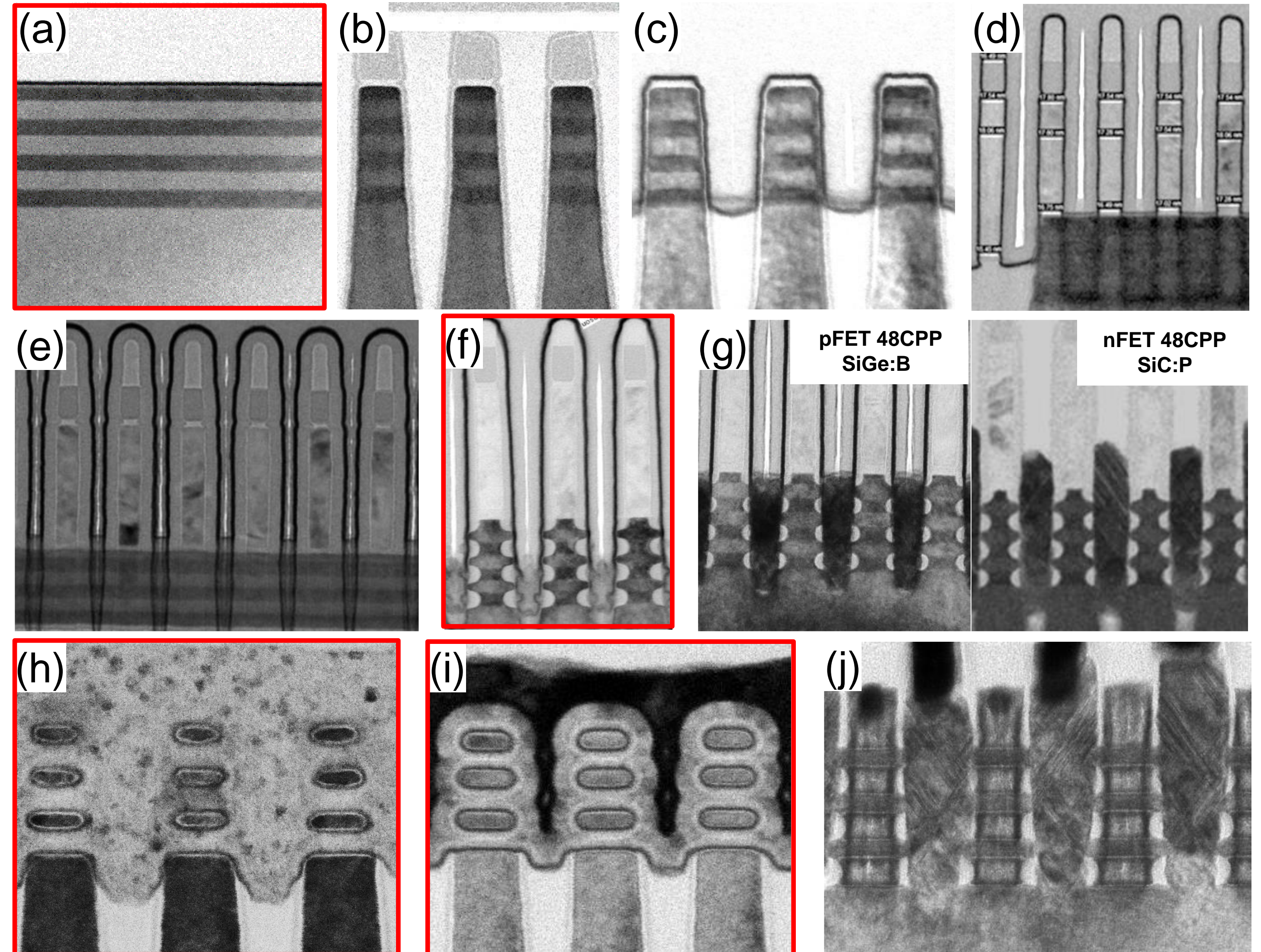

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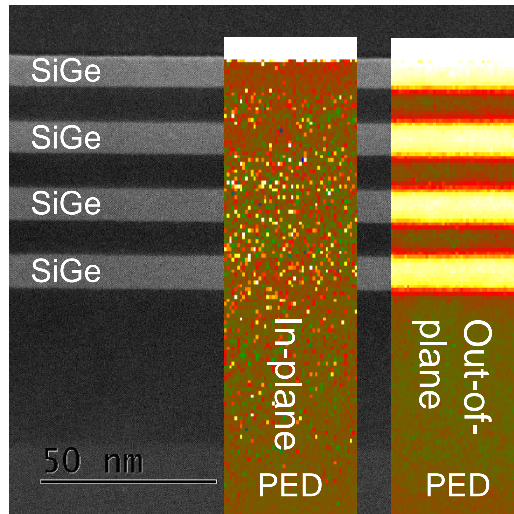
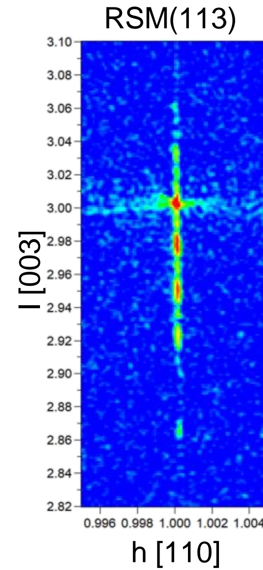
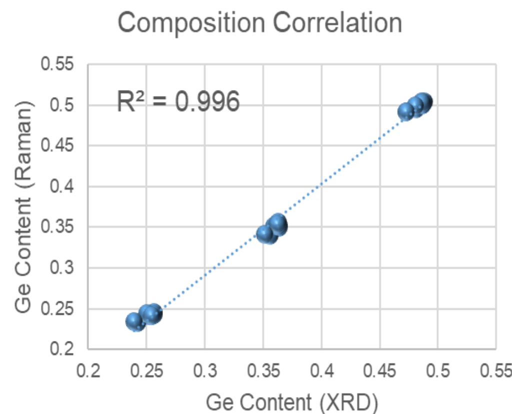
N. Loubet et al., VLSI (2017)

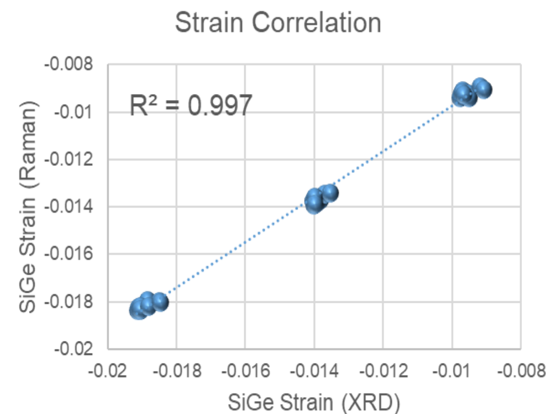
Nanosheet Stack Epitaxy



Li et al. Microsc. Microanal. **25** (2019).







Schmidt et al., SPIE (2021); JM3 (2022).

Multilayer stack determines device performance

- Si layers determine channel thickness and quality
- SiGe layers govern inner spacer, strain, and gate

Parameter of interest

- ✓ Individual sheet thicknesses of all layers
- ✓ Individual Ge concentration
- ✓ Crystal quality (dislocations)
- ✓ Interface quality

Metrology Techniques

- XRR and XRD
- Ellipsometry
- Raman
- PL
- SIMS
- Defect Etch
- TEM, PED

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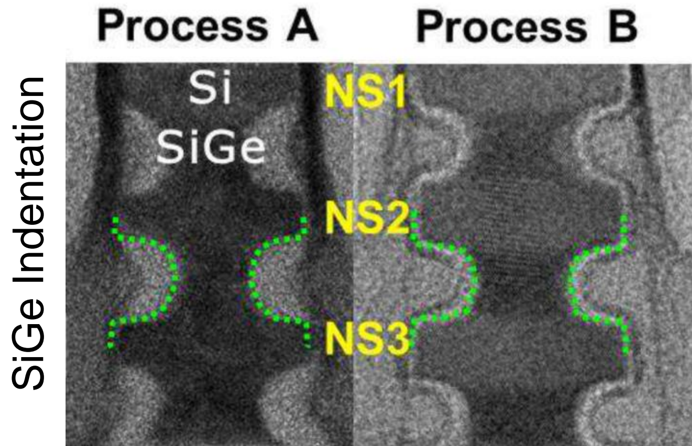
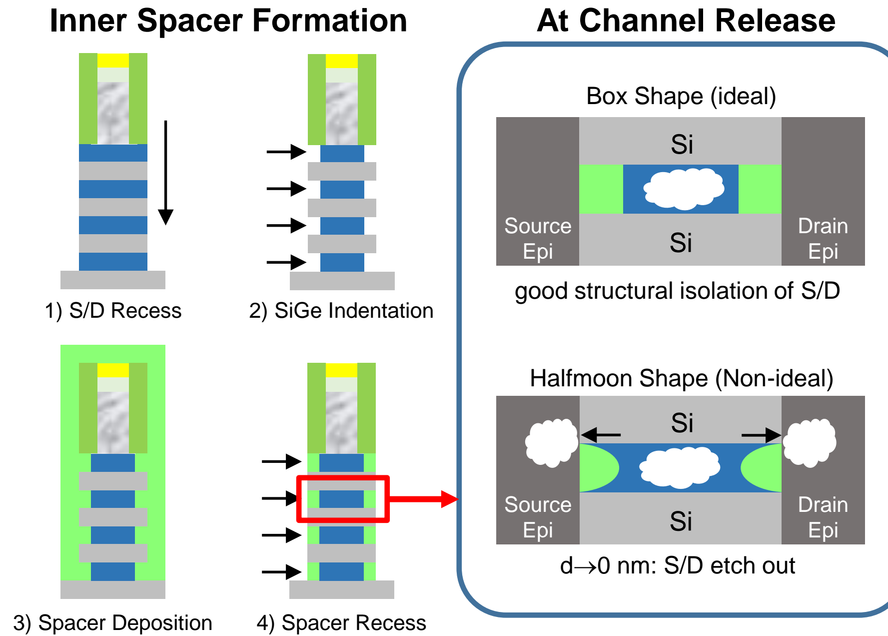
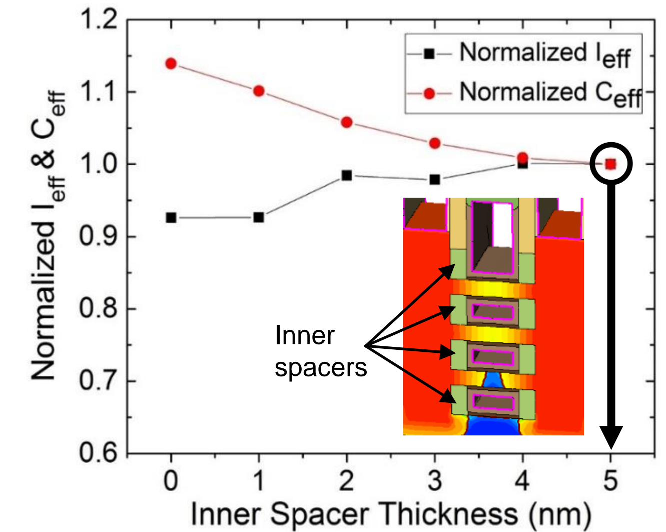
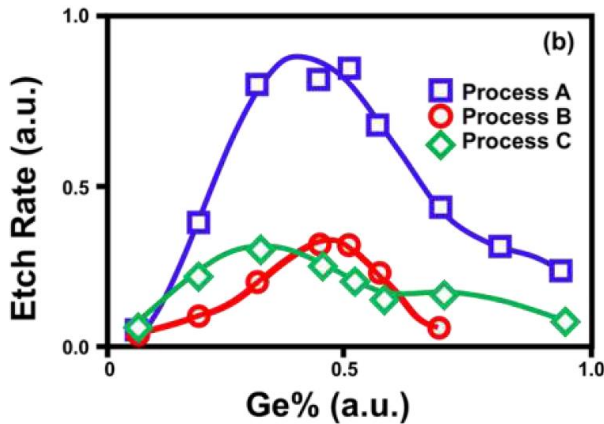
Inner Spacer Module



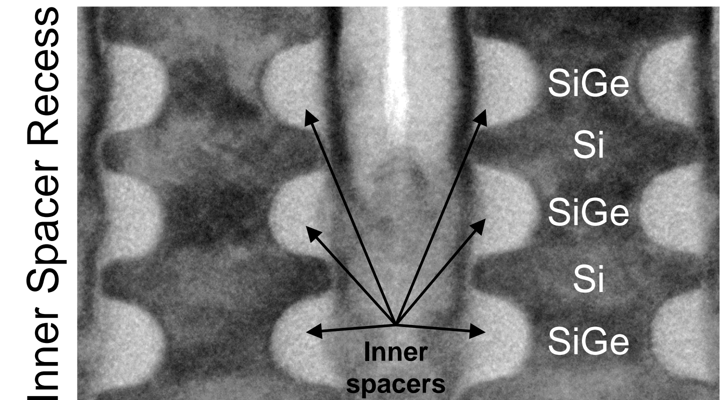






Durfee et al. ECS Trans. 104, 217 (2021).

- Etch rate (indent depth) depends on Ge%
- Spacer profile determined at indentation
- Box shape profile is target
  - provides best L_{metal} control and variability
  - protection of S/D epitaxy from etch at channel release
- Inner spacer thickness of 5 nm is optimum for performance and C_{eff}



Frougier, SSDM (2021).

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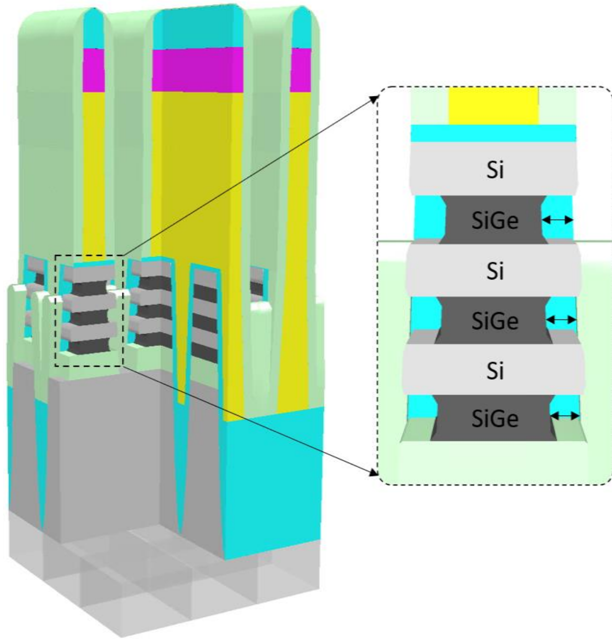
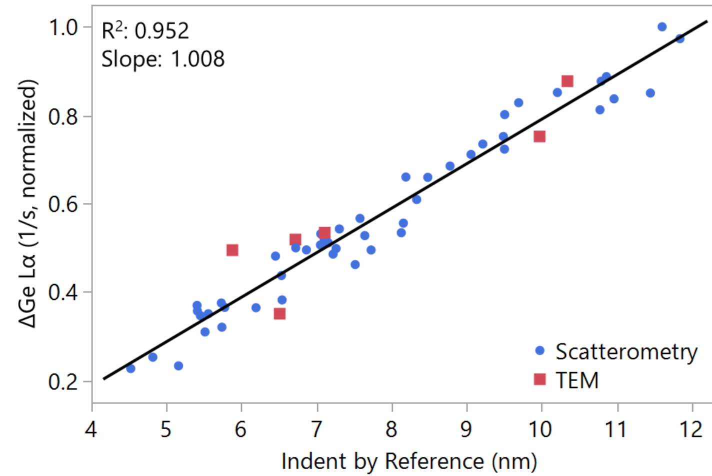
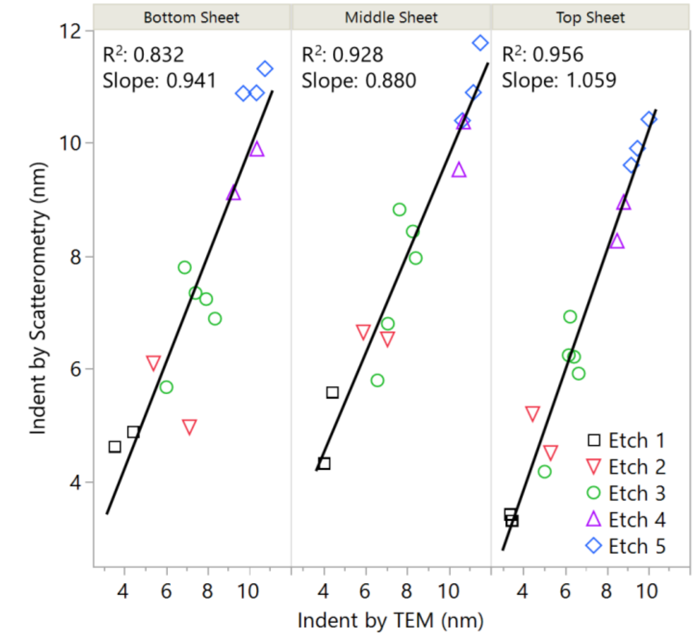
Inner Spacer Module







Average Indent Monitoring

✓ XRF – measure Ge counts
✓ Scatterometry
✓ ML Model (Scatterometry + ΔXRF)

Sheet-Specific Indent Monitoring

✓ Scatterometry
✓ ML Model (Scatterometry + TEM)

→ no in-line solution for indent shape or
Si sheet cleanliness post inner spacer etch back

Kal et al., CMC (2022).

Schmidt et al., IEEE-TSM (2022).

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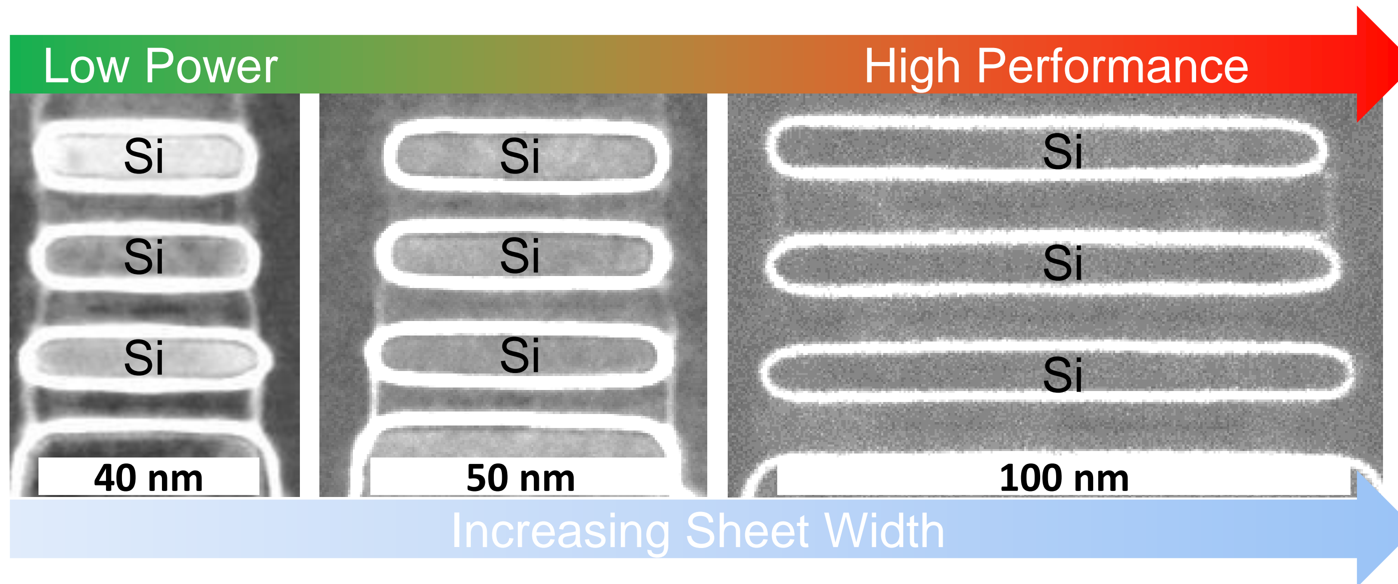
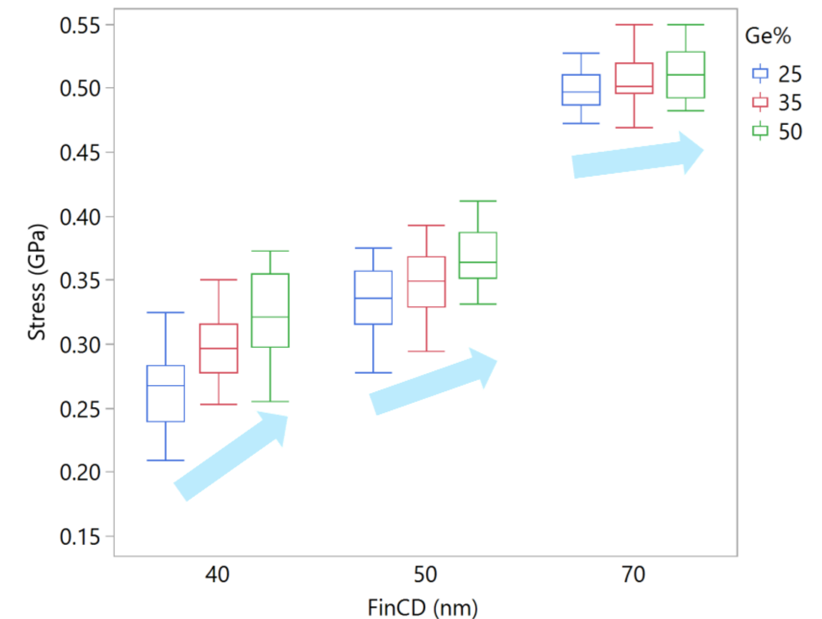
Channel Release





Highly selective SiGe etch to enable gate-all-around formation (selectivity demonstrated of >800:1)

- ✓ monitor complete removal of sacrificial SiGe → XRF, OCD, SEM
- ✓ monitor remaining Si sheet thickness → OCD
- ✓ monitor Si sheet strain/stress → Raman
- ▪ monitor sheet sagging → AFM, CDSEM, OCD

in-line Raman measurements of Si sheet strain for different sheet widths and Ge concentrations (sacrificial SiGe sheets)
→ agreement with simulations!

Schmidt et al., SPIE (2021), JM3 (2022).
Frougier, SSDM (2021). Breton et al., JM3 (2022).

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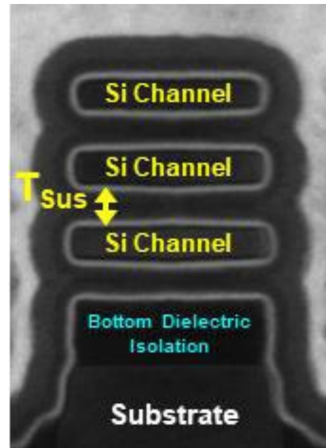
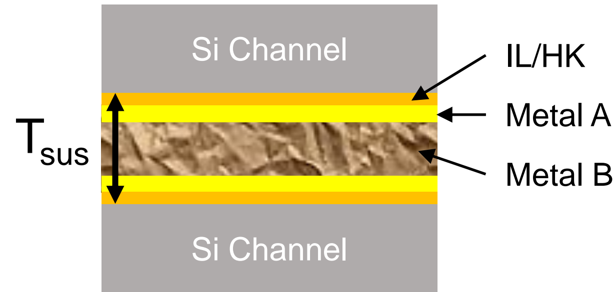
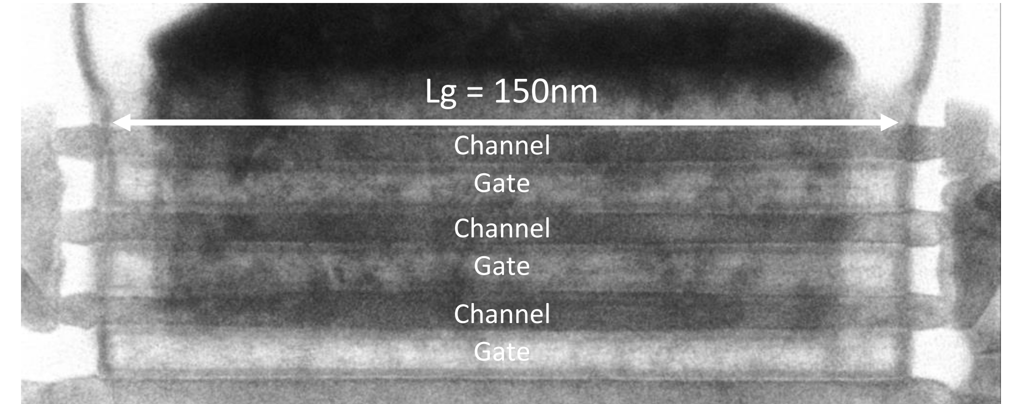
Gate-All-Around and Multi-Vt







- ❑ Multi-Vt solution is vital for technology flexibility to address both High-Performance Compute (high drive current → high Vt) and low power mobile applications (low leakage → low Vt)
- ❑ Classical approach for Multi-Vt using nWFM and pWFM thickness is not as effective in extremely narrow spaces limited by both Lg and Tsus
- ❑ **Solution**: "Volume-less" dipoles at IL-HK interface

- monitor IL/HK thickness uniformity
- monitor Metal A,B thickness uniformity
- monitor dipoles (what, where)

→ ideally, sheet-specific

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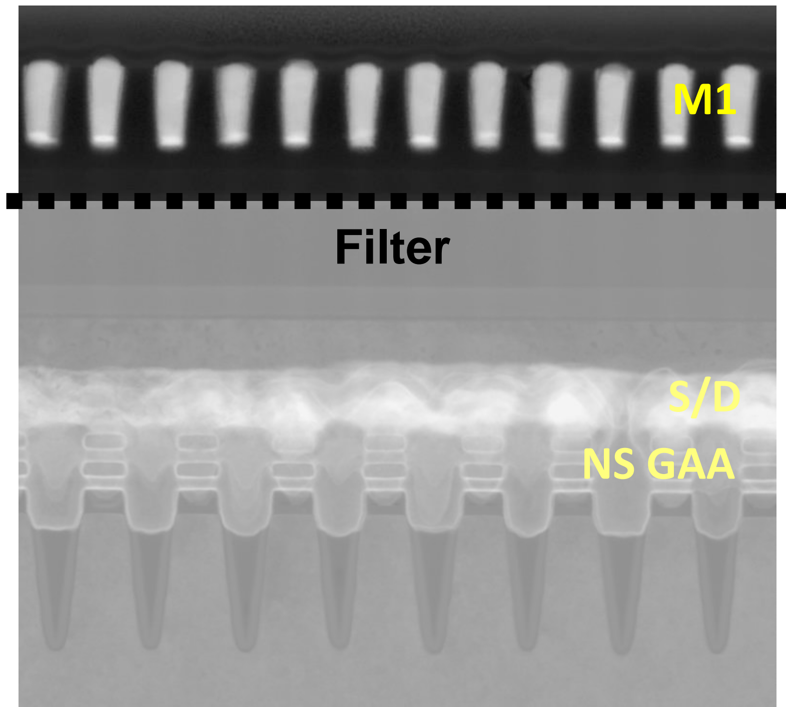
Bao et al. IEDM (2019); VLSI (2020)

BEOL Metrology

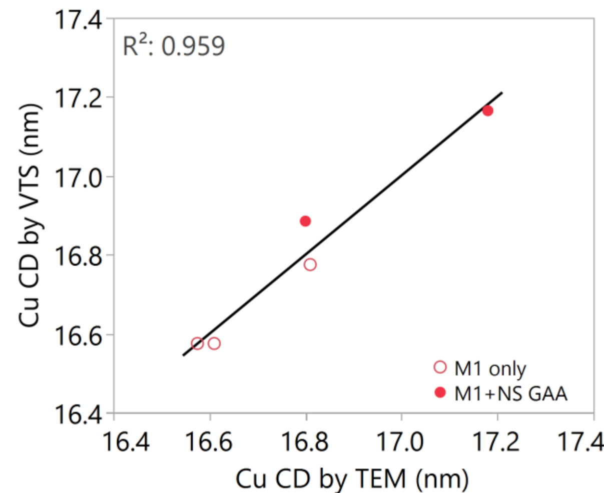


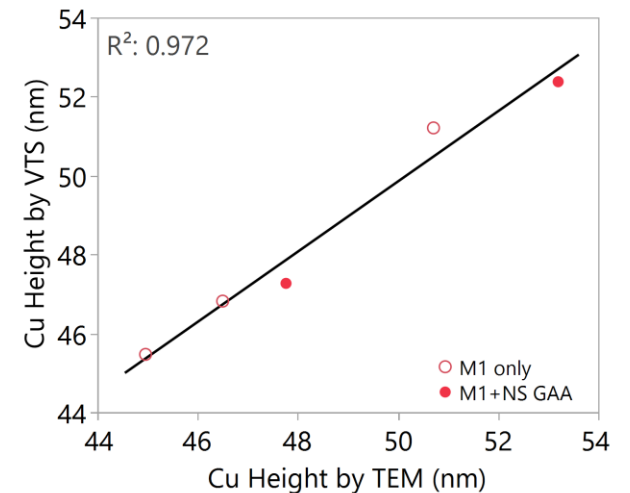
desire to measure M1 line height and CD on device-like target rather than on solid stack

traditional OCD modelling possible but complicated

→ **Vertical Travelling Scatterometry (VTS)**

Filter irrelevant spectral information for simplified solutions





Schmidt et al., SPIE (2022).

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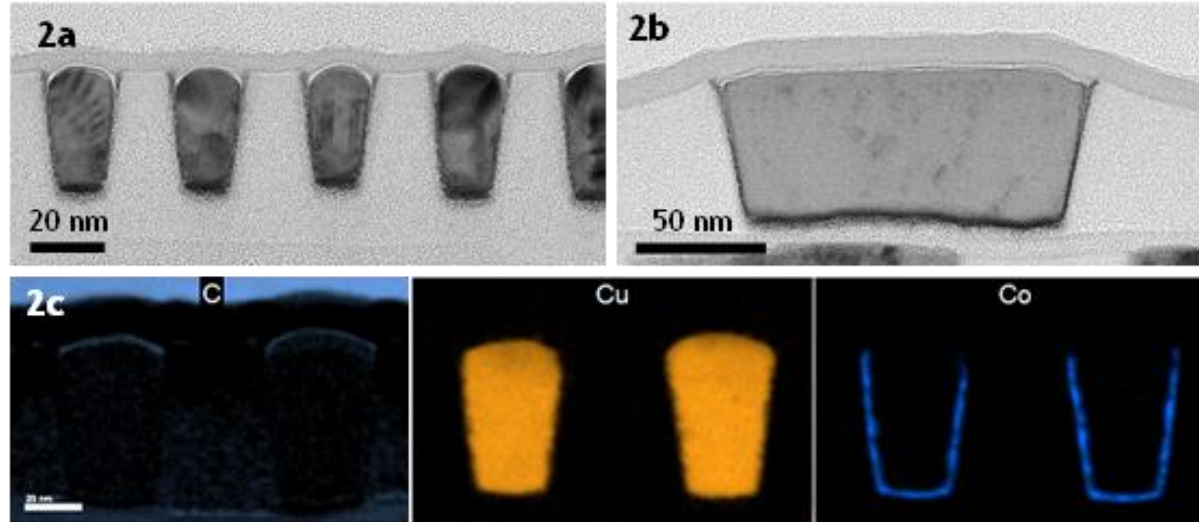
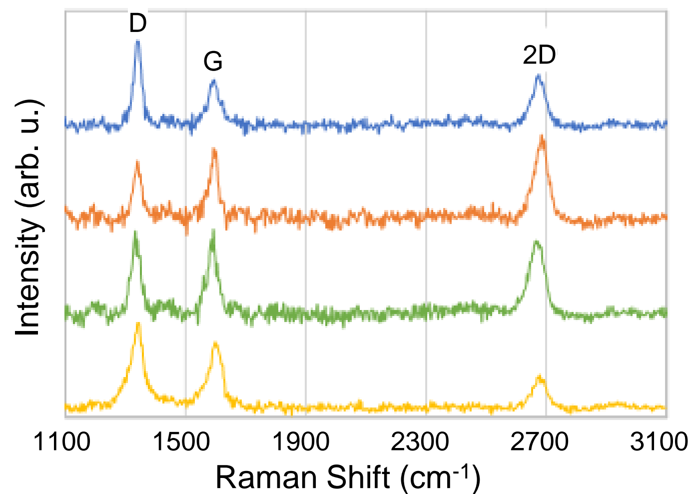
What’s Next: 2D Materials Characterization

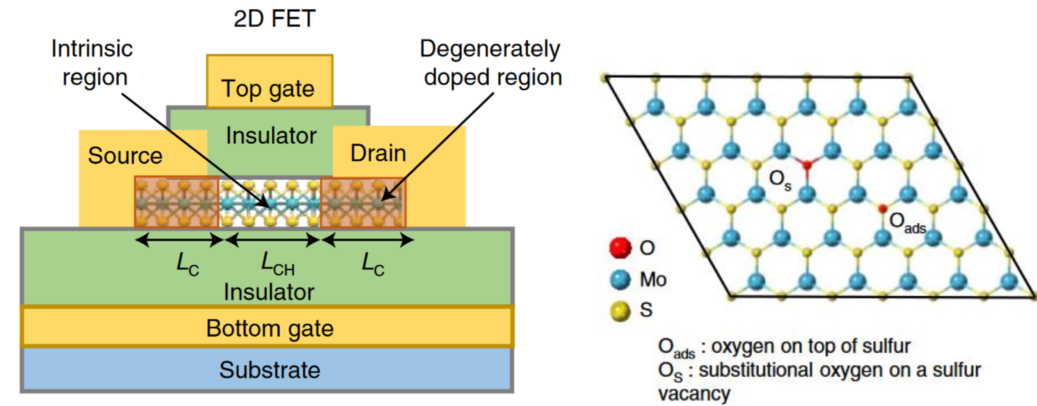


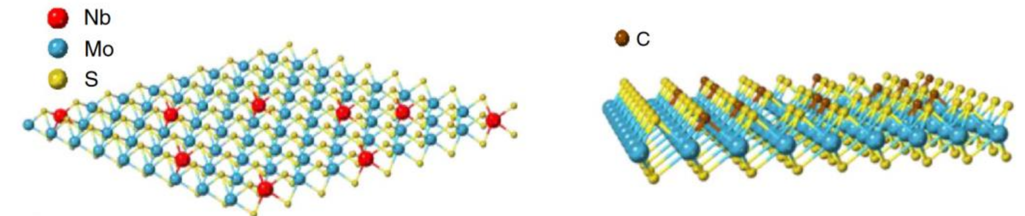


Graphene cap formation on 300 mm wafers

Nogami et al. IEDM 2021

Transistors with two-dimensional channels





Electrical | Chemical | Optical | Structural

Metrology and Characterization needs will keep us busy!

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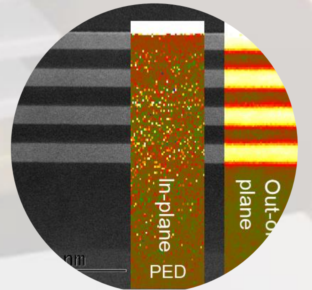
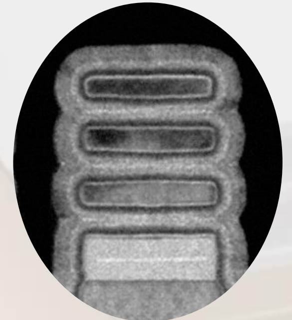
Das et al. Nature Electronics 4, 786 (2021)

Takeaways

Process complexity has increased and so has the amount of metrology required
→ this trend will continue (keywords: backside power, transistor stacking, bonding)



- in the nanosheet era, metrology is a process enabler, not just yield enhancer
- any decrease in measurement uncertainty translates to improved device performance
- further developments of existing techniques and new lab-to-fab introduction required



2D materials will be coming → material and interface characterization critical

Metrology has been gaining importance and will continue to do so

The future is bright!

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Acknowledgements

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Theo Standaert
Nelson Felix

Pathfinding Alliance and Ecosystem Partners at Albany, NY

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