Semiconductor
Research
Corporation

Center for Heterogeneous Integration of Micro Electronic Systems Vision & Plan

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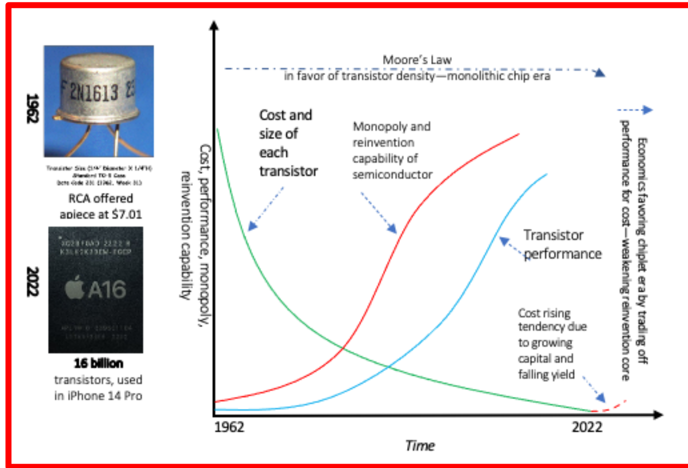
CHIMES
Center for Heterogeneous Integration
of Micro Electronic Systems

Introducing our 23 PIs and 15 Partner Universities

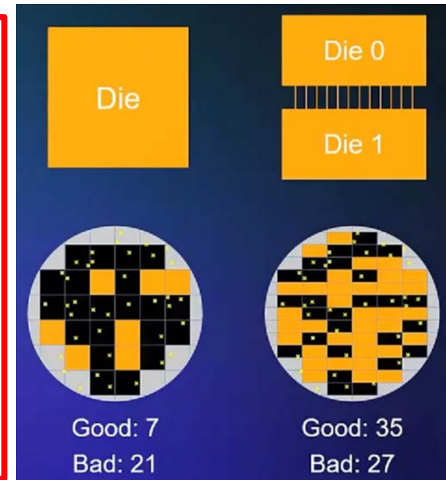
Economics & Continuation of Moore's Law

The Solution

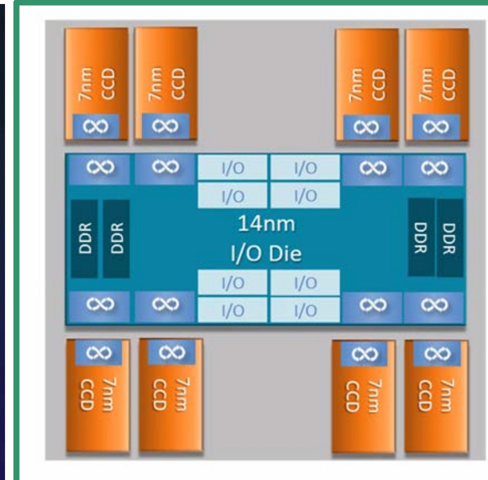
The Problem



Improved Yield

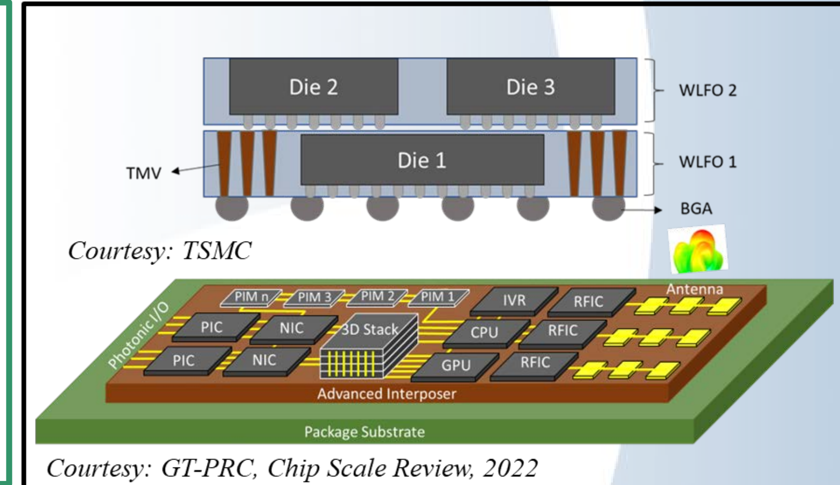


Shorter design time



Courtesy: AMD

Heterogeneous Integration



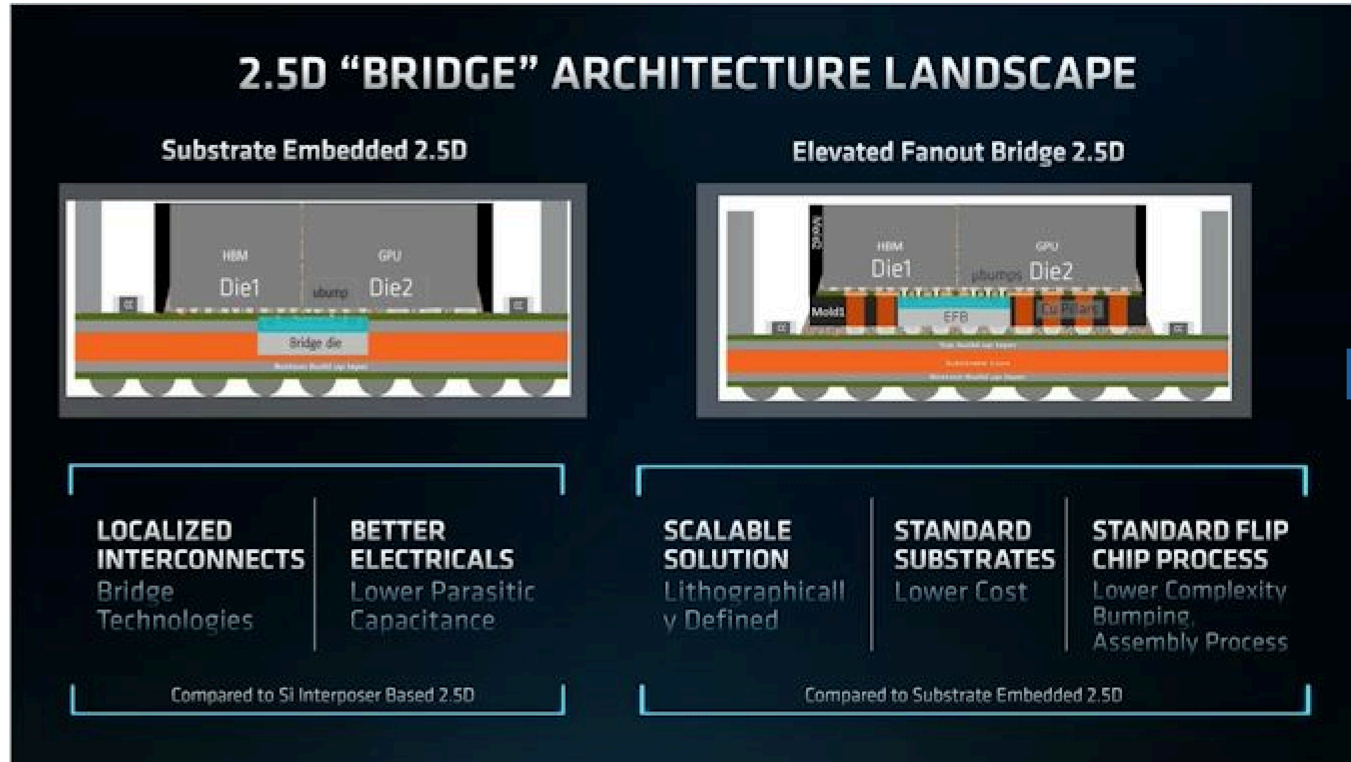
Three reasons why Advanced Packaging is becoming critical for the continuation of Moore's Law:

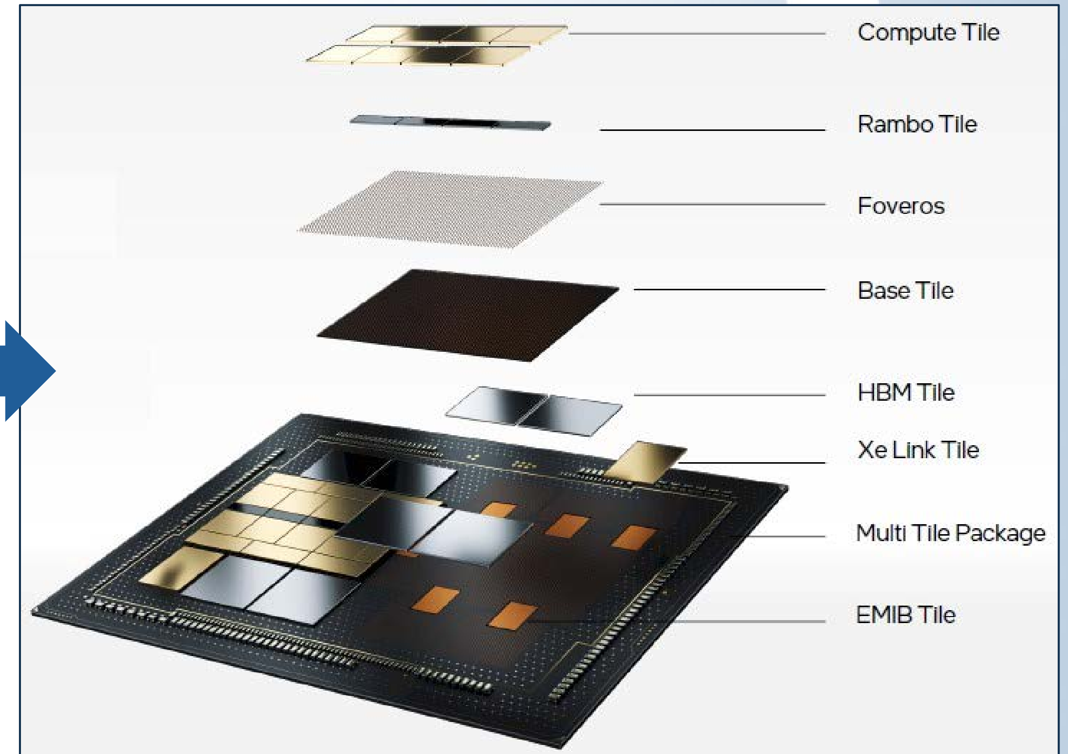
1. Higher yield using smaller dies in advanced nodes.
2. Shorter time to design with smaller dies from optimized legacy technology nodes with enhanced functionality.
3. Move towards **HETEROGENEOUS INTEGRATION**.

Advanced Packaging – Industry SOTA

2D Connectivity

2D & 3D Connectivity



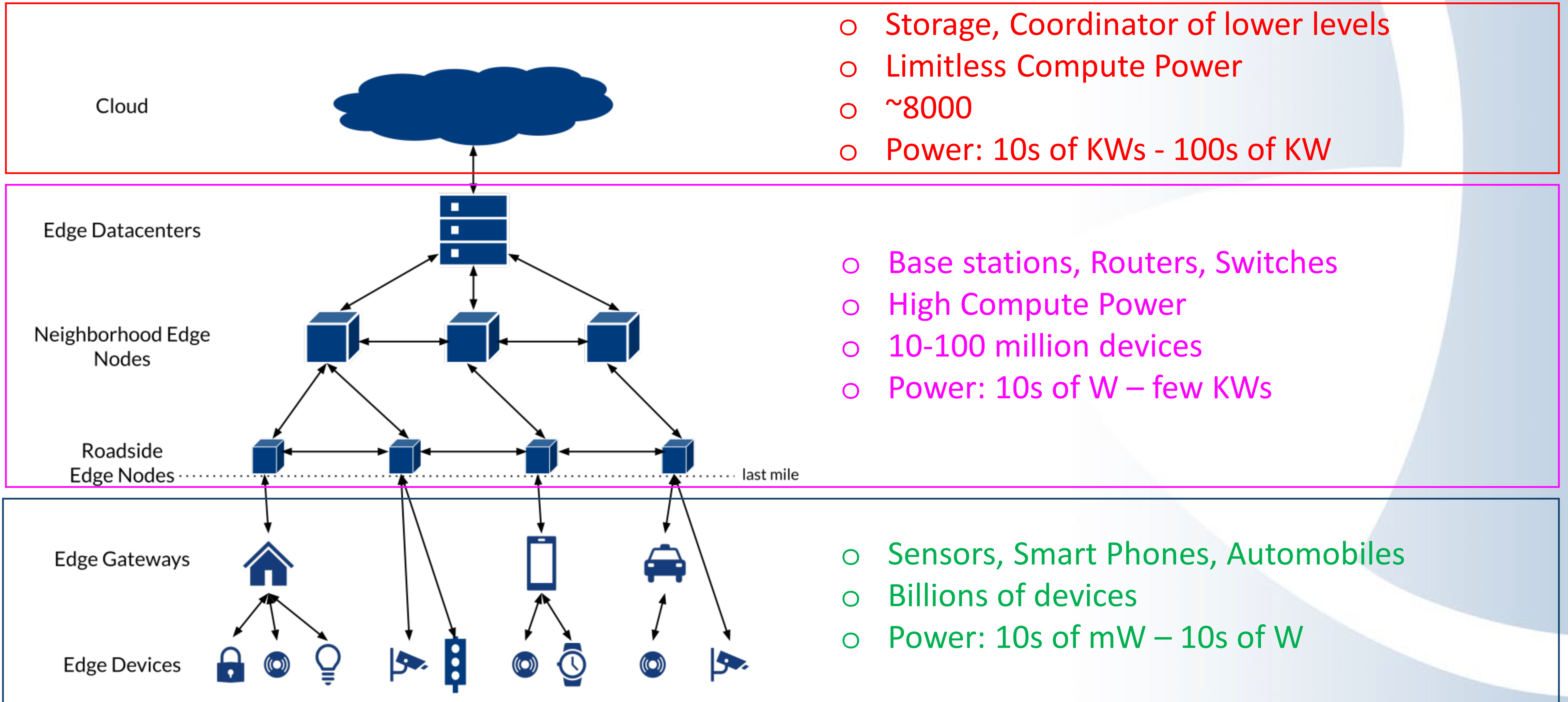


https://www.anandtech.com/show/17054/amd-announces-instinct-mi200-accelerator-family-cdna2-exacale-servers/2

https://www.nextplatform.com/2021/08/24/intels-ponte-vecchio-gpu-better-not-be-a-bridge-too-far/

Ponte-Vecchio - 47 dielets with over 100 billion transistors (Shift from Cost/Transistor to Cost/Function)

Distributed Computing and Communications



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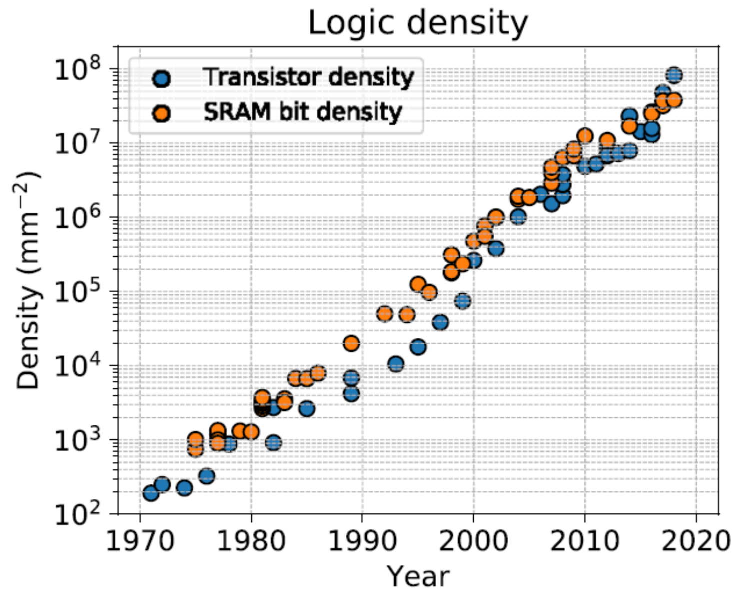
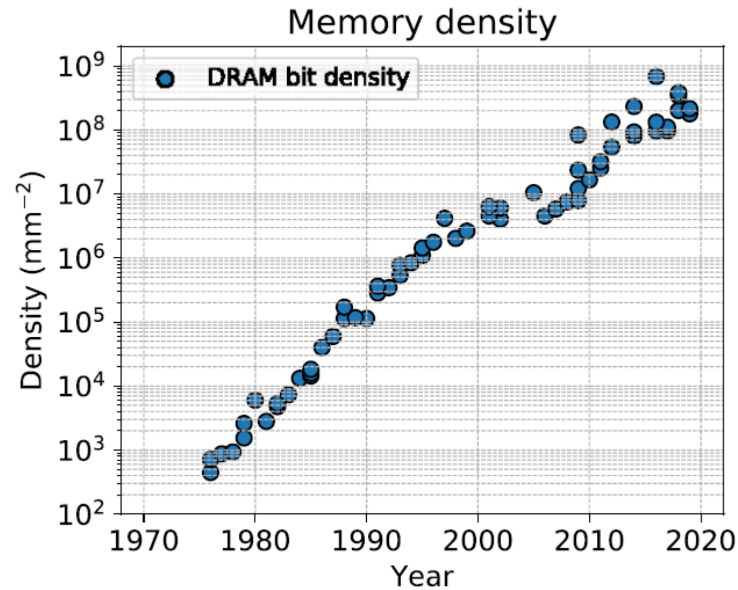
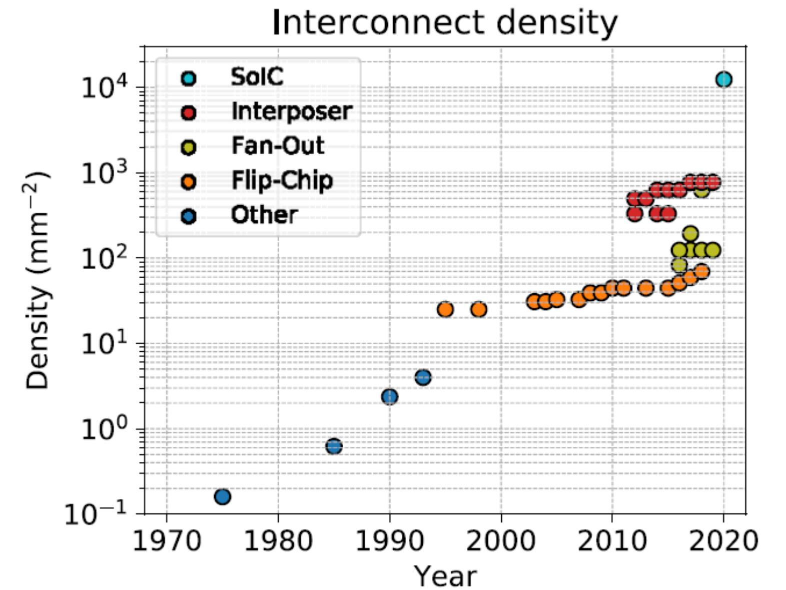
https://www.inovex.de/de/blog/edge-computing-introduction/

Ref: Jeff Burns, "Systems and Architectures for Distributed Compute", SRC Workshop, 2022.

Where are we today & What is needed in the Future?







H.-S. Philip Wong, et al, "A Density Metric for Semiconductor Technology", Proceedings of the IEEE, April 2020

Current State of the Art

- Monolithic logic 10^8 transistors/mm^2
- DRAM 10^9 transistors/mm^2
- IO density 10^4 IO/mm^2
- SRAM Access 20-50 TBps

Emerging distributed and edge computing applications require unprecedented compute and communications capabilities that require far larger logic, memory, IO, & Bandwidth densities!

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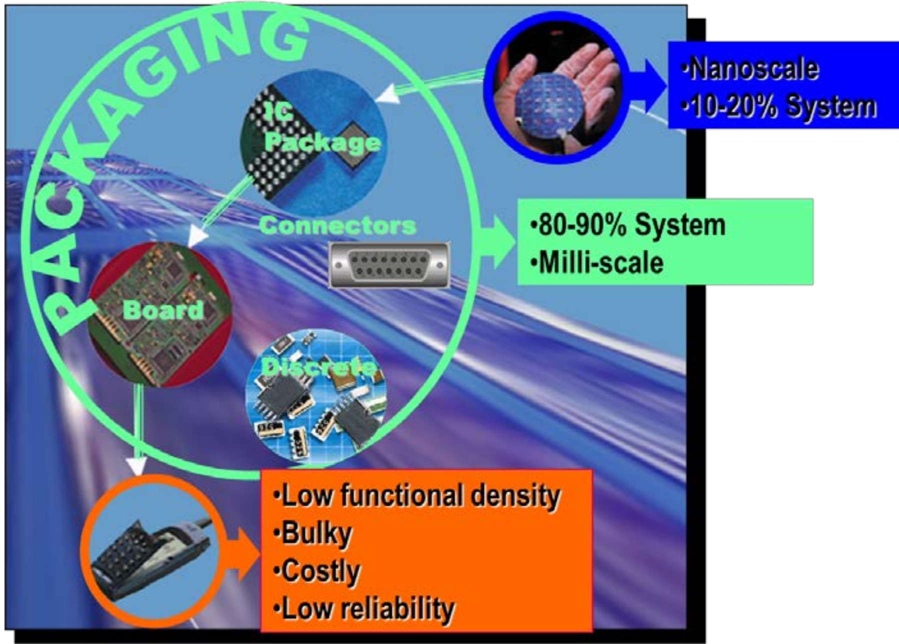
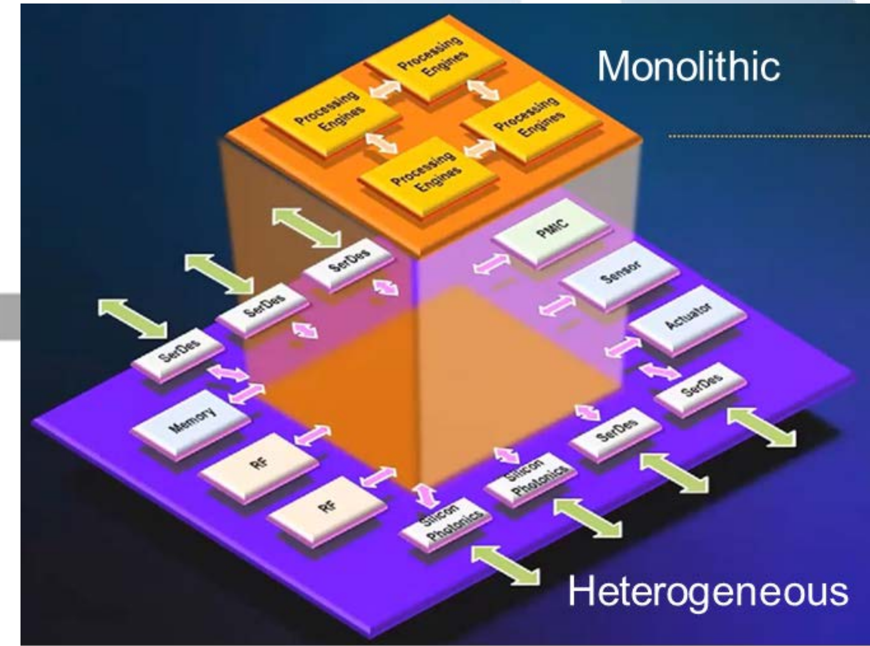
How do we get there?



Packaging (Past)

Advanced Packaging (Present)



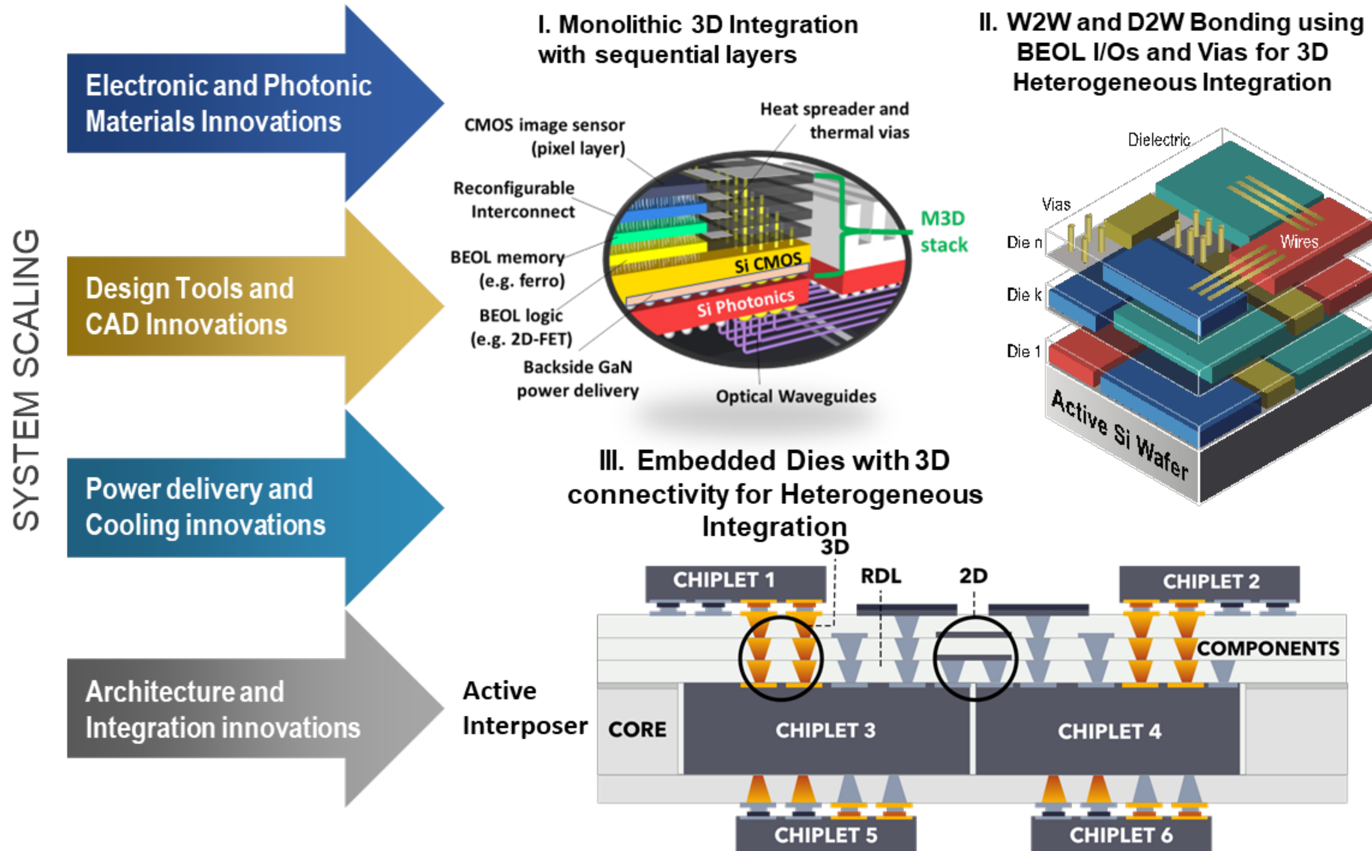
Courtesy: EDAPS 2020, Keynote

- **Present:** FEOL Transistor, BEOL Wiring & Package individually developed and combined
- **Future:** New and transformative logic, memory, and interconnect technologies that overcome the inevitable slowdown of traditional dimensional scaling of CMOS by interconnecting a **diversity of transistors and integrated circuit components**, **blurring the line between what is on-chip and what is off-chip**.

Center Vision & Plan

- Using emerging applications as the driver, our vision is to demonstrate radical heterogeneous integration architectures that enable over a billion transistors per mm^2 with an electrical and optical bandwidth density exceeding 500TBps/mm^2 at femto-joules/bit energy efficiency while developing simulation, deep co-design, and benchmarking tools and methodologies to drive center metrics and promoting center-to-center collaborations.
- We plan to achieve this vision through a combination of novel materials, design tools, architectures, integration strategies, power delivery and cooling technologies.
- CHIMES is a horizontal center with emerging applications and systems driving new technologies; and new technologies enabling future applications & systems.

Center Plan Details



System Scaling Metrics

- Power, Performance, Form-factor, Cost, and Reliability

Enabled through:

- 10-100X increase in transistor densities
- Support of a range of interconnect densities 10^4 to 10^6 and higher (100X)
- Use of 3D integration to reduce energy per bit (EPB) by 3 orders of magnitude (compared to 2D) to femto-joules/bit
- Co-integration of electronics and photonics to enable 500TBps/mm^2 of bandwidth (10X increase)
- Wireless communication at the edge supporting bandwidth of 1Tbps, using 6G frequencies.

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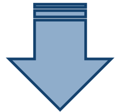
Metrics Driving Four Themes

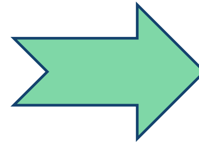
Emerging Applications & Systems: Cognition - AI, Communication - C, Sensing - S, Distributed Computing - DC, Intelligent Memory - M, and Harsh Environments - H)

Metrics & Drivers

State of the Art (SOTA)



Center Metrics



- THEME I: System Driven Functional Integration & Aggregation
- THEME II: Monolithic 3D (M3d) Densification and Diversification on Silicon Platform
- THEME III: Ultra-dense Heterogeneous Interconnect & Assembly
- THEME IV: Materials Behavior, Synthesis, Metrology, And Reliability

Grand Challenges

1. Heterogeneous integrated systems with volumetric transistor and interconnect densities approaching monolithic integration through 250-nm pitch self-aligned chip I/Os, and massive and seamless photonic connectivity with bandwidth density of 100Tbps/mm.
2. A generalized framework for materials synthesis and implementation with optimized properties.
3. Power management with segmented and deeply integrated power delivery solutions at 50kW with >80% efficiency.
4. Ultra-compact multi-scale thermal management solutions for densely integrated electronic, photonic, and sub-Terahertz components with micron-scale heat spreaders for >1kW/cm^2 heat flux, and superior energy efficiency and reliability.
5. Reconfigurable photonic interconnects enabling adaptive & optimized system configurations achieving > 100X enhancement in energy-efficiency and throughput compared to SOTA.
6. Fully integrated electronics, photonics and thermal design automation platform.

SAB Feedback – Addressing the Lowlights

- The large number of grand challenges could somewhat dilute center focus. A couple potential areas to improve include the device development tasks in Theme 2 (II.2 and II.3) which lack focus on the heterogeneous integration theme of the center. Center directors should try to take advantage of what has been attempted by industry to complement their research trajectory. – Task II.2 redefined with power delivery focus & Task II.3 redefined towards 2D materials-based photodetector for optical TSV.
- The lack of focus on design environment, metrology, and process scaling could be improved.
  - Design environment – Addressed In Theme I.
  - Metrology – Every theme has metrology embedded in it. Addressed during panel.
  - Process Scaling – Themes II, III, IV address process scaling through metrics.
- Strong emphasis on vertical M3D carries high risk. The cooling, yield, thermal budget, and manufacturing challenges are concerning. Backside power delivery, enhanced SRAM, etc. are important topics in logic, but may detract from the overall mission and objective of this mission. - Theme II has been suitably modified to reduce risk.
- The applications outlined in this proposal are narrower than the broader goal claimed within the center and not strongly aligned with industry interests. Specifically, theme 2 describes: "We will use real-time streaming and processing massive data (e.g., 4K/8K ultra-high-resolution video) for the autonomous vehicles (drones), augmented reality (AR) glasses and virtual reality (VR) headsets as application drivers to focus our research". Please work with the Liaisons and SAB to help better define more relevant/appropriate demos. – Application in Theme II is being modified. Need more industry input.
- Proposal clearly states the vision and challenges in 3D integration but is short on technical details for their approaches.
  - Several tasks related to 3D integration. Elaborated during panel.

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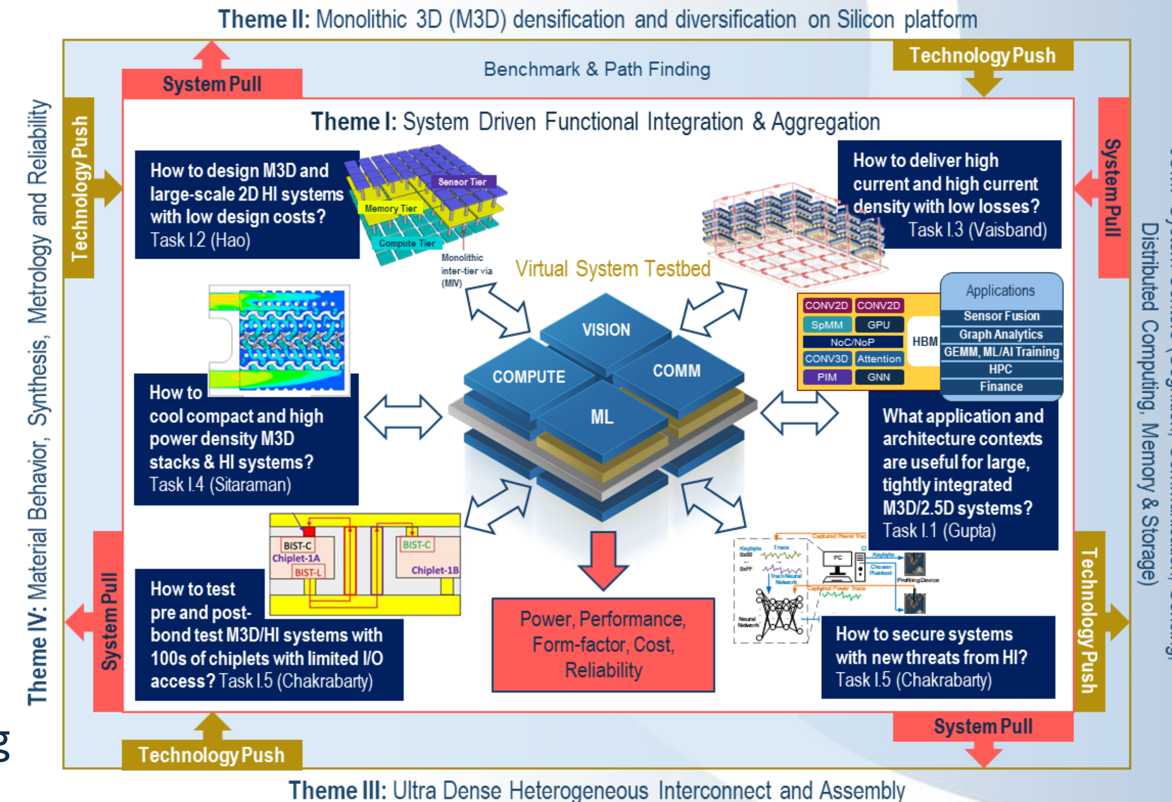
THEME I: System Driven Functional Integration & Aggregation (6 Tasks)

- **PIs: Puneet Gupta (UCLA-Theme Leader)**, Callie Hao (GT), Inna Partin-Vaisband (UI-Chicago), Suresh Sitaraman (GT), Krishnendu Chakrabarty (ASU)
- Co-PIs & Co-Is: Madhavan Swaminathan (PSU), Zhiting Tian (Cornell), Ben Yoo (UCDavis), Shimeng Yu (GT), Subramaniam Iyer (UCLA), Michael Taylor (UW)
- Focus areas:
  - M3D/HI design methodologies and design automation.
  - Power distribution (high current density, low-loss vertical power delivery).
  - Thermal modeling and cooling (both within the M3D stack as well as cooling large sized interposer substrates).
  - Test (pre-bond, mid-bond and post-bond).
  - Security (side-channel, trojans, IP theft).
  - 3D Architectures (Added post award)
  - Theme I serves as the focal point within the center for driving and benchmarking new technologies through virtual testbeds and rapid system-to-technology pathfinding approaches.
  - **Theme I also serves as the focal point for the 4/5 JUMP 2.0 System Centers**



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THEME I: Metrics, PIs & Tasks

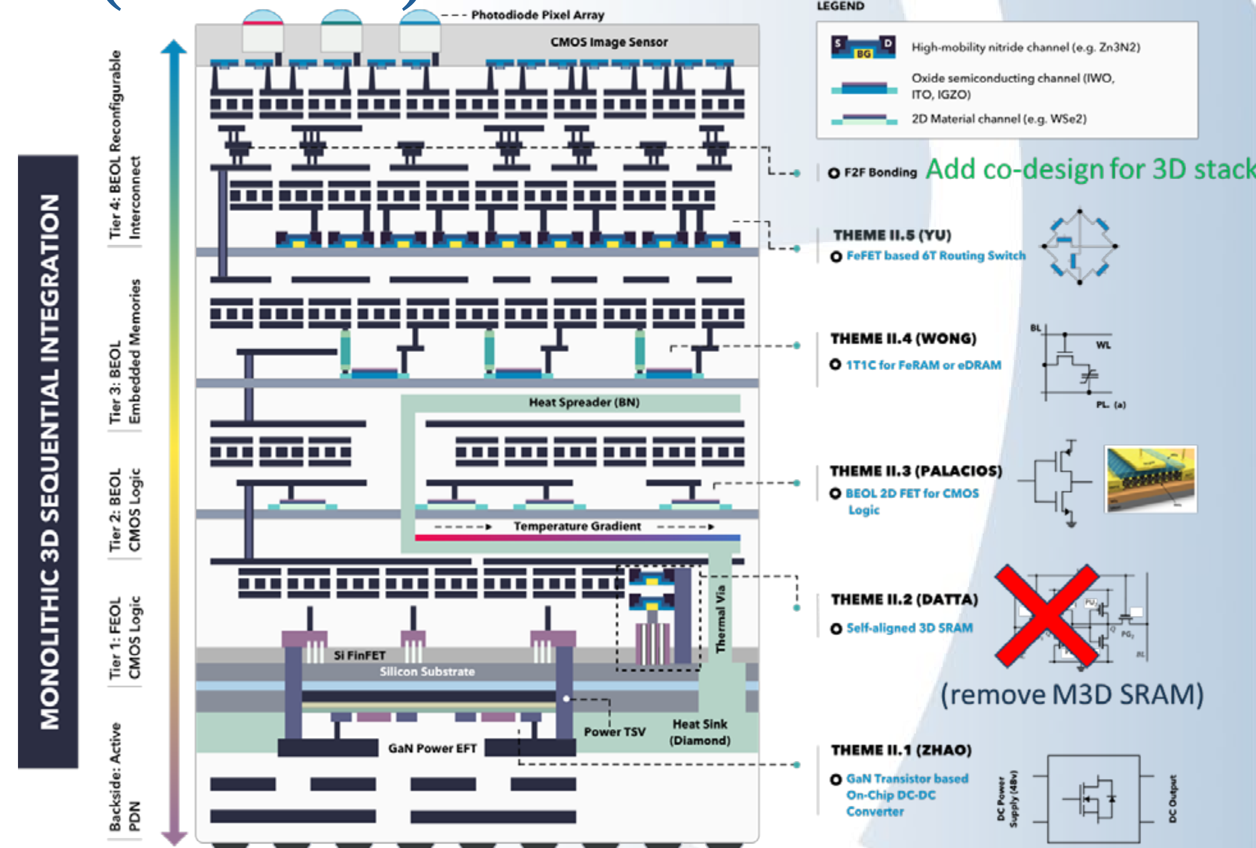
Metrics & Drivers	Center Proposed Metrics	State of the Art (SOTA)
Benchmarking (AI, C, S, DC, M, H)	Automated cross-layer pathfinding framework with Power, Performance, Form-factor, Cost and Reliability (PPFCR) prediction for full systems + applications.	Pathfinding limited to technology or technology + circuit only; limited automation.
Co-Design (AI, C, S, DC, M, H)	Physical design tools for M3D chiplets integrated on systems spanning > 20,000mm^2	No tools for M3D; interposer tools limited to ~2000mm^2
Power Delivery (AI, DC, H)	Power 1000W; Current density 2-5A/mm^2; Efficiency >80% (HIR 10 year)	Power 400W; Current density 1A/mm^2; Efficiency <70%
	Current 50 kAmps; Power 50kW; PDN Power <1kW (2%); Efficiency>80%	Current 18 kAmps; Power 10kW; PDN 5kW (33%); Efficiency <67% (Tesla Dojo)
Thermal (AI, C, DC, H)	Chiplet: Background heat flux (entire die) 2kW/cm^2; hot spot heat flux (0.1mm x 0.1mm) 30kW/cm^2; Vol. removal 2kW/cm^2 mm; Thermal time constant 1μs	Background heat flux (entire die) 200W/cm^2; hot spot heat flux (1mm x 1mm) 1kW/cm^2; Vol. removal 200W/cm^2 mm; Thermal time constant 20μs
	Stack: Thermal isolation ratio 0.95; TIM specific resistance 0.3 mm^2 K/W for 30 μm; k 200 W/mK, elastic modulus 30 MPa	Thermal isolation ratio 0.5; TIM specific resistance 1 mm^2 K/W (DARPA NTI)
	Interposer: Heat spreader effective k 10,000 W/mK; Heat spreader thickness 0.2mm	Heat spr. effective k 4000 W/mK; Heat spreader thickness 2mm (DARPA TGP)
	Server (1U): Volumetric R_{th} 0.015 $^oCcm^3/W$	Volumetric R_{th} 0.03 $^oCcm^3/W$
Electrical/Optical Test (AI, DC)	Fault coverage >99% (Short/Open) & >95% (device/components)	<95% coverage (Short/Open), devices/components (no test or BIST)
	10X reduction in test cost (Package BIST)	(Relative) test cost growing
Hardware Security	Probability of trojan evasion >99%	No universal security metrics available
	Probability of reverse engineering <1%	No universal security metrics available
	Split manufacturing based on fine pitch HI	Not available

PI	Expertise
Puneet Gupta	Applications & System Architectures
Krishnendu Chakrabarty	Test & Security
Suresh Sitaraman	Thermal Management & Reliability
Inna Partin Vaisband	On-chip & System Power Delivery
Callie Hao	Electronic Design Automation
Michael Taylor	3D Architectures

- TASK I.1: System-driven Benchmarking and Pathfinding for Monolithic 3D and Heterogeneous Integration
- Task I.2: Design Automation for Monolithic 3D and Heterogeneous Interposer Integration
- Task I.3: Low Loss Vertical System-Level Power Delivery with Backside M3D and Integrated Voltage Regulators
- TASK I.4: Flexible, Multi-Functional Thermal Management and Electro-Thermal Modeling for Ultra-Compact High Power Density Systems
- TASK I.5: Electrical Test and Security for Integrated M3D and HI Systems
- Task I.6: 3D Architectures

THEME II: Monolithic 3D (M3D) Densification and Diversification on Silicon Platform (5 Tasks)

- **PIs: Shimeng Yu (GT-Theme Leader)**, Suman Datta (GT), Philip Wong (Stanford), Tomás Palacios (MIT), Yuji Zhao (Rice)
- Co-PIs & Co-Is: Inna Partin-Vaisband (UI-Chicago), Steven George (Colorado), Volker Sorger (GWU)
- Focus areas:
  - BEOL compatible logic transistors based on oxide semiconductors (e.g., IWO, ITO, etc.), focusing on ALD process, improving Vth stability, etc.
  - BEOL compatible logic transistors based on 2D materials (e.g., WSe2, etc.), focusing on p-type and CMOS integration.
  - Explore the applications of BEOL logic transistors such as memory access (e.g., 2T gain cell, 1T1C FeRAM, etc.), or peripheral circuits for memory array (e.g., decoder, mux, S/A, etc.), or for ferroelectric gated router.
  - Backside "active" power delivery with GaN power transistor (e.g., 48V to 12V) or with oxide (e.g., IWO) power transistor (e.g., 12V to 3V)
  - Co-design with 3D floor planning with thermal profile modeling (considering heat spreader, e.g., BN to be developed in Theme IV)



Major changes based on SAB feedback

1. p-type GaN and CMOS integration
2. Amorphous Oxide Semiconductor for Integrated Power Delivery & Conversion
3. 2D materials-based photodetector for optical TSV
4. Improve current density per footprint for routing switch

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THEME II: Metrics, PIs & Tasks

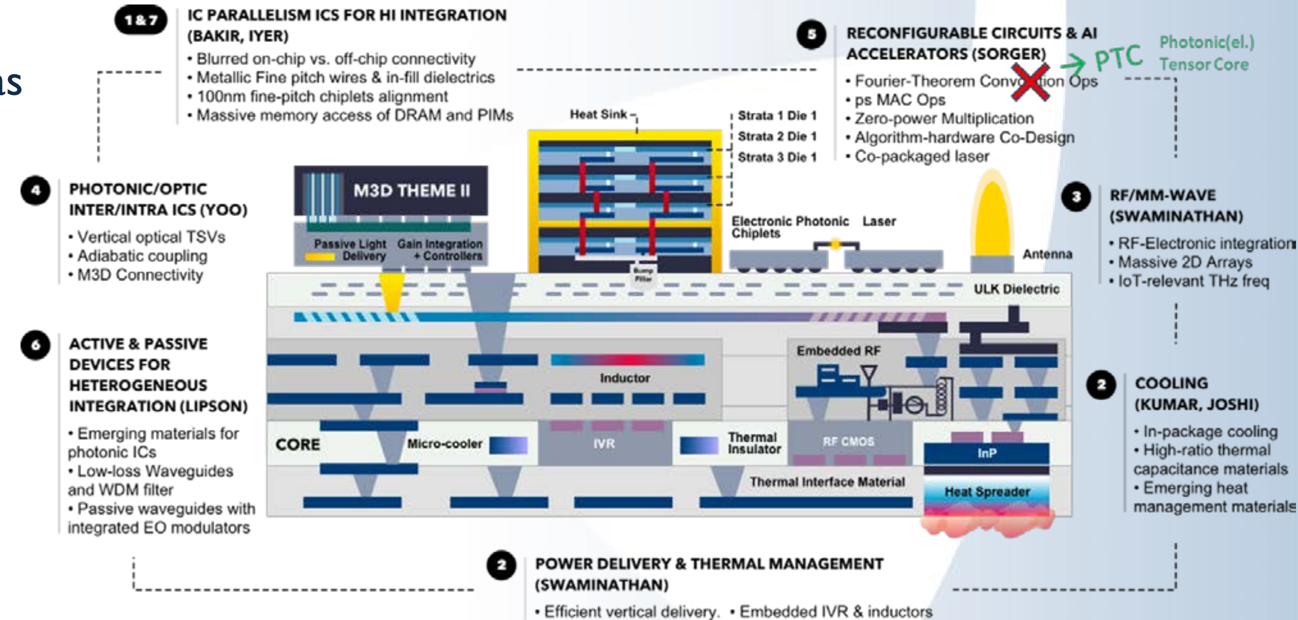
Metrics & Drivers	Center Proposed Metrics	State of the Art (SOTA)
Technology (AI, S, DC, M)	High-density 3D SRAM cell area (2CPP×3MP)	FinFET SRAM cell area (2CPP×8MP) CPP: contact-poly-pitch, MP: M1 pitch
	Mobility for BEOL transistor (2D, oxide, nitride)>100 cm^2/Vs	IWO transistor mobility ~20 cm^2/Vs (from JUMP 1.0)
	Drive current for BEOL memory access at 3V (>2mA/µm)	IWO drive current at 3V ~500µA/µm (from JUMP 1.0)
	BEOL thermal budget < 400°C (e.g. for Zn_3N_2)	GaN growth (~1000°C)
	GaN p-type FET drive current (>1A/mm)	GaN p-type FET drive current (>100mA/mm)
In-pixel Processing System Workloads (AI, S, DC, M) (TOPS normalized by 1b×1b MAC)	Efficiency >50,000 TOPS/W (M3D stack-level)	~5,000 TOPS/W (TSMC ISSCC 7nm SRAM CIM, 4kb 2D macro-level)
	Compute > 5,000 $TOPS/mm^2$ (M3D stack-level)	~500 TOPS/mm2 (at 2D macro-level)
	Power density <1 W/mm^2 (M3D stack-level)	~0.4 W/mm^2 (at 2D macro-level)
	Max runtime temperature (<85°C) (M3D stack-level)	2D circuit runtime temperature <85°C

PI	Expertise
Shimeng Yu	Improve current density per footprint for routing switch; Co-design with 3D floor planning with thermal profile modeling
Philip Wong	BEOL Memories
Yuji Zhao	p-type GaN and CMOS integration
Tomas Palacios	2D materials-based photodetector for optical TSV
Suman Datta	Amorphous Oxide Semiconductor for Integrated Power Delivery & Conversion

- Task II.1: Backside of Silicon with GaN Integration for Active Power Delivery Network (modified)
- Task II.2: 3D Self-Aligned Super High-Density SRAM (modified)
- TASK II.3: BEOL Monolithic Integration of TMD-based CMOS Logic and Photonic Devices (modified)
- TASK II.4: BEOL eNVM/eDRAM Integration with Oxide Channel Access Transistor
- TASK II.5: BEOL High-Mobility FeFET for Reconfigurable Interconnect (modified)

THEME III: Ultra-dense Heterogeneous Interconnect & Assembly (7 Tasks)

- **PIs:Volker Sorger (GWU-Theme Leader),** Muhannad Bakir (GT), Subramanian Iyer (UCLA), Michal Lipson (Columbia), Madhavan Swaminathan (PSU), Ben Yoo (UCDavis)
- Co-PIs & Co-Is: Andrew Kummel (UCSD), Satish Kumar (GT), Suresh Sitaraman (GT), Inna Partin-Vaisband (UI-Chicago), Tomas Palacios (MIT), Shimeng Yu (GT), Puneet Gupta (UCLA), H.-S. Philip Wong (Stanford)
- Focus areas:
  - Die- and wafer-level electrical connectivity approaching BEOL densities for massively parallel interconnectivity.
  - Embedded and wrap-around cooling layers for heat rejection and thermal isolation within and between tiers leveraging advanced materials.
  - New power delivery architectures for extreme fine-grain power management.
  - 2D arrays of mmWave antennas connected vertically for control and amplification structures.
  - Parallelized photonic interconnects via optical through vias and high-speed OE devices and functional materials.
  - On-demand reconfigurability through electronics-photonics, conversion integration, and co-design architectures



Changes based on post-award assessment

1. Reconfigurable HI accelerators for AI/ML/DL
2. Replace Graphene EOM w/ Gr.-WSe2 junction cap EOM

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THEME III: Metrics, PIs & Tasks

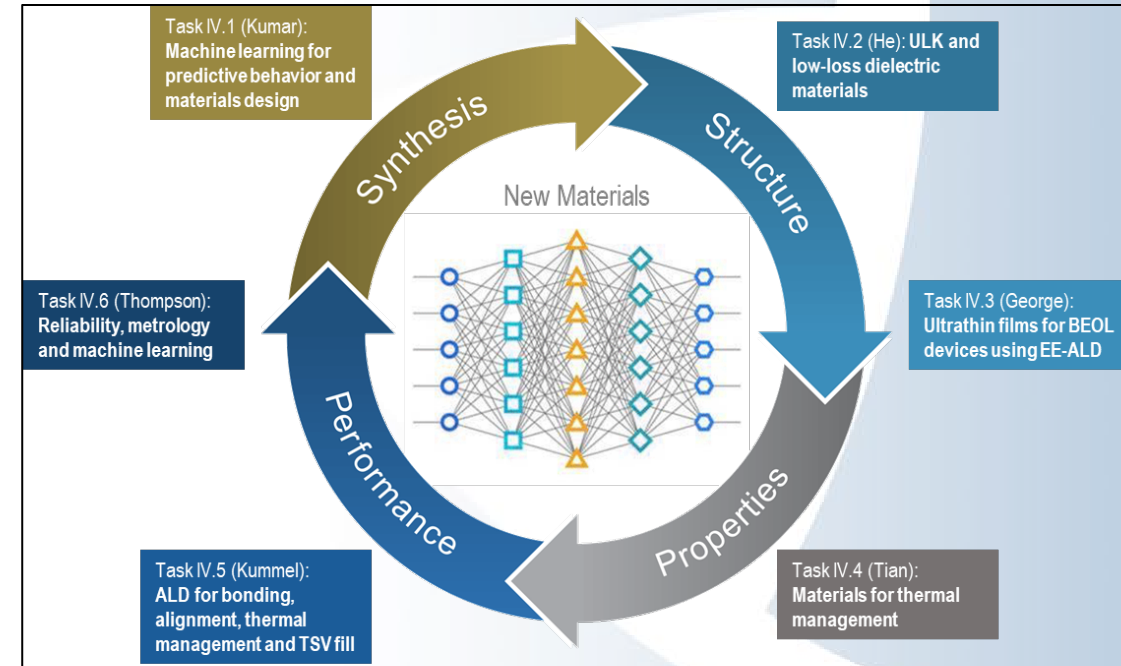
Metric & Drivers	Center Proposed Metric	State of the Art (SOTA)
Electrical IC Parallelism & Volume Scaling (AI, DC, M)	IO density 16M/mm^2	IO density 10K/mm^2
	BW Density > 500Tbps/mm^2; <0.01 pJ/bit	BW density 28Tbps/mm^2; 0.021 pJ/bit (ARM/GT IEDM 2020)
Cooling & Power Delivery (S, C, H, AI)	Power 1000W; Current density 2–5A/mm^2; Efficiency >80% (HIR 10 year)	Power 400W; Current Density 1A/mm2; Efficiency <70%
	Current 50 KAmps; Power 50kW; PDN Power <1KW (2%); Efficiency>80%	Current 18 KAmps; Power 10KW; PDN 5KW (33%); η <67% (Tesla Dojo)
Wireless IC & I/O (C, S, H)	Insertion Loss <1dB (PA output to Antenna input) @ 0.3 – 1THz; DARPA ELGAR 1dB	Insertion Loss >5dB in D-Band (110-170 GHz) (ComSenTer)
	Antenna efficiency >90% @ 0.3–1THz	Antenna efficiency >90% (< 100GHz)
	SNR 30dB (128 QAM)	SNR 20dB (128 QAM) D-Band
Photonic/Optic IC and Chiplet Communication (AI, C, DC)	Coupling loss < 0.9dB; Misalignment; +/−1mm	Coupling Loss ~ 1dB (O-Band)
	100 (Tbps/mm)/(pJ/bit) (link-level)	1 (Tbps/mm)/(pJ/bit) (DARPA PIPES)
	Bandwidth (BW) Reconfigurable ICs between chiplets; 0.5-5Tbps aggregated BW	NA
	Optical gain/laser integration via photonic wire bonds (PWB) and/or mono-int. (DARPA LUMOS)	Laser is off-chip → requiring packaging (costly & not reliable)
Reconfigurable Circuits & Modules (AI, S, DC)	100 TOP/J, 1ns latency, infinite bit-resolution MAC ops (DOD Labs e.g., AFRL, ARL)	<5 TOP/J, 1000+ns latency, 4-12 bit
	AI accelerator: 10–100 fJ/MAC, 1–50 TMACs/mm^2, 1ns–25 ps operation (Google X)	0.5–1 pJ/MAC, 0.5–1 TMAC/s/mm^2, 0.5–1 GMVM/s, and 1–2 us per MVM
Active & Passive Devices for Heterogeneous Integration (C, S, DC)	EO Modulator: ER > 12dB; BW > 15GHz per channel; (next Gen AIM Photonics components)	NA
	Interposer Waveguides; losses < 0.1dB/cm	1.5dB/cm
	Interposer Filters for WDM: filter sharpness > 15dB over < 0.2nm BW (AIM Photonics Foundry)	NA

PI	Expertise
Volker Sorger	Reconfigurable HI accelerators for AI/ML/DL
Muhannad Bakir	3D Stacking, Bonding & Integration
Subramaniam S. Iyer	High Density Interposer & Assembly
S. J. Ben Yoo	Optical TSV & Optoelectronics
Michal Lipson	Optical Waveguides & Modulators
Madhavan Swaminathan	Sub-Thz mmWave, Power Delivery & Interposers

- Task III.1: IC Parallelism and Volume Scaling
- Task III.2: Embedded Power Delivery & Cooling Strategies
- Task III.3: Ultra-Low Loss Vertical (3D) Tiers with Actives and Passives for (sub) THz Sensory I/O
- Task III.4: Photonic/Optic IC and Chiplet Communication
- Task III.5: Electronic-Photonic Reconfigurable Circuits & AI Accelerators
- Task III.6: Active & Passive Devices for Heterogeneous Integration
- Task III.7: Lithographically Defined Fine Pitch Inter-Strata Interconnects for 3D Heterogenous Stacking using Hydrogen Exfoliation

THEME IV: Materials Behavior, Synthesis, Metrology, and Reliability (6 Tasks)

- **PIs: Carl Thompson (MIT-Theme Leader),** Satish Kumar (GT), Ximin He (ULCA), Steven George (Colorado), Zhiting Tian (Cornell), Andrew Kummel (UCSD)
- Co-PIs & Co-Is: Yuji Zhao (Rice), Subramanian Iyer (UCLA), Madhavan Swaminathan (PSU), Suman Datta (GT), Muhannad Bakir (GT)
- Focus areas:
  - New principles and methods for design of materials across length scales
  - New approaches for characterization of properties, including measurement of reliability made at different stages of development.
  - Thermal interface materials, materials that spread heat laterally and conduct heat vertically through thermal vias, and materials that provide thermal isolation.
  - Photo imageable ultra-low-k materials for interlayer BEOL electrical interconnections and ultra-low-k/low loss materials for sub-THz antenna integration.
  - Ultra-thin films for BEOL transistors, including semiconductor and high-k dielectric layers, along with diffusion/adhesion layers and bottom-upfilling of high aspect ratio BEOL vias.
  - New approaches for fabrication, alignment, and bonding of interlayer vertical interconnects at unprecedented high densities.



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THEME IV: Metrics, PIs & Tasks

Metrics & Drivers	Center Proposed Metrics	State of the Art (SOTA)
Ultra-low K Dielectrics AI, C, DC, M)	Permittivity < 2.5, Loss 0.01 @ 1THz, Thickness: 1μm – 100μm, CTE: <30 ppm/C	Permittivity 3.0, Loss 0.05 @ 150GHz, Thickness: 5mm, CTE: 30-40 ppm/C
Interconnects (AI, DC, M)	For BEOL Devices: 100nm pitch, 50nm dia., aspect ratio 2-10 for 2-5 tiers for via bottom-up fill.	400nm pitch, 200nm dia., aspect ratio up to 5 (selective ALD for Co from ASCENT)
	TSVs: 100 nm diameter, 250 nm pitch; aspect ratios >30:1	9 μm pitch and ~2μm diameter [AMD 3D V-cache]
	Misalignment-tolerant bonding process for inter-layer interconnects at 250 nm pitch	5.5 μm pitch using face-to-face hybrid bonding [ARM/GF]
Thermal (AI, C, S, DC, H)	TIM: 200W/m-K; Thickness <30μm; CTE 20 ppm/C	TIM: 25-100 W/m-K; CTE 55-200 ppm/C
	Heat Spreader: - cBN 200 W/mK at 100 nm thick, 500W/mK at 1 μm - Diamond 400 W/mK at 1 μm, 1500 W/mK at 10 μm, 2000 W/mK at 50μm.	Heat Spreader: Cu 400 W/mK bulk
	Ultra-low interface thermal resistance, e.g. GaN/diamond 3 m^2K/GW, Si/diamond 3 m^2K/GW	GaN/diamond 6.5 m^2K/GW Si/diamond 9.5 m^2K/GW
	Thermal isolation materials: 0.02 W/m-K, dielectric constant < 1.5, thermally stable above 300°C	Thermal isolation materials (SiCOH): 0.6 W/m-K, dielectric constant 1.8-2.5, and thermally stable above 300°C

PI	Expertise
Carl Thompson	Reliability, Failure Modes, & Metrology
Ximin He	Synthesis of Polymer Materials
Steven George	ALD/ALE for Metal Depsotion & Etching
Andrew Kummel	ALD, Thin Film AlN, & Diamond Dep.
Satish Kumar	Physics based models & ML
Zhiting Tian	TIM & Transport Modeling

- Task IV.1: Machine Learning Enabled Predictive Behavior and Materials Design
- Task IV.2: Photo-definable ULK and Low-Loss Dielectric Materials, with Electrical, Mechanical & Thermal Integrity
- TASK IV.3: Ultrathin Diffusion Barriers and Bottom-Up Metal Interconnects Using Electron-Enhanced Atomic Layer Deposition (EE-ALD) with Reactive Background Gas
- Task IV.4: Materials for Thermal Management
- TASK IV.5 Wafer and Chiplet Bonding with Selective ALD, Heat Spreader Infill, and Magnetic Alignment
- TASK IV.6: Machine Learning-enhanced Coordinated Materials Synthesis, Metrology, and Reliability

Cross Center Collaborations – Early Discussions

- COCOSYS
  - TBD
- CUbiC
  - Naresh Shanbhag, Pavan Hanumolu (CUbiC) & Muhannad Bakir, Michal Lipson (CHIMES)
- CogniSense
  - Muhannad Bakir & Inna Partin-Vaisband (CogniSense, CHIMES)
- ACE
  - Tushar Krishna (ACE) & Puneet Gupta (Theme I Lead, CHIMES)
  - Michael Taylor (ACE, CHIMES)
- PRISM
  - Shimeng Yu (CHIMES) & Tajana Rosing (PRISM)
  - Nam Sung Kim (PRISM) & Muhannad Bakir (CHIMES)
  - Vijay Narayanan (PRISM) & Madhavan Swaminathan (CHIMES)
- SUPREME
  - Monthly Director Meetings; Formalizing the collaboration model
  - Huili (Grace) Xing (SUPREME), Tomas Palacios (SUPREME, CHIMES); Muhannad Bakir, Madhavan Swaminathan (CHIMES)

Summary

- Center focus is on developing new and transformative Heterogeneous Integration technologies to overcome the slowdown of traditional dimensional scaling of semiconductors
- 23 PIs from 15 Universities
- 24 Research Tasks
- Expected: 85-87 graduate students supported per year
- Annual Review Sep 5-6, 2023 @ Penn State
  - We have one of the best creamery
- A passionate and well gelled team with senior and junior PIs off to a fantastic start!

CHIMES Pre-Center Kickoff Meeting
Nov. 16, 2022 @ Georgia Tech

Participation

- 21 PIs
- Qorvo
- IBM
- Intel
- Boeing
- Samsung
- ….

SRC Event: MRS Spring Meeting 2023

www.chimes.psu.edu

Nov. 16, 2022 @ Georgia Tech

SRC Event: MRS Spring Meeting 2023