SUPREME – a JUMP2.0 center Overview

April 26, 2023
SAB-Director F2F Meeting, @ADI
Huili Grace Xing, Cornell University
Tomas Palacios, MIT

Overview

- SUPREME Team overview
- Thrusts
- Q&A (~45 min)

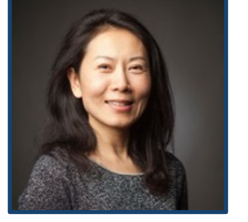
JUMP 2.0, Tentative Annual Review Dates

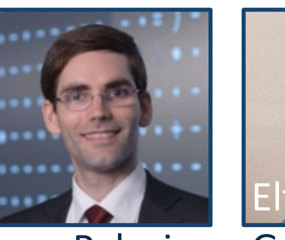
Center	Tentative Dates	Tentative Location
COCOSYS	May 16-17, 2023	Atlanta, Georgia Tech
CUBIC	June 27-28, 2023	NYC, Columbia
SUPREME	August 2-3, 2023	Ithaca, Cornell University
CHIMES	September 5-6, 2023	State College, Penn State
ACE	October 4-5, 2023	Urbana, UIUC
COGNISENSE	October 11-12, 2023	Atlanta, Georgia Tech
PRISM	October 8-9, 2023	La Jolla, UCSD

14 Universities – 1 Center

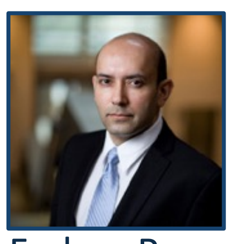
25 PIs – One SUPREME

PIs


Grace Xing


Tomas Palacios

Elton Graugnard

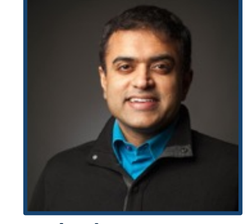

Farhan Rana

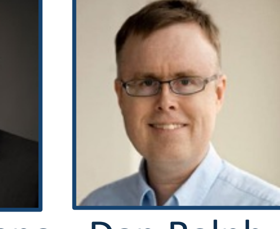
Chris van de Walle

James Rondinelli

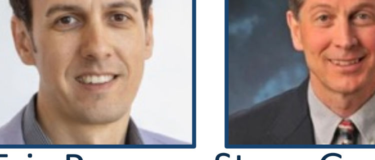
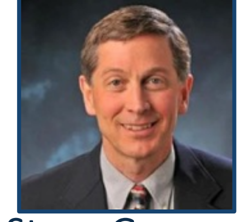
Mike Niemier

James Hwang

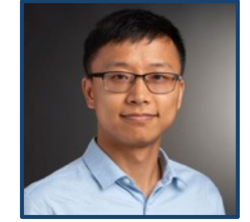

Debdeep Jena


Dan Ralph

Judy Cha



Eric Pop

Steve George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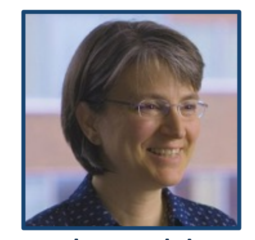
Farnaz Niroui

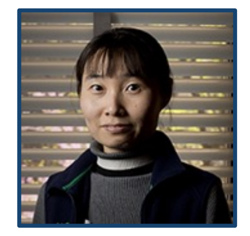
Darrell Schlom

Feliciano Giustino

Asif Khan

Greg Parsons


Hong Tang


Bilge Yildiz

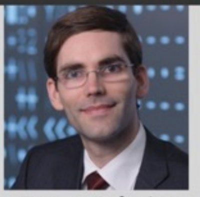
Jing Kong

Luqiao Liu

Organization Chart

Center 7: SUPeRior Energy-efficient Materials and dEvices (SUPREME)

H. Grace Xing[v]
Director


Tomas Palacios
Associate Director

Thomas Dienel
Managing Director

FUNCTIONS

Project, Budget & Conflict Management, Strategic Planning, Annual Meeting Coordination, IP/Spin-off Coordination, Research Development, Reporting

Electrical Engineering · Biology · Material Science · Mechanical Engineering · Computer Science · Physics · Chemistry · Computer Engineering · Neuroscience

Scientific Advisory Board
Visionaries funding a shared technology future

intel · Micron · HRL Laboratories · Raytheon Technologies · Boeing · Samsung · IBM · arm · EMD Electronics · Qorvo · MediaTek · DARPA · Analog Devices · SK hynix · tsmc · GlobalFoundries

FUNCTIONS

Center Evaluation, Strategic Planning and PI Re-alignment, IP Filing Decision, Center to Center Collaboration

Thrust 1: Digital & Analog

Debdeep Jena Thrust Lead

- **Tomas Palacios** (Co-Lead)
- **H. Grace Xing**
- **James Hwang** [1]
- **Farnaz Niroui**^[1v]
- **Luqiao Liu***^

Thrust 2: Memories & Applications

Asif Khan^ Thrust Lead

- **Dan Ralph** (Co-Lead)
- **Kai Ni**^
- **Mike Niemier*** (Liaison Lead)
- **Bilge Yildiz**[1v]

Thrust 3: Interconnects & Metrology

Farhan Rana Thrust Lead

- **Daniel Gall** (Co-Lead)
- **Hong Tang**[1]
- **Judy Cha***^[v]
- **Chris Hinkle**
- **Eric Pop**

Thrust 4: Materials Discovery & Processing

Feliciano Giustino[1]
Thrust Lead

- **Jing Kong**[1v] (Co-Lead)
- **Steven George**
- **Chris Van de Walle**
- **Darrell Schlom***
- **James Rondinelli**
- **Elton Graugnard**
- **Greg Parsons**

* Liaisons to interface with other JUMP 2.0 centers
^ Young Faculty (5)
[1] First-time SRC Performers (6)
[v] Female Faculty (5)

Note: Only primary thrust affiliation is shown.

Cornell University · MIT · Georgia Tech · Notre Dame · RIT · Rensselaer · CU · UCSB · Texas · Yale · NC State · Boise State University · Northwestern University · Stanford University

Cognition

Communication

Smart Sensing

Distributed Systems

Intellegent memory

Seismic Shifts *Bridging the gap and enabling the seismic shifts in ICT.*

Application-level Benchmarking *Meeting the workload demands of the future.*

Machine Learning & Artificial Intelligence
- Hyperdimensional Computing models
- Transformer Networks — GPT-3 and beyond
- Recommendation Systems
- Perception and Autonomy

Associative Memories
- Key Value Storage
- RF Intelligence
- Bioinformatics

Physics-based Computing

Augmented Memory Hierarchy

Impacts of Interconnects

Secure Processing
- Trusted execution environments
- Homomorphic encryption

Devices & Interconnects *Accelerating innovations in Analog, Digital, Memory, & Storage Devices & Interconnects.*

1 Analog & Digital

2 Memory & Applications

3 Interconnects & Metrology

4 Materials Discovery & Processing: *Taming new materials and new physics.*

Accelerated Materials Discovery | **AI-assisted Synthesis & Manufacturing** | **Processing & Metrology**

TMDs $MoSe_2$, WS_2, WSe_2	Nitrides AlScN, ScGaN, BN, InN	Proton electrolyte in electrochemical RAM (ECRAM) - HfO_2, ZrO_2	Synthetic antiferromagnets FeCoB/Pt/Ru/Pt/FeCoB	Oxide interconnect metals $PdCoO_2$, $PdRhO_2$
Conventional semiconductors Si, SiGe, Ge, GaN, SiC	2-D Materials InN, ZnO, SnSe	Ferroelectrics SnS, AlScN, $BaTiO_3$	Proton channnel in ECRAM - MoO_3	Intermetallic interconnect metals VPt_2, $MoNi_2$, $NiIr_3$
Anisotropic spin sources PtO, $Sr_3Ru_2O_7$	Proton reservoir in ECRAM - Metal hydrides, PdH_x	Conductive boride-based interconnect metals - YCo_3B_2, NbFeB, Mn_2B	p-channel oxides Ta_2SnO_6, Ba_2BiTaO_6	Weyl semi-metals, Heusler alloys - Co_2MnGa, Mn_3Sn

Seismic Shifts *Bridging the gap and enabling the seismic shifts in ICT.*

Application-level Benchmarking *Meeting the workload demands of the future.*

Machine Learning & Artificial Intelligence
- Hyperdimensional Computing models
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Associative Memories
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Devices & Interconnects *Accelerating innovations in Analog, Digital, Memory, & Storage Devices & Interconnects.*

1 **Analog & Digital**

2 **Memory & Applications**

Write Gate Reservoir / Electrode Electrolyte Ion Read Source Channel Drain

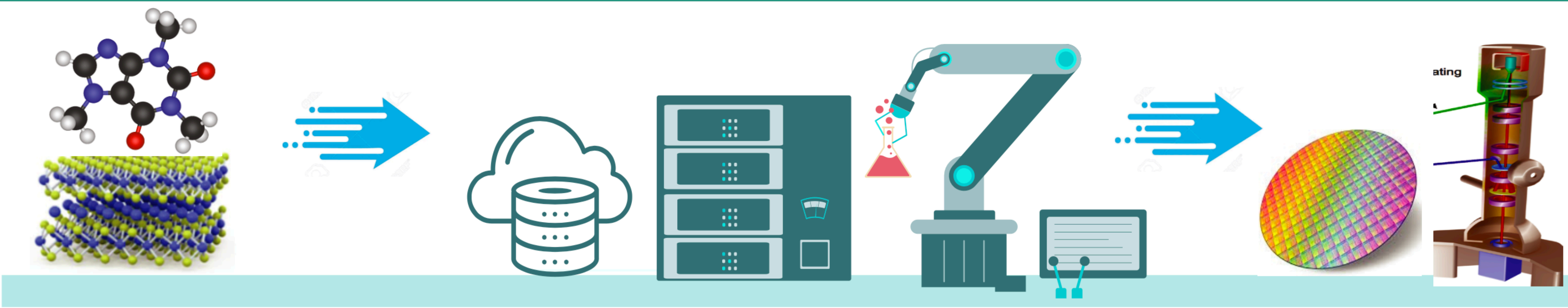
3 **Interconnects & Metrology**

4 **Materials Discovery & Processing:** *Taming new materials and new physics.*

Accelerated Materials Discovery | **AI-assisted Synthesis & Manufacturing** | **Processing & Metrology**

4 **Materials Discovery & Processing:** *Taming new materials and new physics.*

Accelerated Materials Discovery	AI-assisted Synthesis & Manufacturing	Processing & Metrology



TMDs
$MoSe_2$, WS_2, WSe_2

Nitrides
AlScN, ScGaN, BN, InN

Proton electrolyte in electrochemical RAM (ECRAM) - HfO_2, ZrO_2

Synthetic antiferromagnets
FeCoB/Pt/Ru/Pt/FeCoB

Oxide interconnect metals
$PdCoO_2$, $PdRhO_2$

Conventional semiconductors
Si, SiGe, Ge, GaN, SiC

2-D Materials
InN, ZnO, SnSe

Ferroelectrics
SnS, AlScN, $BaTiO_3$

Proton channnel in ECRAM - MoO_3

Intermetallic interconnect metals
VPt_2, $MoNi_2$, $NiIr_3$

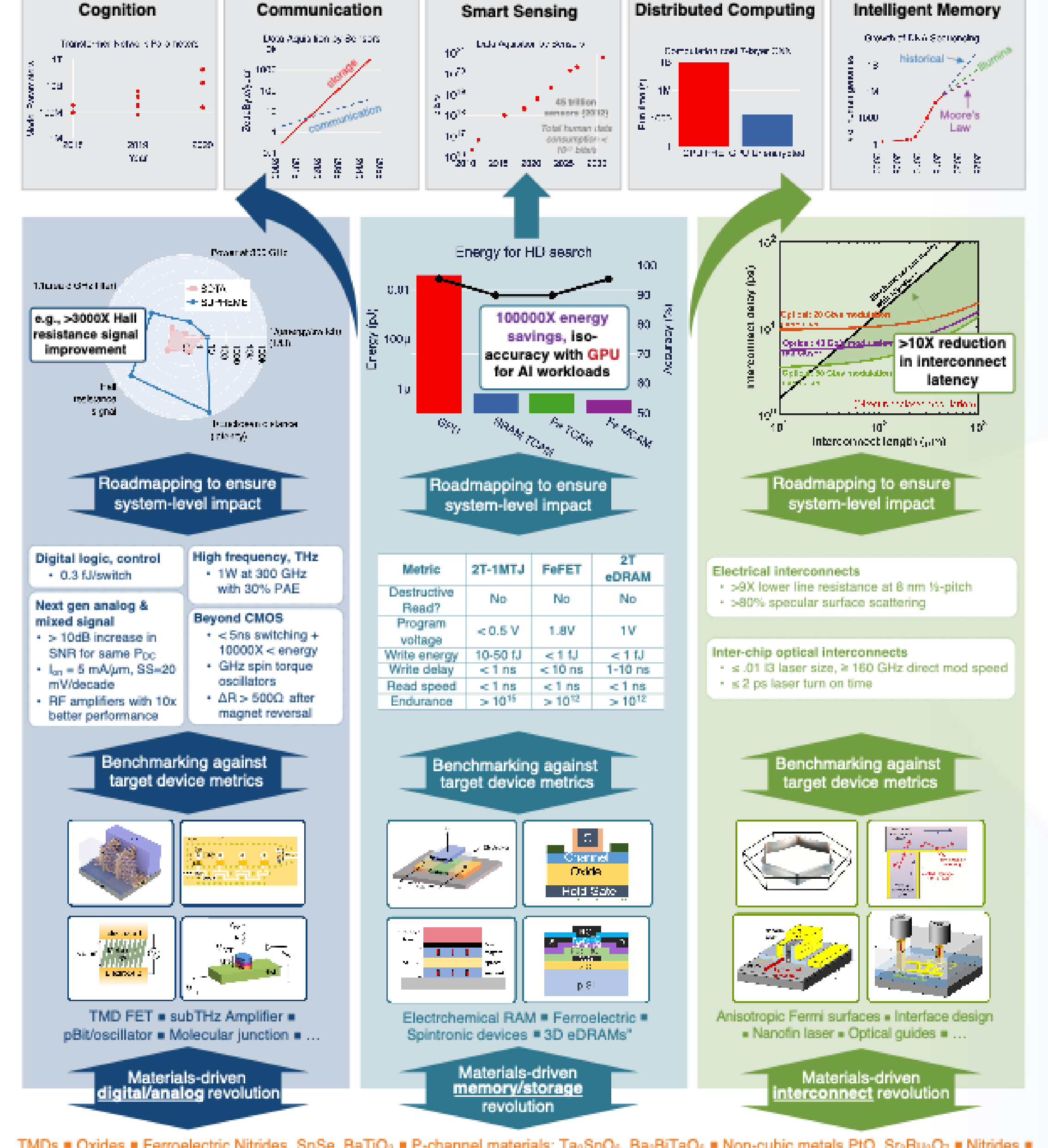
Anisotropic spin sources
PtO, $Sr_3Ru_2O_7$

Proton reservoir in ECRAM - Metal hydrides, PdH_x

Conductive boride-based interconnect metals - YCo_3B_2, NbFeB, Mn_2B

p-channel oxides
Ta_2SnO_6, Ba_2BiTaO_6

Weyl semi-metals, Heusler alloys - Co_2MnGa, Mn_3Sn



TMDs ■ Oxides ■ Ferroelectric Nitrides, SnSe, $BaTiO_3$ ■ P-channel materials: Ta_2SnO_6, Ba_2BiTaO_6 ■ Non-cubic metals PtO, $Sr_3Ru_2O_7$ ■ Nitrides ■ Hydrogen reservoir PdH_2 ■ Heusler Alloys, Weyl semi-metals Co_2MnGa, Mn_3Sn ■ H+ conducting layer: MoO_3 ■ Synthetic antiferromagnets: FeCoB/Pt/Ru/Pt/FeCoB ■ Conductive delafossite oxides: $PdCoO_2$, PtCoO2, $PdRhO_2$ ■ Metallic carbides: Mo_2C, AlVCrC, $TiAl_2Cr_3C_2$ ■ Intermetallic compounds: VPt_2, $MoNi_4$, $NiIr_3$ ■ Conductive borides: YCo_3B_2, NbFeB, Mn_2B ■ Topological semimetals: CoSn, MoP, MoP_2

Materials Discovery and Processing		
Accelerated Materials Discovery	AI-assisted Synthesis and Manufacturing	Processing and Metrology

SRC | SUPREME
SUPeRior Energy-efficient Materials and dEvices

Roadmapping to ensure system-level impact

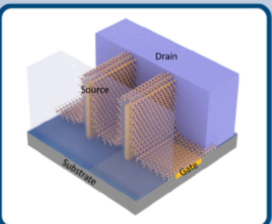
Digital logic, control
- 0.3 fJ/switch

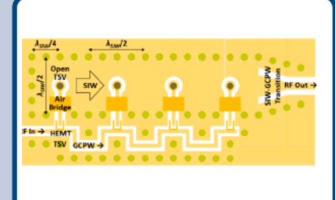
High frequency, THz
- 1W at 300 GHz with 30% PAE

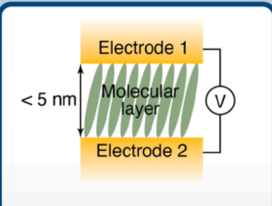
Next gen analog & mixed signal
- > 10dB increase in SNR for same P_{DC}
- I_{on} = 5 mA/μm, SS=20 mV/decade
- RF amplifiers with 10x better performance

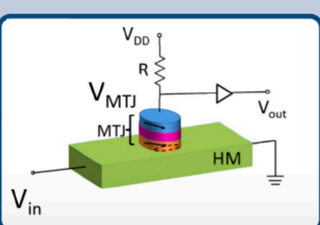
Beyond CMOS
- < 5ns switching + 10000X < energy
- GHz spin torque oscillators
- ΔR > 500Ω after magnet reversal

Benchmarking against target device metrics





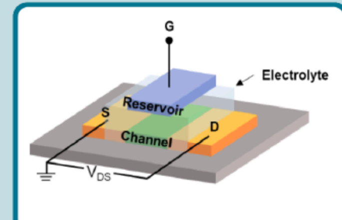


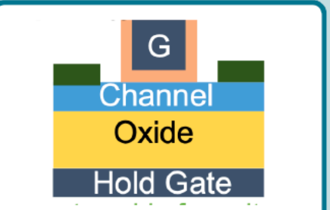


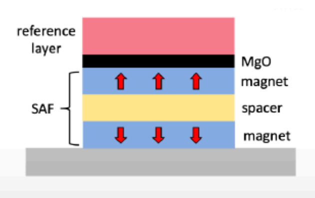
Roadmapping to ensure system-level impact

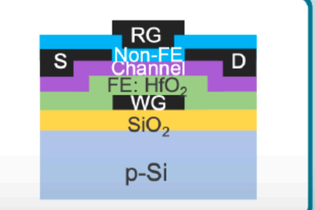
Metric	2T-1MTJ	FeFET	2T eDRAM
Destructive Read?	No	No	No
Program voltage	< 0.5 V	1.8V	1V
Write energy	10-50 fJ	< 1 fJ	< 1 fJ
Write delay	< 1 ns	< 10 ns	1-10 ns
Read speed	< 1 ns	< 1 ns	< 1 ns
Endurance	> 10^{15}	> 10^{12}	> 10^{12}

Benchmarking against target device metrics







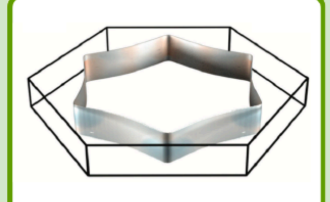


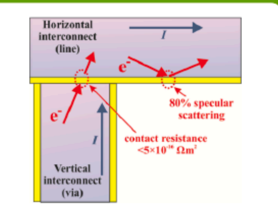
Roadmapping to ensure system-level impact

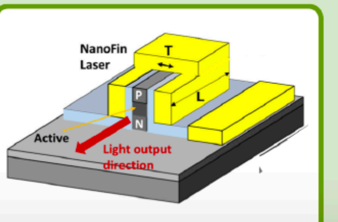
Electrical interconnects
- >9X lower line resistance at 8 nm ½-pitch
- >80% specular surface scattering

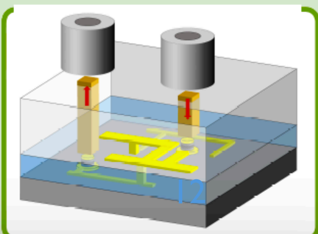
Inter-chip optical interconnects
- ≤ .01 l3 laser size, ≥ 160 GHz direct mod speed
- ≤ 2 ps laser turn on time

Benchmarking against target device metrics





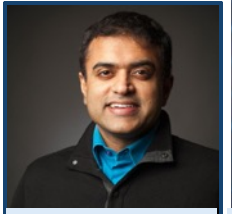
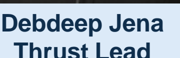




Thrusts & PIs

Thrust 1: Digital and Analog

Thrust 1: PIs and Projects



Debdeep Jena
Thrust Lead

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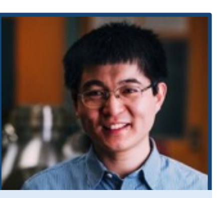
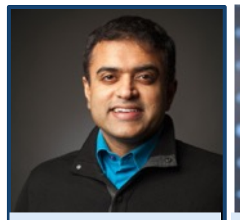

Luqiao Liu

Project 1.1: Digital Logic and Control

Project 1.2: Next Generation Analog And Mixed Signal

Project 1.3: High Frequency and THz Devices

Thrust 1: PIs and Projects



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Project 1.1: Digital Logic and Control

Energy per switching
<0.3 fJ/switch (Task 1.1-1.2, 1.11)

Project 1.2: Next Generation Analog And Mixed Signal

Mixed signal circuits with >10 dB increase in SNR for same P_{DC} (Task 1.3)

Transistors with I_{on}=5 mA/µm and SS=20 mV/dec (Task 1.4)

Project 1.3: High Frequency and THz Devices

RF GaN-on-Si Transistors with beyond GaN-on-SiC performance(Task 1.5)

1 W at 300 GHz with 30% PAE (Task 1.6-1.7)

Project 1.4: Beyond CMOS

GHz spin torque oscillators (Task 1.9)

ΔR>500Ω after magnet reversal (Task 1.10)

<5 ns switching + 10000x lower energy (Task 1.8)

Thrust 1: PIs and Projects

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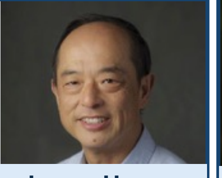

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2D Materials

Tunable Molecules

III-Nitrides

<5 ns switching
+ 10000x lower energy
(Task 1.8)

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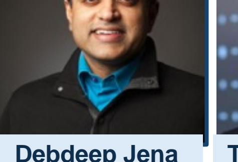
Thrust 1: PIs and Projects


Debdeep Jena
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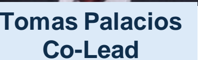
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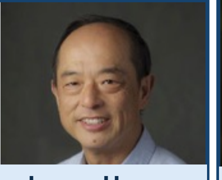
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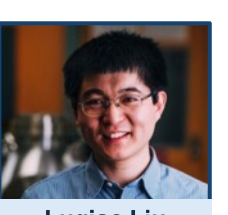
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Project 1.4: Beyond CMOS

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ΔR>500Ω after magnet reversal (Task 1.10)

<5 ns switching + 10000x lower energy (Task 1.8)

Electrostatics + low Temp. synthesis

Spin-to-charge transduction

Dynamic range + large BW

Ultimate scalability

Ferroelectricity

Programmable non-linearities

Seamless Si integration

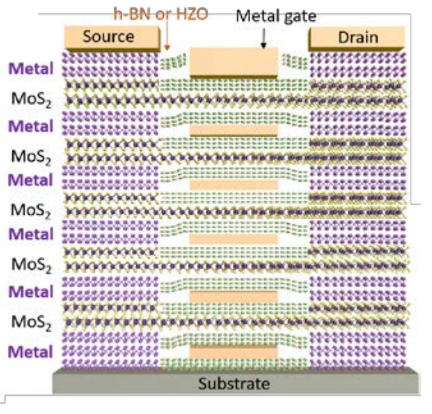
Piezoelectricity

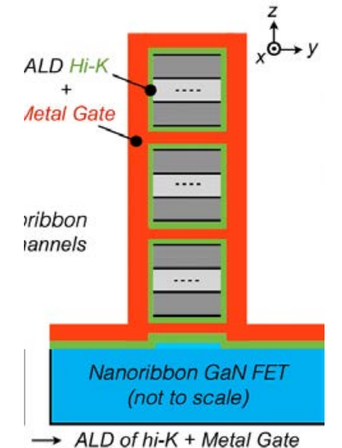
2D Materials

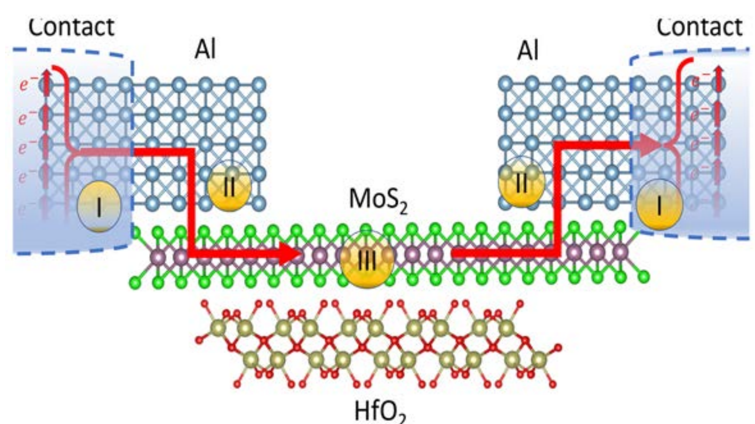
Tunable Molecules

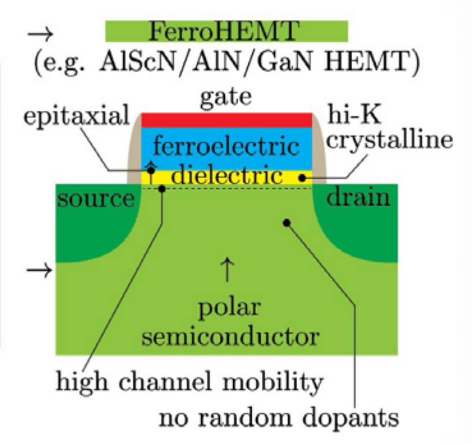
III-Nitrides

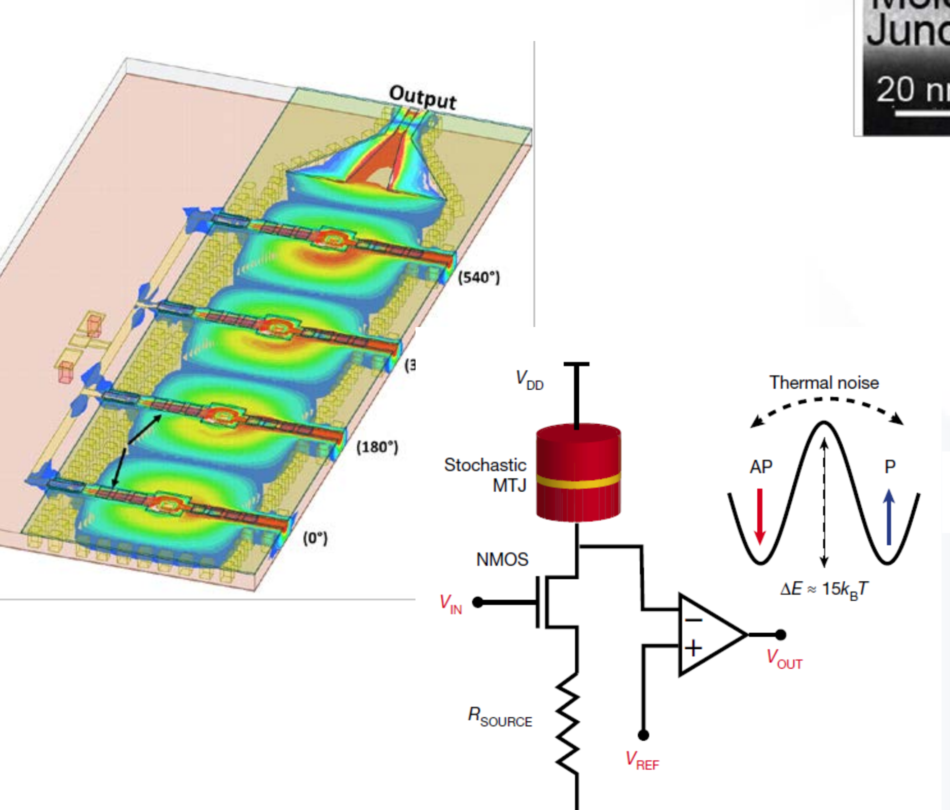
Thrust 1

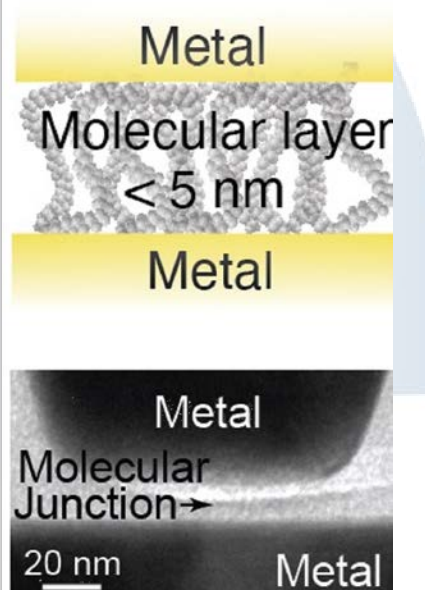


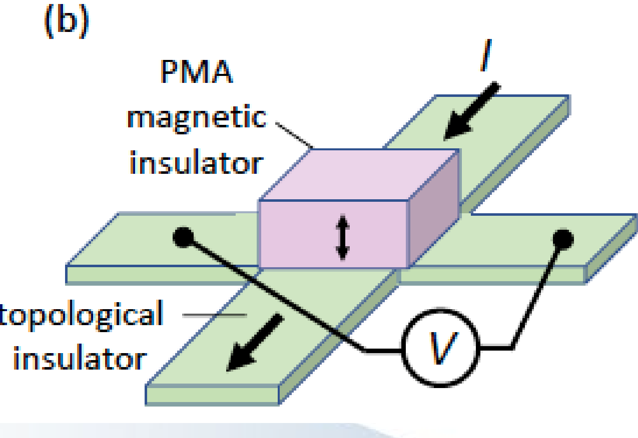












Convergence with CUBIC, COGNISENSE, CHIMES

Theme 3: Wireless Circuits and Technology

Large-Scale Millimeter-Wave Arrays

LAIR

2D-MaSMA

1-bit resolution signal path

CMOS reflective surface

GaN PAs

RE-AIM

InP LNAs

CMOS reflective surface

Wideband High-Dynamic Range Analog Signal Processing Interfaces and High-Dimensional Digital Signal Processing for Emerging Wireless

Hi-SPAR

LPTV spatio-spectral filters and self-interference cancellers

BIRDA

Broadband interference-resilient dynamic arrays

T-SPAR

Time-domain signal processing at RF

OPeRA

Optimized photonic interfaces for mmWave massive MIMO

ADAPT

Adaptive and distributed massive MIMO decoders

PAYGO

Pay as you go FEC decoder

EVO

Ensemble Velocity Overshoot

GoG

Growth on bulk GaN

HiFi

High-K and Ferroelectric Dielectrics

D-Therm

Diamond for Thermal Management

Heterogeneous Technologies for Next Generation Wireless

CUbiC

Antenna

Pixel

1mm

Coupler/ Photodetector

MIMO Correlator

LNA

MIMO Signal Processing

Machine Learning and Adaptation Engine

TIA

Beamformer

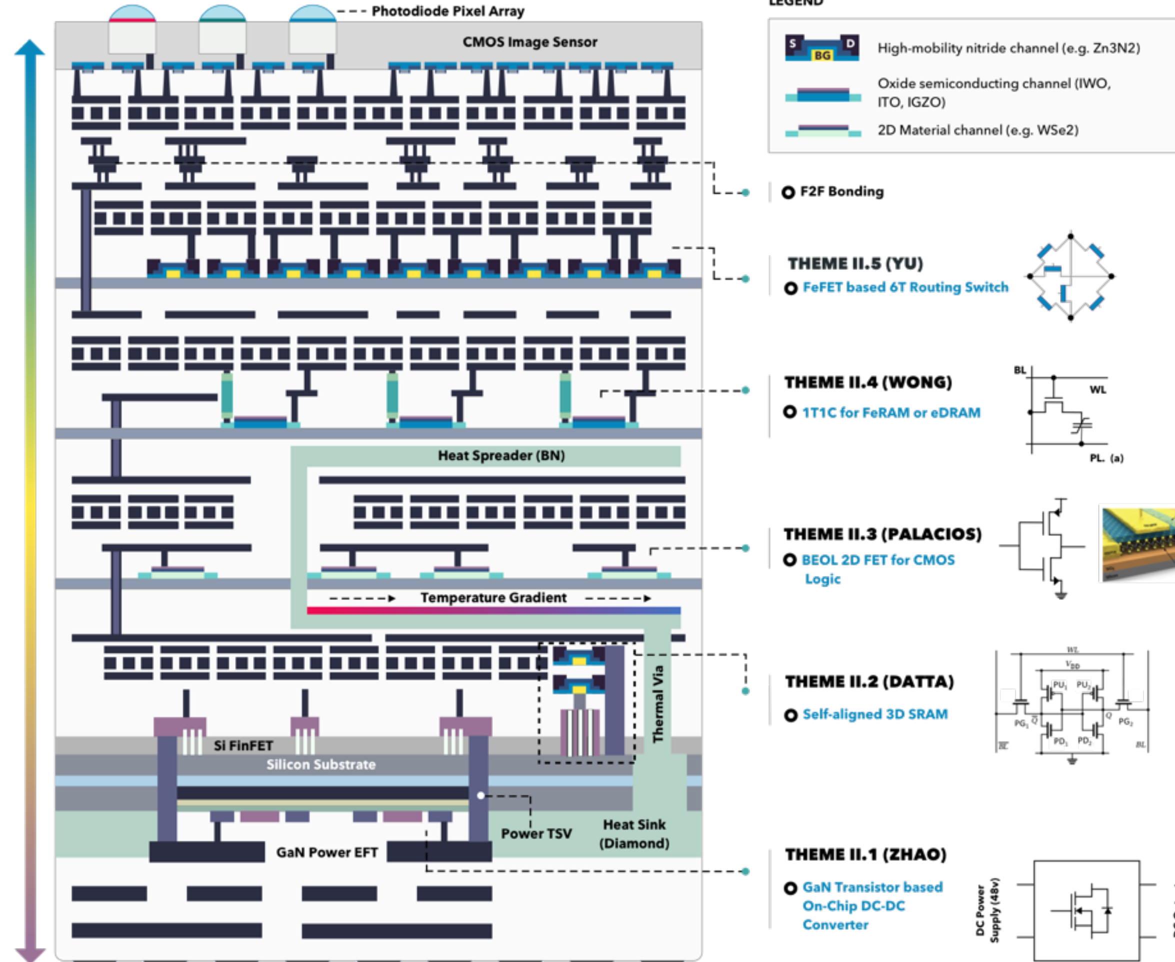
SRC

CogniSense

CENTER ON COGNITIVE MULTISPECTRAL SENSORS

CHIMES CENTER FOR HETEROGENEOUS INTEGRATION OF MICRO ELECTRONIC SYSTEMS

Theme 3: Monolithic 3D (M3D) Densification and Diversification on Silicon Platform

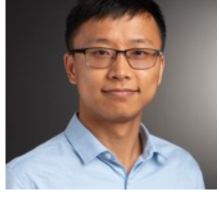


Thrust 2: Memories and Applications

Thrust-2 : Memories and Applications

Niemier

Ni



Khan

Hinkle

Ralph

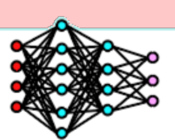
Lu

Rondinelli

Yildiz

Application-level Benchmarking

Machine Learning & Artificial Intelligence



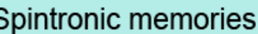
Secure Processing

Associative Memories

Augmented Memory Hierarchy

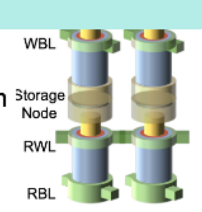
Ferroelectric memories

- Demonstrate write voltage <0.4 V in ALD perovskite ferroelectrics at BEOL and FEOL.
- Novel HfO_2 based FE devices: assymetric DG-FeFETs, MFMIS for high MW.



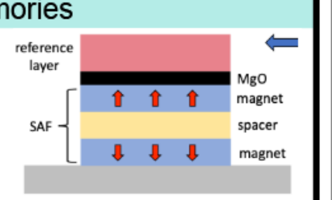
3D eDRAM

- Vertically stacked wide bandgap TFTs.
- 3D 2T0C gain-cell eDRAM with 10^{-19}A/um leakage, 10 uA/um on current, 1000s retention with 100 aF storage capacitor.



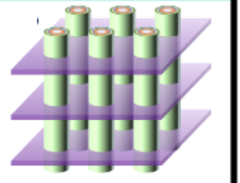
Spintronic memories

- Write energy of ~10 fJ
- TMR > 1000 %
- Immunity to external fields up to 1 Tesla.



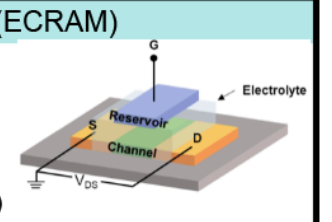
3-D NAND flash

- Conformal MOCVD of monolayer TMDs on the side-wall of punch-hole with mobility >20 cm^2/Vs
- Enable continual XY and Z scaling in vertical 3D NAND flash



Electrochemical RAM (ECRAM)

- Complete CMOS compability with HfO_2-based electrolytic layer
- 1000 analog states
- 10-100 aJ energy per state
  -Scalability down to 10 nm (lateral)



Thrust 4 - Materials Discovery & Processing

Ferroelectrics HfO_2, $BaTiO_3$,SnS	TMDs $MoSe_2$, WS_2, WSe_2	Proton electrolyte in electrochemical RAM (ECRAM) - HfO_2, ZrO_2	Synthetic antiferromagnets FeCoB/Pt/Ru/Pt/FeCoB	Proton channnel in ECRAM - MoO_3
Non-cubic metals PtO, $Sr_3Ru_2O_7$	Weyl semi-metals, Heusler alloys - Co_2MnGa, Mn_3Sn	Proton reservoir in ECRAM - Metal hydrides, PdH_x	Insulator-metal transition materials for selectors $La_{0.5}Sr_{0.5}CoO_{0.3}$, $SrRuO_3$/$LaCoO_3$/$SrRuO_3$	

Task 2.8: Materials-driven application-level analysis

- Objective
  - Couple application-level memory and storage requirements for grand challenge studies in COCOSYS, CUbiC, COGNISENSE, ACE, & PRISM to materials development and discovery
  - Push innovation in SUPREME memories to end-to-end evaluations in other centers
- PI/Collaborators: <u>Mike Niemier (lead)</u>
  - **SUPREME:** Khan, Ralph, Liu, [many other task PIs]
  - **COCOSYS:** Datta, Gupta, Naeemi, Raghunathan, Yu
  - **ACE:** Martinez
  - [continuing to establish links with other centers]
- Innovative claims
  - Metric "ceilings", identification of unique compute capabilities of advanced memory technologies at application-level
- Year 3 accomplishment goals
  - *<u>Representative example with COCOSYS</u>:* ***systematically evaluate MANNs across multiple FOM*** *+ identify, evaluate proxies for transformer, RecSys*

SUPREME
PRISM
SUPREME & PRISM
[cataloging in progress]

JUMP 2.0 Memory Technologies

Device structure

Projected metrics

Materials

Accuracy with Different Approaches

CPU/GPU
Some experimental projections
All experimental

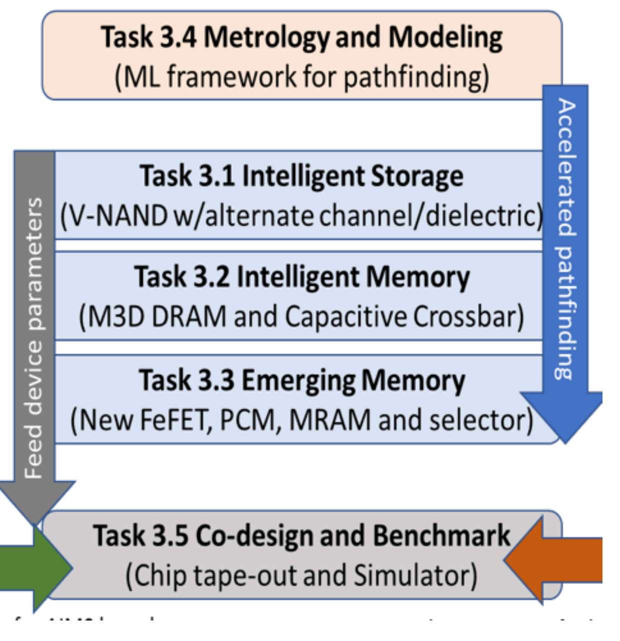
Distance function, attention mechanism

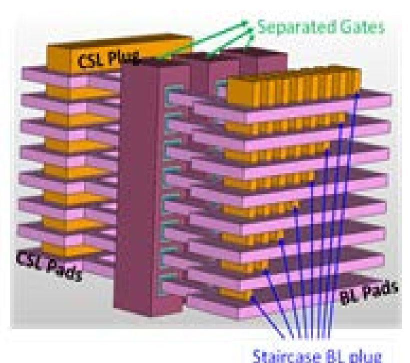
Cosine
Hamming
Euclidean
Sigmoidal
Dot product

Convergence with PRISM, CHIMES & COCOSYS

Processing with Intelligent Storage and Memory

Theme 3: Devices and circuits

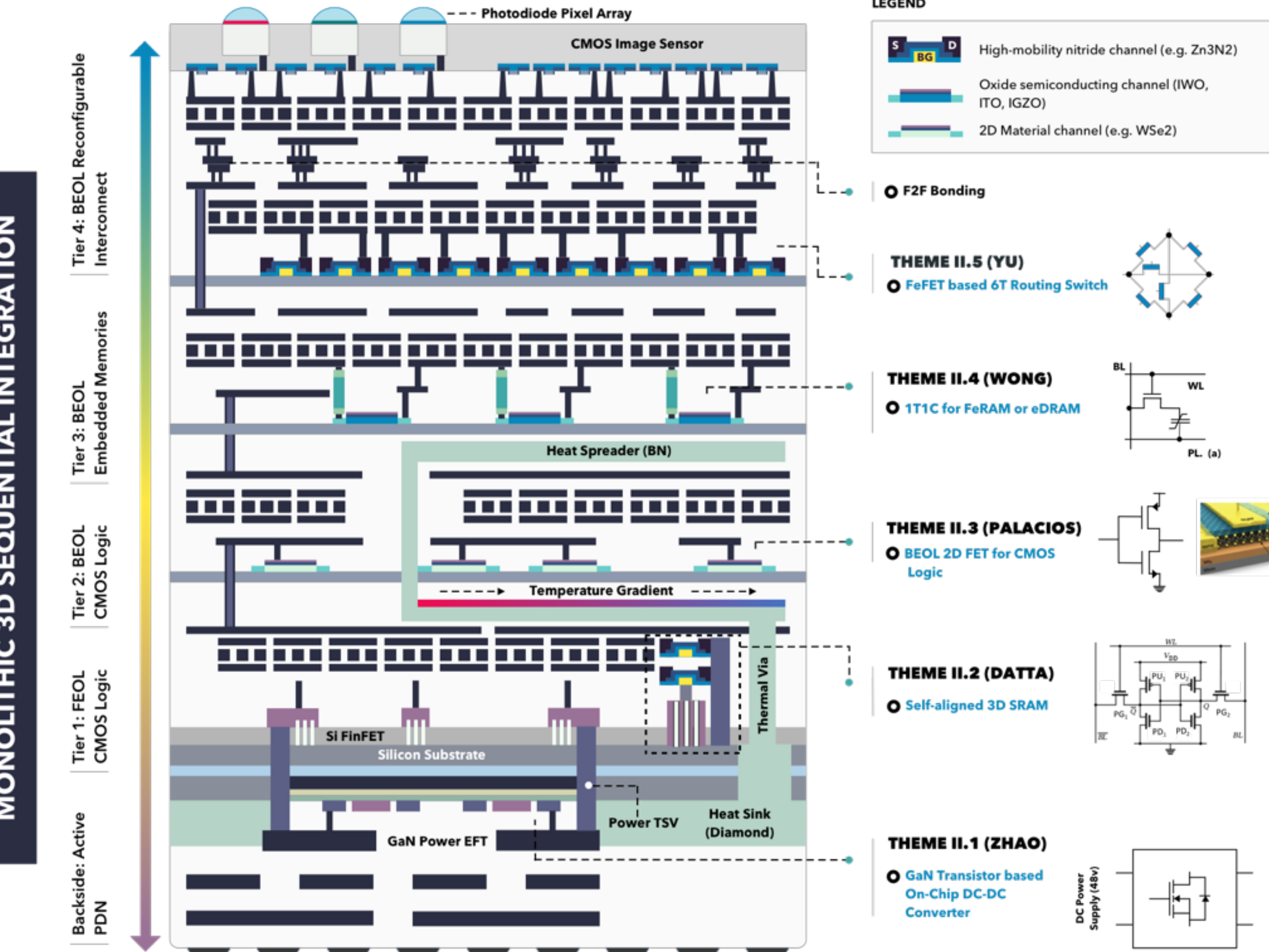




M3D DRAM

CHIMES CENTER FOR HETEROGENEOUS INTEGRATION OF MICRO ELECTRONIC SYSTEMS

Theme 3: Monolithic 3D (M3D) Densification and Diversification on Silicon Platform

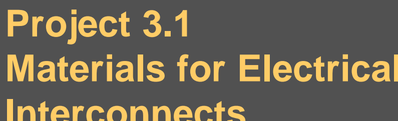


Thrust 3: Interconnects and Metrology

Thrust 3

Thrust 3: Interconnects and Metrology

- New materials: discovery and synthesis
- New processes and devices
- New high-throughput characterization schemes



Project 3.1
Materials for Electrical Interconnects

- Anisotropic Fermi surface conductors
- Topological semimetals
- Engineering metal-metal and metal dielectric interfaces
- Accelerated materials discovery platforms
- Material synthesis

Project 3.2
Materials and Devices for Optical Chip-to-Chip Interconnects

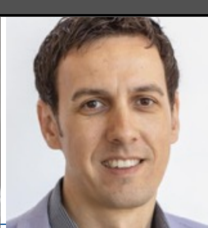
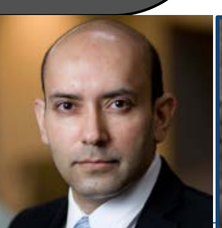
- Nanoscale semiconductor lasers, LEDs, and detectors
- Ultra-compact broadband optical modulators

Project 3.3
Material Characterization and Metrology

- Nanoscale imaging: in-situ TEM studies
- Optical, terahertz, spin resonance characterization
- High-throughput electronic characterization
- Thermal engineering, modeling and characterization
- Surface and interface characterization

Project 3.4
Interconnect Benchmarking

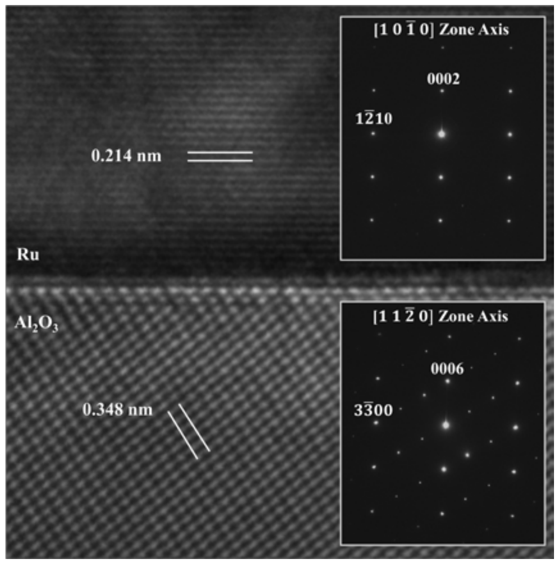
- Benchmark new interconnect ideas with respect to system level performance benefits

Task 3.1 Materials discovery and benchmarking for interconnects ≤ 8 nm

- Objective
  - Materials discovery/benchmarking
  - Demonstrate interconnect solution which outperforms Ru, Cu, Co
- PI/Collaborators:
  - Daniel Gall (lead); Tang, Cha, Rana
- Innovative claims
  - *In situ* measurements of intrinsic resistivity scaling
  - Directional conductors
  - Synthesize theoretically predicted conductors
- Year 3 accomplishment goals
  - Quantify resistivity scaling in boride, oxide, and directional conductors.
  - Blanket layer stack with >1.5x10^{15} Ω^{-1}m^{-2}.

Epitaxial Layers

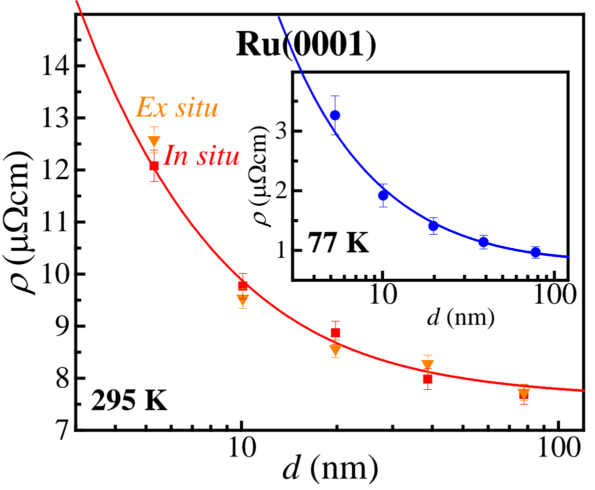


Directional conductors

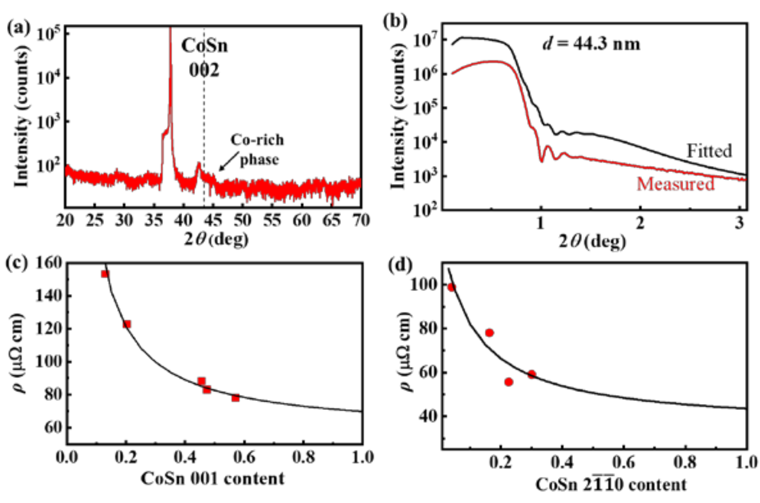
5×10^5 m/s
v_f
0

Predicted Fermi surface of Cr_2AlC

***In situ* Transport**



Explore new materials (e.g. CoSn)



Task 3.4: Materials and Designs for Nanoscale Light Sources

- Objective
  - Materials and designs for nanoscale semiconductor lasers and LEDs for chip-to-chip optical interconnects
- PI/Collaborators:
  - Farhan Rana (lead); Jing Kong, Hong Tang, Mike Niemier, Xing/Jena, CHIMES PIs
- Innovative claims
  - Use new materials for BEOL integration: e.g. 2D materials
  - Use new materials for lower optical losses: e.g. transition metal nitrides
  - Benchmark system level performance gains
- Year 3 accomplishment goals
  - Direct current modulation with CMOS electronics
  - > 80 Gb/s data rates, < 5 fJ/bit EO transduction, & < 0.1 sq-microns footprint
  - Highly directional output

State of the art (not compact and power hungry) ➔ new designs

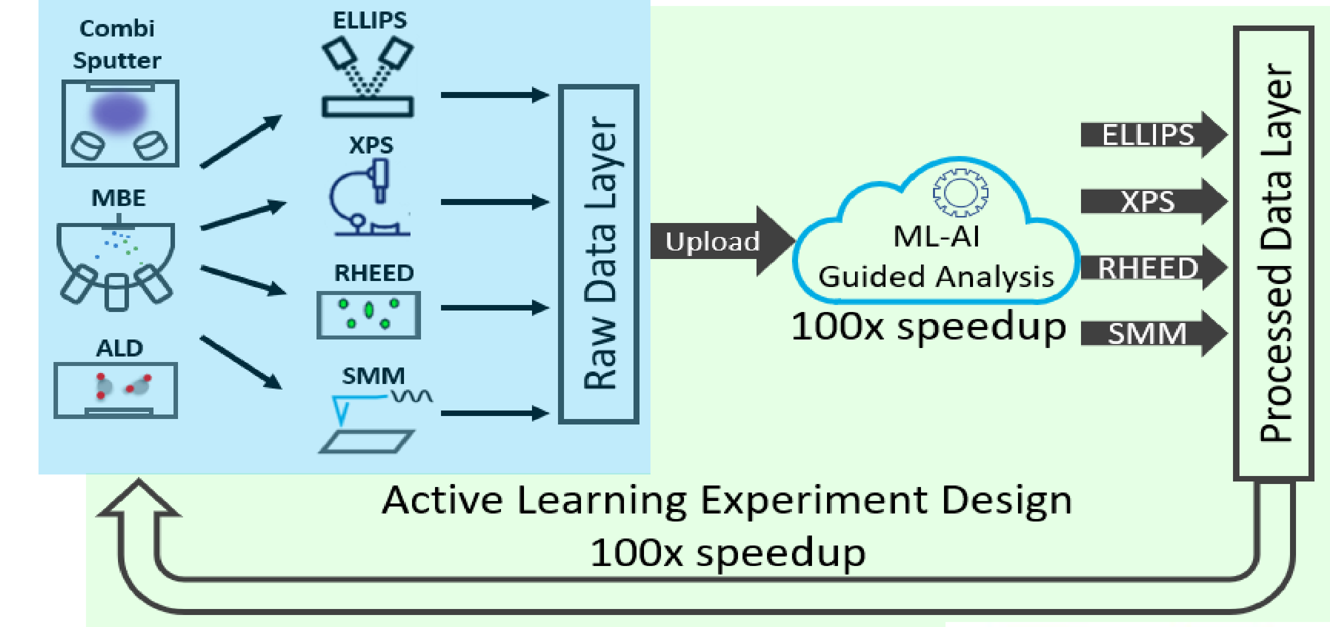
CPU/GPU/ FPGA/ASIC
Electrical I/O
Optical-electrical interface chip
Optical power
Light sources (DFB arrays, multiwavelength lasers)
Optical I/O
a)

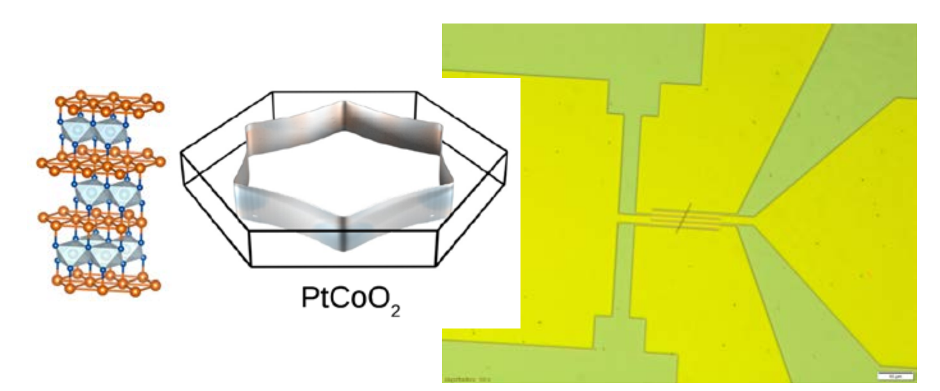
CPU/GPU/ FPGA/ASIC with optical I/O
Optical I/O
b)

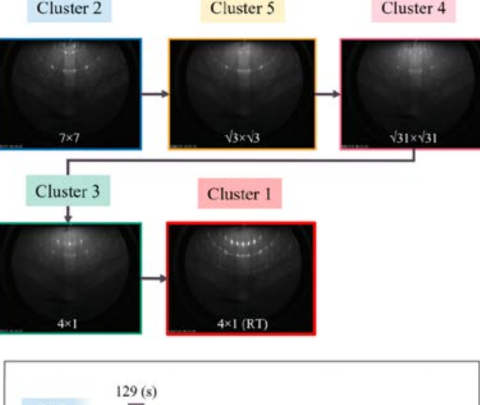
Optical fiber
Optical via
Metal
Nanopatch Laser
Nanopatch detector
Electrical via
IMD
Substrate

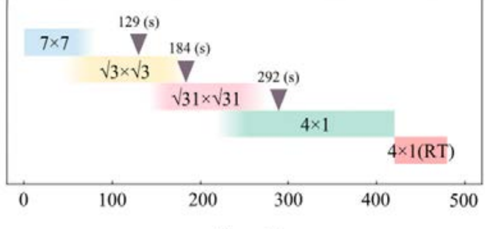
Task 3.10 Accelerated Materials Platform and Interconnects

- Objective
  - Develop high-throughput materials synthesis and characterization techniques
  - Make new interconnects that can outperform Cu and Ru at scaled dimensions
- PI/Collaborators:
  - Chris Hinkle (lead); Rondinelli, Gall, Cha, Pop
- Innovative claims
  - 10-100x speedup in materials synthesis/characterization
  - Active learning experiments with ML-guided materials characterization
  - New interconnects predicted by high-throughput and de novo theory
- Year 3 accomplishment goals
  - ML-guided diffraction, XPS, ellipsometry, scanning microwave impedance microscopy
  - Interconnect materials with lower resistivity than Cu and Ru at < 200 nm^2 conductor area



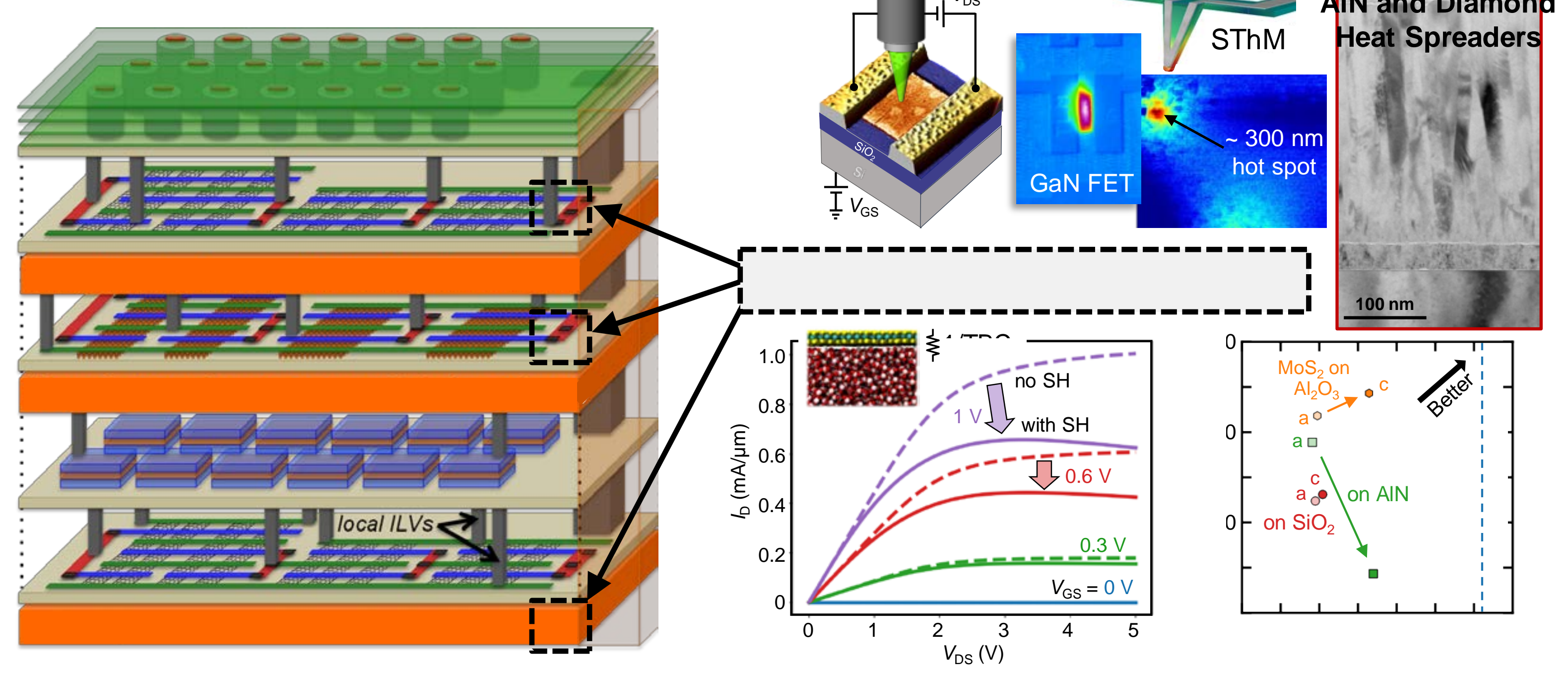






Task 3.11: Thermal Engineering & Materials for 3D Integration

- Objective
  - Electro-thermal co-design of materials, devices, interconnects
- PI/Collaborators:
  - Eric Pop (lead); Hinkle (mater.), Giustino (model), Xing, Gall, Cha, Theme 6 Center
- Innovative Claims:
  - Thermal modeling of 2D and RF transistors + topological interc.
  - Unique thermal measurement capability (Raman, SThM)

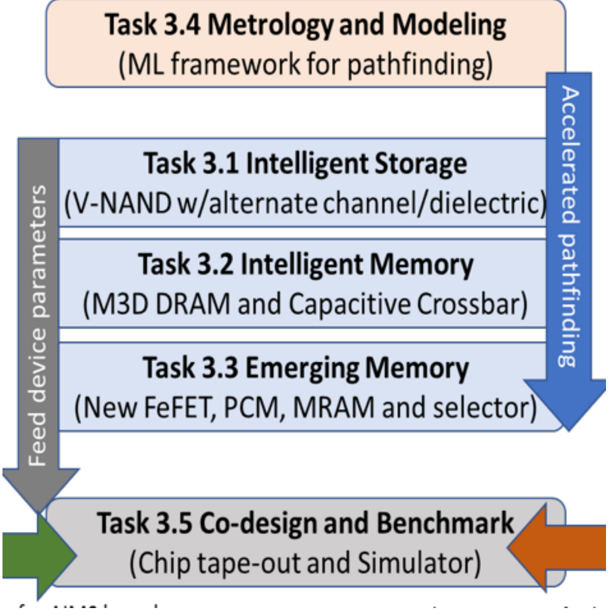


- Year 3 Accomplishment Goals:
  - Electro-thermal model of 2D and RF transistors, including finite-element and (approximate) analytic models
  - Clear guidelines for optimization of heat spreading, e.g. material property vs. thermal boundary resistance

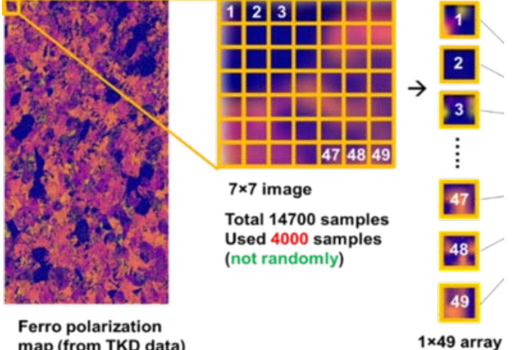
Convergence with PRISM & CHIMES

Processing with Intelligent Storage and Memory

Theme 3: Devices and circuits

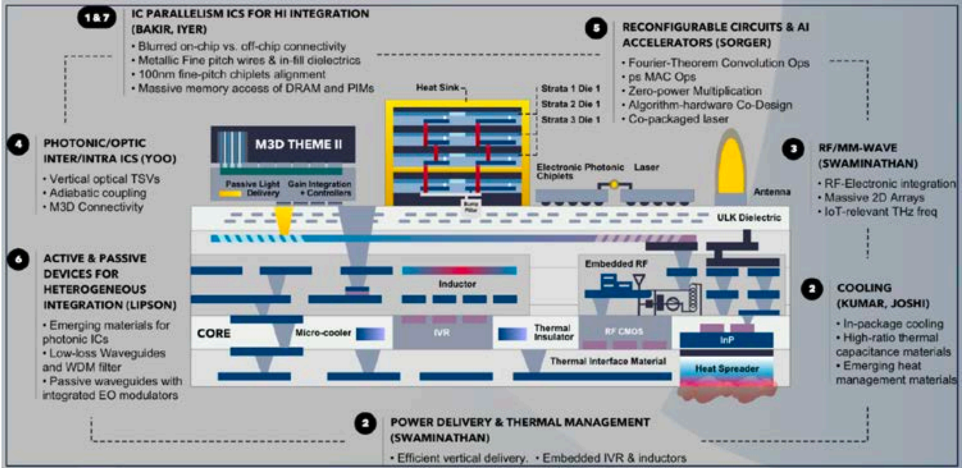


Metrology

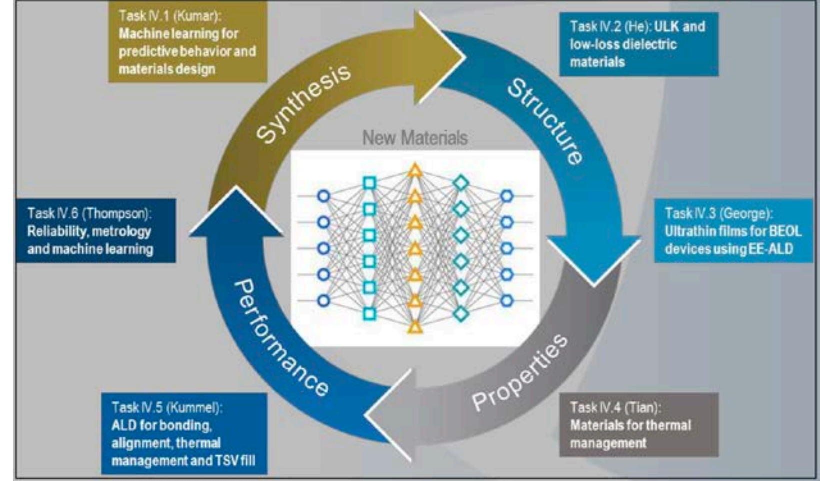


CHIMES CENTER FOR HETEROGENEOUS INTEGRATION OF MICRO ELECTRONIC SYSTEMS

Theme III: Ultra-dense Heterogeneous Interconnect & Assembly



Theme IV: Materials Behavior, Synthesis, Metrology & Reliability



Thrust 4: Materials Discovery and Processing

Thrust 4 Investigators and relation to Center

Center 7: SUPeRior Energy-efficient Materials and dEvices (SUPREME)

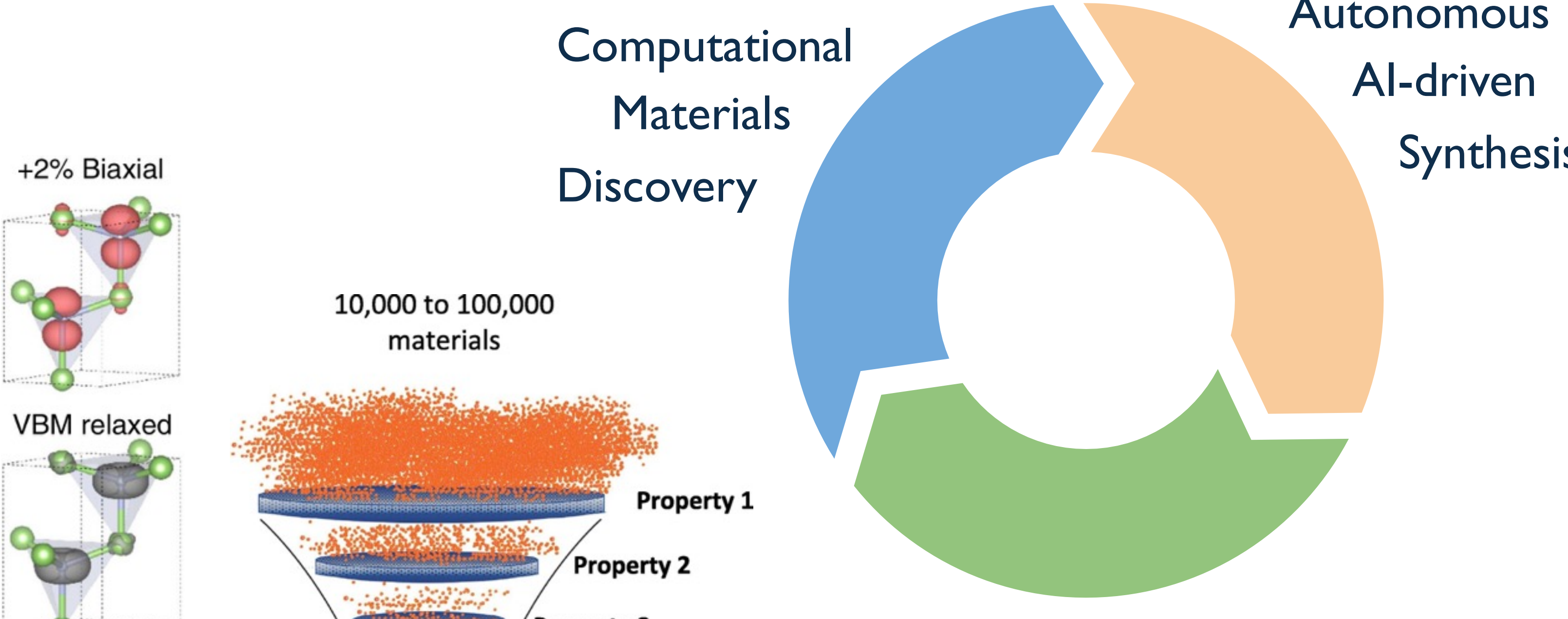
Thrust 1: Digital & Analog	Thrust 2: Memories & Applications	Thrust 3: Interconnects

Thrust 4: Materials Discovery & Processing

Lead	Feliciano Giustino	UT Austin	Co-Lead	Jing Kong	MIT
	Chris Van de Walle	UCSB		Steven George	UC Boulder
	James Rondinelli	Northwestern		Elton Graugnard	Boise State
	Debdeep Jena	Cornell		Darrell Schlom	Cornell
	Bilge Yildiz	MIT		Greg Parsons	NCSU
	(Theorists)			(Experimentalists)	

Thrust 4 Vision & Mission

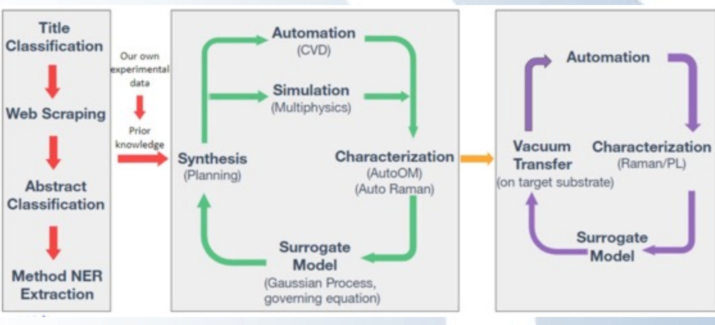
Materials Discovery & Advanced Processing

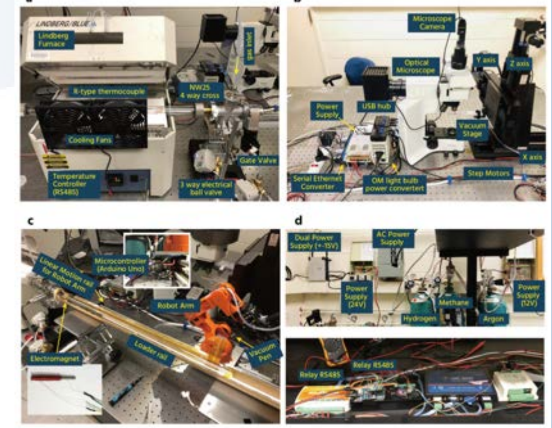


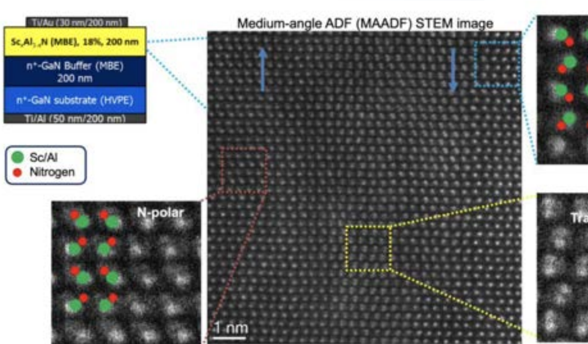
-2% Biaxial

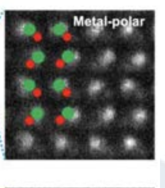
Property 2
Property 3
Property 4
Property 5

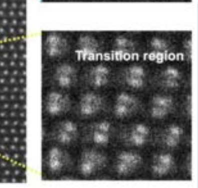
10 to 100
materials
candidates

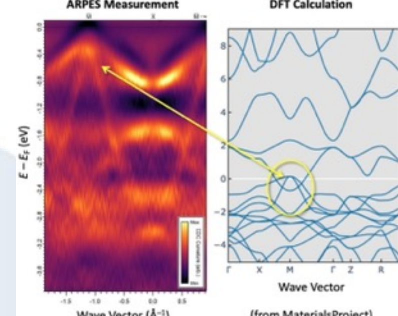












Thrust 4 Vision & Mission

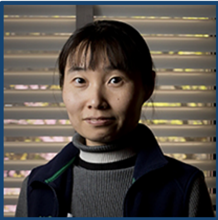
Materials Discovery

Leads

Team meetings
TBD

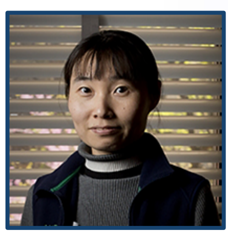
Workshop (TBD)

High throughput



Advanced Processing

Leads



Team meetings
Every Monday at 3:30pm ET

Workshop (TBD)

In the context of devices

Thrust 4 Topics

13 tasks focusing on 4 classes of materials

2D Materials (e.g. TMDs and more)

Large Gap Channel Materials (e.g. GaN, oxides)

New Ferroelectrics, high-K and Nonlinear Materials (e.g. AlScN, perovskite oxides)

Ionic materials for Electrochemical RAMs (oxides, oxynitrides, etc)

Thrust 4 Tasks

2D Materials	Ferroelectric & nonlinear materials
Large gap channel materials	Ionic synapses

Task	Description	Lead
Task 4.1	High-throughput discovery of high-mobility 2D channel materials	Giustino
Task 4.2	High-quality 2D materials discovery and growth via BEOL compatible approaches	Kong
Task 4.3	Artificial Intelligence-Assisted Synthesis and Integration Optimization of 2D Materials (eg G/BN)	Kong
Task 4.4	Controlled Etching of 2DTMD Films Using Electron-EnhancedAtomic Layer Etching with Reactive Background Gas	George
Task 4.5	Discovery of high mobility p-type nitride semiconductors for wide bandgap CMOS (eg GaN)	Jena
Task 4.6	*n*-type and *p*-type oxide channel materials for complementary transistor technology (eg PdO)	Schlom
Task 4.7	AlScN and related alloys as nonlinear optical and piezoelectric materials	Van deWalle
Task 4.8	New ferroelectric and High-K materials (theory, epitaxy, and ALD)	Jena
Task 4.9	Discovery of channel materials with the highest sensitivity of electronic conductivity to proton insertion	Yildiz
Task 4.10	BEOL Area-Selective Atomic Layer Deposition of Conformal Crystalline 2D Materials (egTMDs)	Graugnard
Task 4.11	Atomic Layer Deposition of Ultrahigh-k Dielectrics (eg BaHfO3)	Graugnard
Task 4.12	Inherent Selective Atomic Scale Processing	Parsons
Task 4.13	Active and Physics-Informed Machine Learning for Accelerated Materials Discovery (eg ME/FE oxides)	Rondinelli

Convergence with PRISM & CHIMES

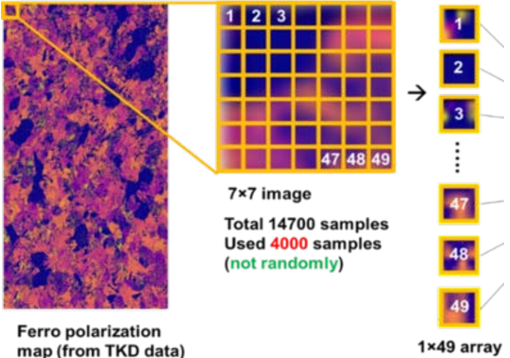
Processing with Intelligent Storage and Memory

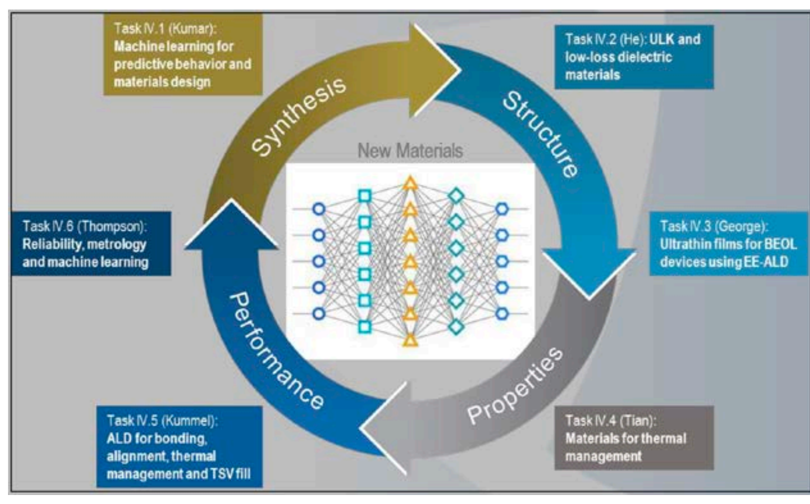
Theme 3: Devices and circuits

CHIMES CENTER FOR HETEROGENEOUS INTEGRATION OF MICRO ELECTRONIC SYSTEMS

Theme IV: Materials Behavior, Synthesis, Metrology & Reliability

Metrology

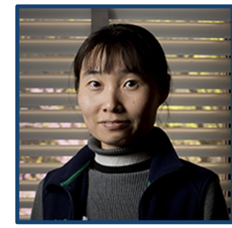
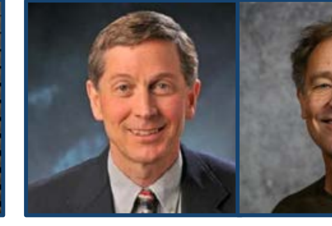
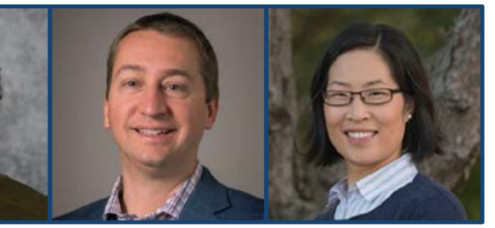




Advanced Processing – a Inter-Center Topic

Elton Graugnard

SUPREME PIs

& PRISM PIs & CHIMES PIs

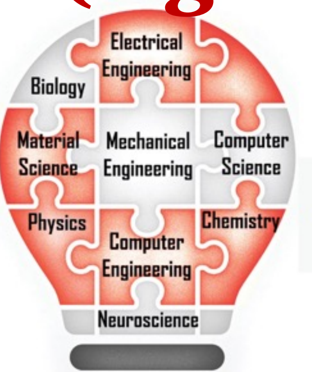
Workshop (TBD)

Organization Chart: SUPREME Thrust-Liaison Meetings on every Wednesday@4pm ET (sign up for SUPREME task)

H. Grace Xing[v] Director | Tomas Palacios Associate Director | Thomas Dienel Managing Director

FUNCTIONS

Project, Budget & Conflict Management, Strategic Planning, Annual Meeting Coordination, IP/Spin-off Coordination, Research Development, Reporting



Scientific Advisory Board

Visionaries funding a shared technology future

intel, Micron, HRL Laboratories, Boeing, Samsung, IBM, arm, EMD Electronics, qorvo, MediaTek, DARPA, Analog Devices, SK hynix, tsmc

FUNCTIONS

Center Evaluation, Strategic Planning and PI Re-alignment, IP Filing Decision, Center to Center Collaboration

Thrust 1: Digital & Analog

Debdeep Jena Thrust Lead

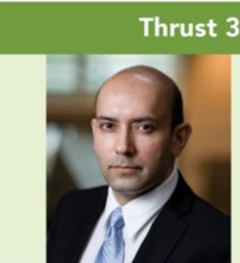
- **Tomas Palacios** (Co-Lead)
- **H. Grace Xing**
- **James Hwang** [1]
- **Farnaz Niroui**^[1v]
- **Luqiao Liu***^

Thrust 2: Memories & Applications

Asif Khan^ Thrust Lead

- **Dan Ralph** (Co-Lead)
- **Kai Ni**^
- **Mike Niemier*** (Liaison Lead)
- **Bilge Yildiz**[1v]

Thrust 3: Interconnects & Metrology



Farhan Rana Thrust Lead

- **Daniel Gall** (Co-Lead)
- **Hong Tang**[1]
- **Judy Cha***^[v]
- **Chris Hinkle**
- **Eric Pop**

Thrust 4: Materials Discovery & Processing

Feliciano Giustino[1] Thrust Lead

- **Jing Kong**[1v] (Co-Lead)
- **Steven George**
- **Chris Van de Walle**
- **Darrell Schlom***
- **James Rondinelli**
- **Elton Graugnard**
- **Greg Parsons**

* Liaisons to interface with other JUMP 2.0 centers
^ Young Faculty (5)
[1] First-time SRC Performers (6)
[v] Female Faculty (5)

Note: Only primary thrust affiliation is shown.

Cornell University, MIT, Georgia Tech, Notre Dame, RIT, Rensselaer, Colorado, UCSB, Texas, Yale, NC State, Boise State University, Northwestern University, Stanford University

Seismic Shifts *Bridging the gap and enabling the seismic shifts in ICT.*

Application-level Benchmarking *Meeting the workload demands of the future.*

Machine Learning & Artificial Intelligence
- -Hyperdimensional Computing models
- -Transformer Networks — GPT-3 and beyond
- -Recommendation Systems
- -Perception and Autonomy

Associative Memories
- -Key Value Storage
- -RF Intelligence
- -Bioinformatics

Physics-based Computing

Augmented Memory Hierarchy

Impacts of Interconnects

Secure Processing
- -Trusted execution environments
- -Homomorphic encryption

Devices & Interconnects *Accelerating innovations in Analog, Digital, Memory, & Storage Devices & Interconnects.*

1 **Analog & Digital**

2 **Memory & Applications**

Write Gate Reservoir / Electrode Electrolyte Ion Read Source Channel Drain

3 **Interconnects & Metrology**

4 **Materials Discovery & Processing:** *Taming new materials and new physics.*