STUDENTS' CATALOG

Student name	Photo	Email	Advisor name	Available for hire date	Poster title	Abstract	Additional authors (if any)
Pradyot Yadav		yadavps@mit.edu	Tomas Palacios	Summer 2024 Internship/ Summer 2027 Full Time	Heterogeneous Integration of GaN and Si CMOS for W-Band 3D Integrated RF Front Ends	3HI of Gallium Nitride and Si CMOS for Next-Gen Communications Systems	-
Kad Kook		dkook3@gatech.edu	Satish Kumar	Summer 2025 Internship Fall 2027 Full Time	Machine Learning to Develop Process-Structure-Property Relations for hBN Thin-film	Efficient and Interpretable Gaussian Process Regression by Applying Linear Combination toward High Dimensional Vectors	-
Zachary Sobell		zaso6688@colorado.edu	Steven George	Spring 2024 Full Time	Electron-Enhanced Atomic Layer Deposition (EE-ALD) of Tunable Ternary Nitride Diffusion Barriers	Low temperature deposition of ultrathin TiCN diffusion barriers with tunable C content by EE-ALD with an NH_3 reactive background gas.	Andrew Cavanagh
Mingeun Choi		mingeun.choi@gatech.edu	Satish Kumar	Fall 2027 Full Time	Thermal Analysis of High Current Vertical Power Delivery Architectures	Numerical Simulation of On-Interposer GaN-based Vertical Power Delivery Architecture with DPMIH Converters	-

Uttara Chakraborty		uttara@mit.edu	Carl Thompson, Duane Boning	Summer 2024 Internship / 2025 Full Time	Identification of Multiple Failure Mechanisms for Reliability using Differential Evolution	We develop a differential evolution framework to identify more than one failure mechanism from both synthetic and real reliability data for packages and circuits. Our method outperforms the state of the art on various metrics in a statistically significant way.	Duane Boning
Jiyoung Kim		jk2626@cornell.edu	Zhiting Tian	Summer 2027 Full Time	Thermal Isolation Performance of Polyimide Aerogel within Die-embedded Glass Interposer	Verification of application of polyimide aerogel to a die-embedded glass interposer	-
Shuhan Liu		shliu98@stanford.edu	H.-S. Philip Wong	Summer 2024 Internship	Hybrid Gain Cell: ITO FET Integrated on 40nm CMOS for On-chip Memory with High Speed and Large Capacity	Monolithic 3D integration of oxide semiconductor FET with Si FET for hybrid gain cell memory	-

Russell Schwartz		rschwartz2@ufl.edu	Volker Sorger	Summer 2026 Full Time	Laser Integration on Photonic Tensor Cores	The process and results of integrating III-V lasers with photonic tensor cores using photonic wire bonds to enable high throughput, low latency accelerators	Nicola Peserico
Xiaofan Jia		xjia48@gatech.edu	Madhavan Swaminathan	Fall 2023 Full Time	Die-embedded glass packaging for FutureG wireless communications	This poster presents the latest advancements in integrating the 140 GHz InP power amplifiers with glass interposer for the 6G wireless communications. We address the electrical and thermal challenges that arise from heterogeneous integration by developing embedded die packaging technologies using glass substrates.	-
Shisong Luo		sl187@rice.edu	Yuji Zhao	Summer 2024 Internship/Summer 2027 Full time	GaN Transistor for On-Chip Power Delivery Network	GaN n channel and p channel transistors for integration circuits	Zhaobo Mei, Mingfei Xu

Lingjun Zhu		lingjun@gatech.edu	Callie Hao	Spring 2024 full time	Heterogeneous 3D Integration Design Flow and Thermal Analysis	In this study, we develop a customized physical design flow to enable heterogeneous 3D integration and show the PPA and thermal benefits.	-
Hae Won Lee		hw93528@mit.edu	Tomas Palacios	Summer 2025 Internship/ Fall 2027 Full Time	BEOL Integration of TMD-based CMOS Logic and Photonic Devices	Low temperature growth technology of TMDs for the integration of TMD devices on flexible substrate and contact engineering for TMD devices	-
Ramin Rahimzadeh Khorasani		rbr5373@psu.edu	Madhavan Swaminathan	Summer 2024 Internship/	Efficient Architecture for 48-1 V IVR	Presenting an efficient single-stage, multi-phase architecture for integrated voltage regulator module (IVR) converting 48 V input to 1 V. Achieved significant inductor reduction	-

						(0.5-25 nH) for high-power, high-frequency IVR (Output power 1 kW, Switching frequency 1-5 MHz). Eliminated switching and capacitive turn-on losses, enhancing efficiency, and reducing GaN FETs temperature.	
Myriam Bouzidi		mbouzidi3@gatech.edu	Suresh Sitaraman	Summer 25 (Internship)/ Summer 26 Full Time	Flexible, Multifunctional Thermal Management and Electro-Thermal Modeling for Ultra-Compact High-Power Density Systems	A novel cooling solution that will use a capillary-driven flow for thin film evaporation to address heat removal challenges in high-power density systems. The proposed solution targets 2kW/cm^2 of heat rejection and will aim to accommodate differences in topology within a single architecture.	Dr. Im Yunhyeok
Pruek Vanna-Iampikul		v.pruek@gatech.edu	Callie Hao and Sung Kyu Lim	Summer 2024 Full Time	Glass Interposer Integration of Logic and Memory Chiplets: PPA and Power/Signal Integrity Benefits	Explore the benefit of 3D die stacking in glass in a full-chip system.	-

Omkar Phadke		omkarphadke@gatech.edu	Shimeng Yu	Summer 25 Internship	Study of Low-Frequency Noise Characteristics of Back-End-of-Line W-doped In2O3 MOSFET and FeFET	Investigating the Effect of DC Stress on noise response of BEOL Compatible MOSFET and FeFET	-
George Karfakis		georgekarfakis@ucla.edu	Puneet Gupta	Summer 2024 Internship/ 2028 full time	Investigating Thermal Coupling in Heterogeneous Integrated Systems	A methodical investigation of different thermal coupling approaches in 2.5D heterogeneous systems using a novel simulator. Very promising results achieved with split heatsink topologies.	-
Gangchen Ren		gr354@cornell.edu	Zhiting Tian	Summer 2024 internship/ 2027 full time	Vertically Aligned Polyethylene Fibers for Enhanced Thermal Conductivity	Vertically aligned polyethylene demonstrates surprisingly high thermal conductivity which can be a promising candidate for TIM.	-
Janak Sharda		jsharda3@gatech.edu	Shimeng Yu	Summer 2024 internship/2026 full-time	Design and Thermal Analysis of 2.5D and 3D Integrated Package of a CMOS Image Sensor and a Sparsity-Aware Processor for Autonomous Driving	Thermal-aware co-design of a 2.5D and 3D package of a frontend CMOS Image sensor and a backend accelerator capable of performing multi-object tracking on QDTrack network	Madison Manley, Ankit Kaul, Wantong Li, Muhannad Bakir

						for autonomous driving.	
Madison Manley		madison.manley@gatech.edu	Muhannad Bakir	Summer 2024 internship/2025 full time	Towards Selective Cobalt Atomic Layer Deposition for 3D Heterogeneous Integration	Using selective Co ALD for fine pitch Cu-Cu interconnects	Victor Wang, Chenghsuan Kuo
Jungyoun Kwak		jkwak38@gatech.edu	Shimeng Yu	Summer 2026 full	A Reconfigurable Monolithic 3D DC-DC Converter with Back-end-of-line Oxide Channel Transistor	Monolithic 3D DC-DC converter to provide efficient power delivery	Wantong Li
Vivian Zhou		vz2159@columbia.edu	Michal Lipson	2026 Full time	Active and Passive Photonic Devices for Heterogeneous Integration	Demonstration of ultra-low power, ultra-low loss and high bandwidth optoelectronic components by heterogeneous integration of new-emerging materials on passive photonic platforms	Shriddha Chaitanya
Ahmet Mete Muslu		metemuslu@gatech.edu	Suresh Sitaraman	Fall 2024	Triply-Periodic Minimal Surfaces for Thermal Management of High-Power Density Microsystems	A novel hybrid cooler design approach that strategically positions triply periodic minimal surfaces near localized hotspots is proposed to effectively address	-

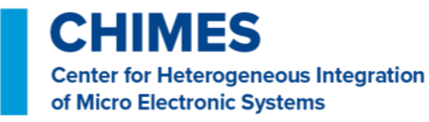
						heat spreading and removal challenges in high-power density microsystems with embedded cooling. The proposed solution helps avoid oversizing of integrated coolers with sufficiently increased design complexity.	
Junmo Lee		junmolee@gatech.edu	Shimeng Yu	Fall 2027	High Voltage Capacitor For Power Delivery Network in 3D Integrated Chips	Development of BEOL-compatible high voltage capacitor for integrated voltage regulator	-
Haoxiang Ren		haoxiang.ren@g.ucla.edu	Subramanian S. Iyer	Spring 2025	Power-efficient and Cost-effective Power Delivery Architecture for Heterogeneously Integrated Wafer-scale Systems	Front-side power delivery + Si-GaN 3D integration using Cu-Cu bonding for large chiplet-based systems	-
Krutikesh Sahoo		krutikesh@g.ucla.edu	Subramanian S. Iyer	Spring 2024	A High Throughput Two-Stage Die-to-Wafer Thermal Compression Bonding Scheme for Heterogeneous Integration	High throughput thermal compression bonding process for wafer-scale & chiplet-based systems including mechanical and electrical reliability measurements.	-

Sriharini Krishnakumar		skrish47@uic.edu	Inna Partin-Vaisband	Fall 2025	Vertical Power Delivery for Emerging Packaging and Integration Platforms - Architectures, Models, and Circuits	Characterization of proposed vertical power delivery architectures for high power (1kW), high-current density (>2A/mm2) systems.	-
Khandker Akif Aabrar		kaabrar3@gatech.edu	Suman Datta	Fall 2024	BEOL Compatible Tungsten-doped Indium Oxide Power Transistors for On-Chip Voltage Conversion	Co-integration of BEOL-compatible E-mode and D-mode power transistors for energy efficient on-chip DC-DC converter	-
Olusola Akinbami		olusola.akinbami@colorado.edu	Steven George	Summer 2024 Internship/ Summer 2027 Full Time	Atomic Layer Deposition of Channel Material for Power Delivery	Investigate wide band-gap semiconductors with impressive carrier mobility that can be deposited with low temperature Atomic Layer Deposition.	-
Jonti Talukdar		jonti.talukdar@duke.edu	Krishnendu Chakrabarty	Spring 2024 full time	Voltage droop based timing deration of critical paths in 2.5D Chiplets	Approach for Side Channel Security Evaluation due to RO-induced Voltage Droop in Chiplet PDN	-

Ashita Victor		avictor8@gatech.edu	Muhannad Bakir	Internship: Summer 2024 Full Time: Summer 2027	Chiplet Reconstitution Technology using SiO2 for High-density Heterogeneous Integration	To achieve 3DHI by encapsulating a "sea of chiplets" using low- temperature CMOS compatible silicon dioxide. The chiplet tiers can be post processed at a wafer scale. High I/O density can also be achieved using fine-pitch through-oxide-vias.	-
Dhruv Thapar		dhruv.thapar@asu.edu	Krishnendu Chakrabarty	Summer 2024 internship	Characterization of defects in FeFETs	Ferroelectric field-effect transistors, referred to as FeFETs, are promising emerging devices, but the impact of manufacturing imperfections on these devices has yet to be studied. We develop a machine-learning (ML) framework to characterize these fault-injected FeFET devices.	-

Hang Yang		hyang628@gatech.edu	Callie Hao and Sung-Kyu Lim	Tentative: 2027 summer	Back-side Power Delivery Networks (BS-PDN) with Integrated Voltage Regulator (IVR)	We try to use back-side PDN and back-side IVR to address challenges for advanced node front-side PDN.	Lingjun Zhu
Gauthaman Murali		gauthaman@gatech.edu	Callie (Cong) Hao and Sung Kyu Lim	Fall 2023	3DNN-Xplorer – A Machine Learning Framework for Design Space Exploration of Heterogeneous 3D DNN Accelerators	3DNN-Xplorer predicts PPA and workload-specific runtime and energy metrics for larger accelerator designs without actual physical design or simulation based on ML models trained with smaller accelerator designs.	-
Alexander Graening		agraening@ucla.edu	Puneet Gupta	Summer 2025	A Chiplet Cost Model and Cost-Aware System Partitioning	Cost model to help with system design space exploration and early physical architecture decisions. Additionally, we are experimenting with using this cost function for system partitioning.	-

Abdullatif Jazzar		jazzar@g.ucla.edu	Ximin He	PhD student sponsored by Saudi Aramco (employed)	Phase Separation based Modulation of Low Dielectric Gels	In attaining a suitable photo-definable low dielectric material, we employ a structure modulation strategy that we have verified on a model system, where chain mobilization and phase separation increase molecular entanglement and crystallization, respectively. Subsequently, the plan would be to modify the monomers to have photo-reactive groups to achieve photo-patternability.	-
Ahmed Mortuza Saleque		asaleque@ucdavis.edu	Prof. S. J. Ben Yoo	Fall 2023	Fabrication of Optical TSV on Silicon CMOS Photonics for Future 3D Electronic and Photonic Integrated Circuits	Design, fabricate, and test of optical TSV using both dry and wet etching method to achieve low-loss and high-bandwidth interconnections	Yi-Chun Ling, Yichi Zhang
Wanshu Zeng		wzeng60@gatech.edu	Muhannad Bakir	Summer 2024 internship	3D Integration of SiO2-based Chiplet Reconstituted Tiers by Cu-Cu Direct Bonding	3D integration between de-attachable reconstituted tiers consisting of 15 µm-thick SiO2 encapsulation with	Ashita Victor, Rohan Sahay



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						embedded emulated chiplets using Cu-Cu bonding	
Victor Wang		viw031@ucsd.edu	Andrew Kummel	Hired at SRC member company	Effects of Reverse templating on Ru ALD grown on sputtered Ru	By combining low resistivity ALD Ru with a smooth sputtered Ru seed layer, this work has produced low resistivity Ru films with smooth interface and resistivities below that of sputtered Ru.	Chenghsuan Kuo
Vineeth Harish		vineeth@g.ucla.edu	Subramanian Iyer		Hybrid Substrates with Organic Composite Materials for Silicon Interconnect Fabric	A novel approach for integrating fine pitch inorganic wiring layers using CMOS BEOL processes with coarse pitch organic wiring layers	-
Xingchen Li		xingchen.li@gatech.edu	Madhavan Swaminathan	Summer 2024 internship, spring 2025 full time	Characterization of Broadband Multi-chip Embedded Glass Interposer	Multiple chip embedded glass interposer with low-loss interconnection and integrated thermal management	-
Shurui Li		shuruili@ucla.edu	Puneet Gupta	Summer 2024	Photonic Joint Transform Correlator-based Neural Network accelerators	Photonic on-chip neural network accelerators based on Joint transform correlator with optical buffer, demonstrates state-of-the-art power	-

						efficiency for CNN workloads.	
Chenghsuan Kuo		c2kuo@eng.ucsd.edu	Andrew Kummel		Selective Growth of Co ALD for Copper bonding in the horizontal and 3D structure of chiplets		-
Ping Che Lee		p5lee@ucsd.edu	Andrew Kummel	Fall 2026 full time	Achieving a High Thermal Conductive One Micro AlN deposition By High Power Impulse Magnetron Sputtering plus Kick	1 µm HIPIMS+Kick AlN on bare Si substrate with Thermal conductivity 112 W/m-K has been achieved	-
Joon Woo Kim		jkim3375@gatech.edu	Madhavan Swaminathan	Summer 2024 internship, Spring 2024 full time	Thermal Management for High Power Density Chips Packaging using Die Embedding for 6G Wireless Applications	Thermal management of high power density chips using chip embedding in glass and Alumina Ribbon Ceramic (ARC) using multilayer substrates bonding	-
Shriddha Chaitanya		shriddha.chaitanya@columbia.edu	Michal Lipson	Spring 2026 full time	Active and Passive Photonic Devices for Heterogeneous Integration	Demonstration of ultra-low power, ultra-low loss and high bandwidth optoelectronic components by heterogeneous integration of new-emerging materials on passive photonic platforms	Vivian Zhou

Rohan Sahay		rsahay7@gatech.edu	Rohan Sahay	Summer 2024 Full time	Towards Advanced Bonding Technologies For 2.5D/3D Heterogenous Integration	Inverse Hybrid bonding	Ashita victor, Michael Nieves, Victor Wang, Jung Mu, Dipayan Pal,