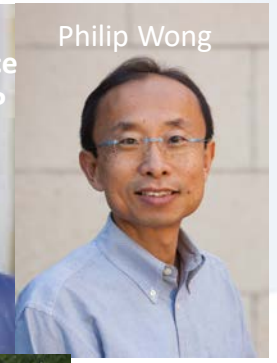
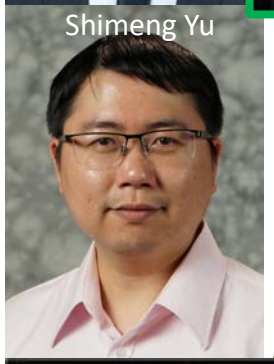
Center for Heterogeneous Integration of Micro Electronic Systems
SAB Review - Center Plan of Action for 2024

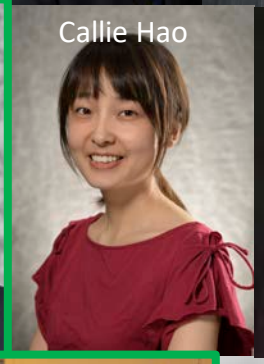
Madhavan Swaminathan (Penn State), Center Director
Muhannad Bakir (Georgia Tech), Assistant Director

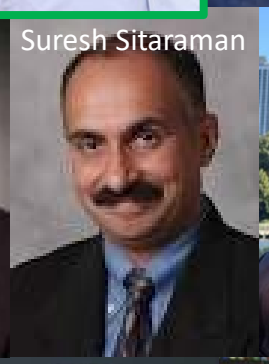
The CHIMES Team (23 PIs & 15 Univ)

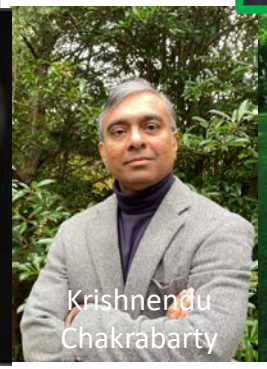


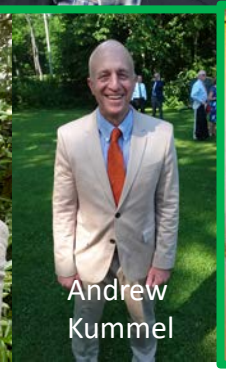


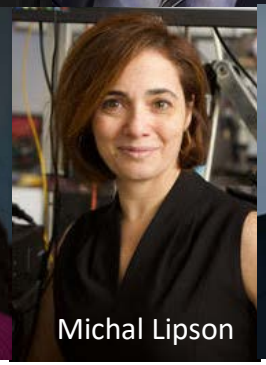
Satish Kumar









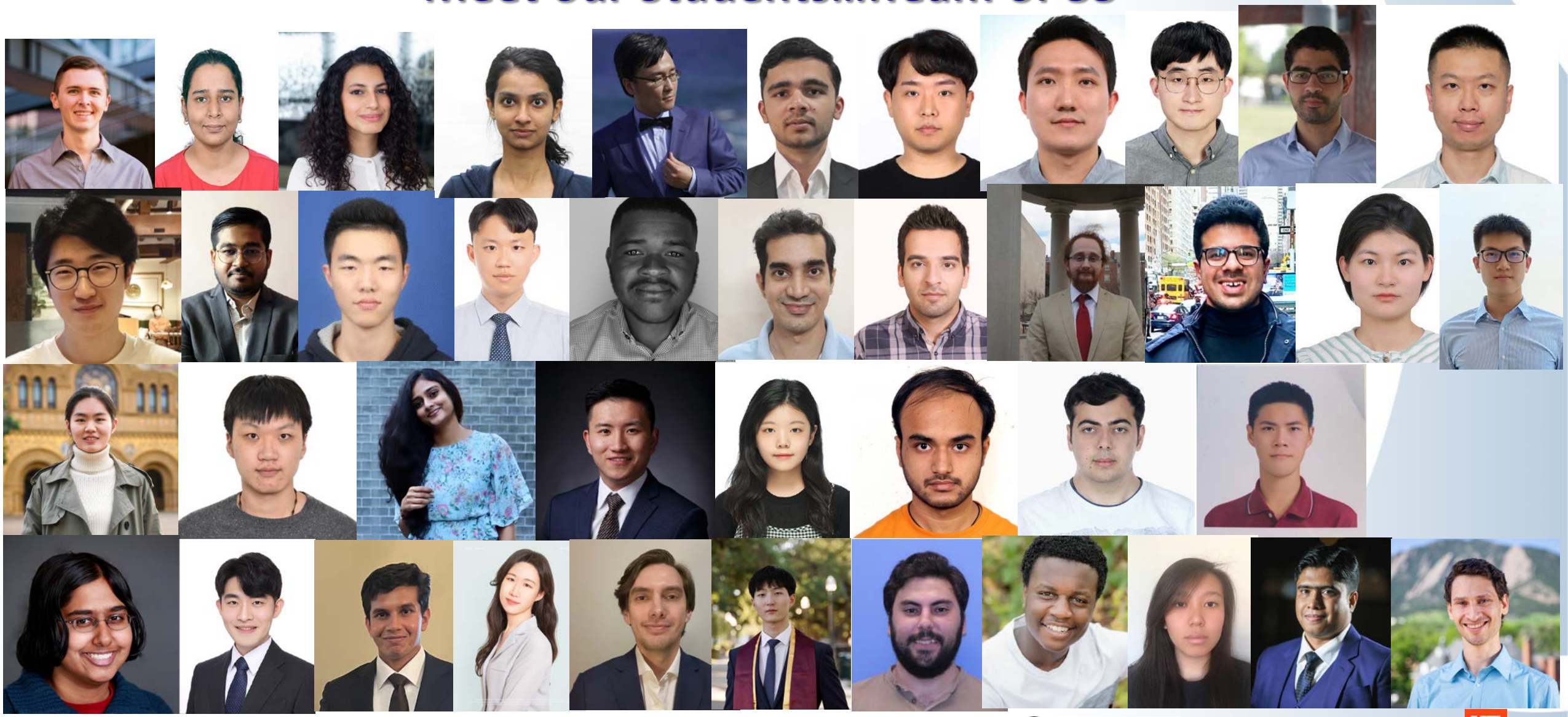


PennState
UCLA Georgia Tech
Columbia University in the City of New York
Cornell University
ASU Arizona State University
MIT Massachusetts Institute of Technology
Stanford University
The George Washington University, Washington, DC
UC San Diego
Rice University
UIC University of Illinois Chicago
UC Davis University of California
University of Washington
University of Colorado Boulder

SRC

CHIMES
Center for Heterogeneous Integration of Micro Electronic Systems

Meet our Students….Team of 88



SRC

CHIMES
Center for Heterogeneous Integration of Micro Electronic Systems

PennState · Georgia Tech · UCLA · Columbia University in the City of New York · Cornell University · ASU Arizona State University · UC Davis University of California · UF University of Florida

MIT Massachusetts Institute of Technology · Stanford University · UC San Diego · Rice University · UIC University of Illinois Chicago · University of Colorado Boulder

Change in Management

Rohit Sharma

Managing Director, CHIMES
Last date Apr. 30, 2024
Returned to India
Associate Prof. IIT Ropar

Saber Soltani

Operations Director, CHIMES
Start date date Apr. 22, 2024
Ph.D. HKUST 2016

Outline

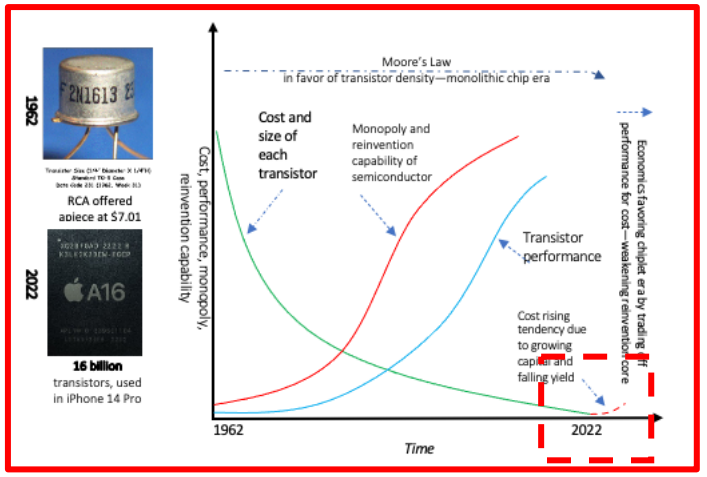
- CHIMES – A Summary
  - Our Vision
  - Themes-Roadmaps-Technical Approach
  - Research output 2023

- Plans for 2024
  - Realignment of Task ID 3136.017
  - Rapid Prototype Vehicle (RPV)
  - Inter Center and Sponsor Collaborations
  - Student Council
  - Expanding the CHIMES National & Global footprint
  - Year 2 Goals & Status

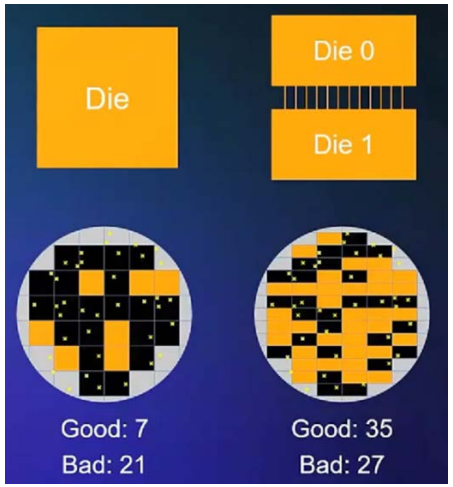
- Summary

Economics & Continuation of Moore's Law

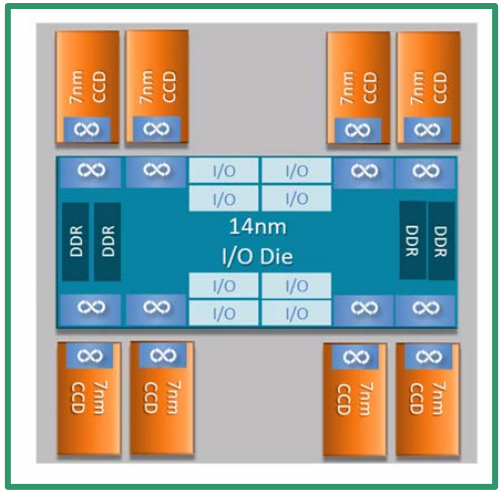
The Problem



Improved Yield

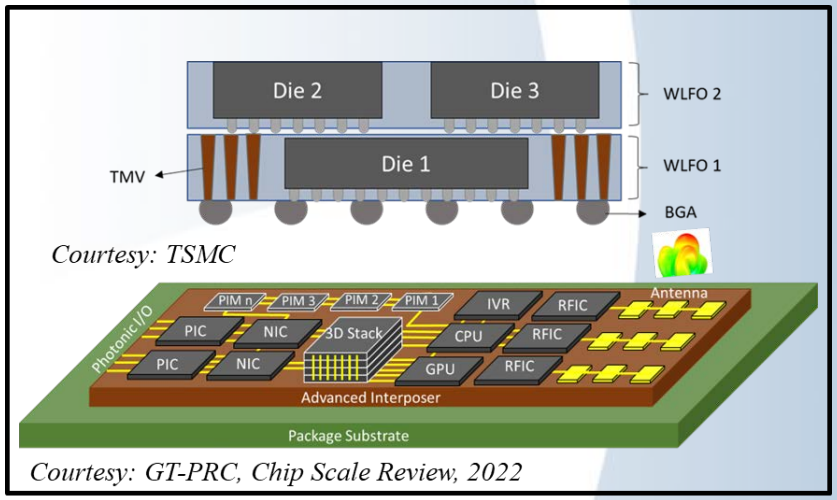


Shorter design time



Courtesy: AMD

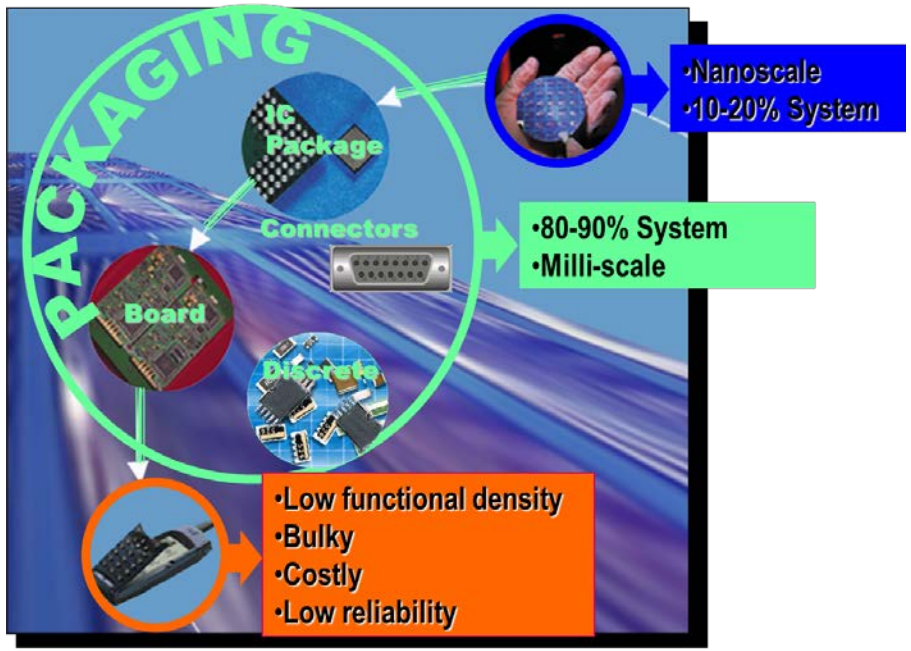
Heterogeneous Integration



Three reasons why Advanced Packaging is becoming critical for the continuation of Moore's Law:

1. Higher yield using smaller dies in advanced nodes.
2. Shorter time to design with smaller dies from optimized legacy technology nodes with enhanced functionality.
3. Move towards **HETEROGENEOUS INTEGRATION**.

Packaging: Past, Present, and Future ….



Packaging (Past)

Advanced Packaging (Present)

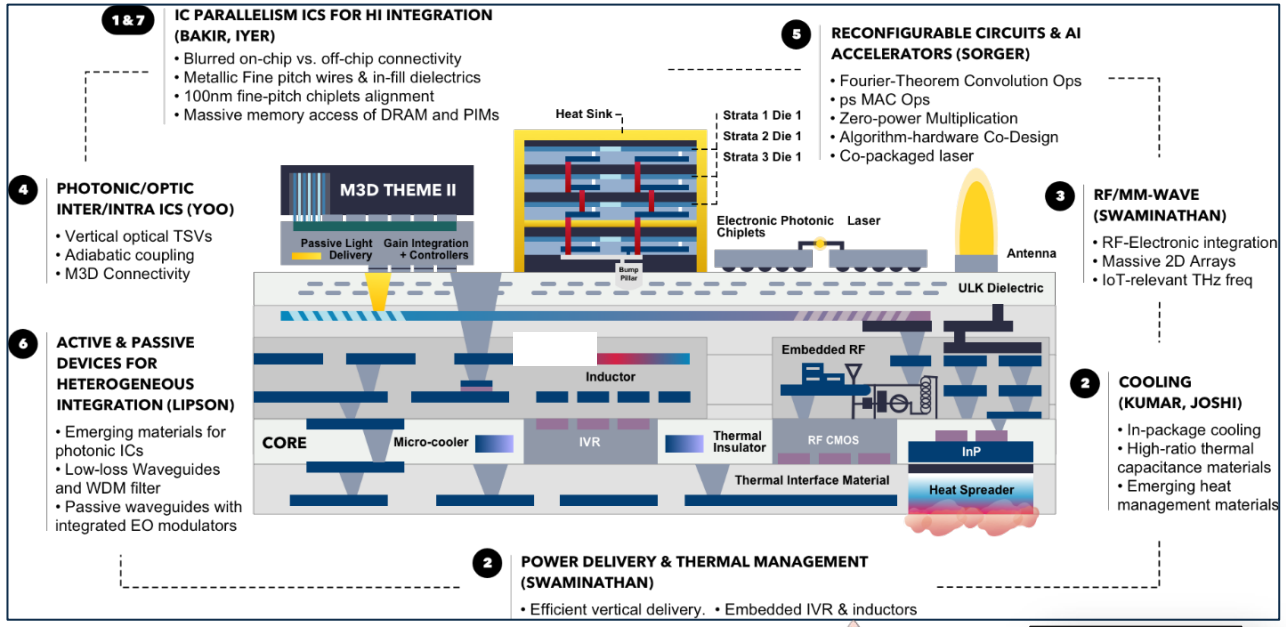
Heterogeneous Integration (Future)

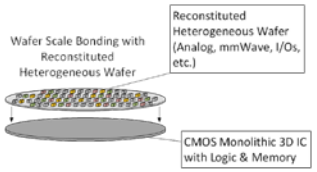
- **Present:** FEOL Transistor, BEOL Wiring & Package individually developed and combined
- **Future (CHIMES Vision):** New and transformative logic, memory, and interconnect technologies that overcome the inevitable slowdown of traditional dimensional scaling of CMOS by interconnecting a **diversity of transistors and integrated circuit components**, **blurring the line between what is on-chip and what is off-chip**.

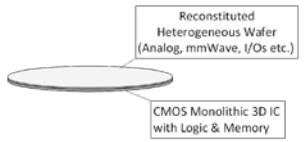
CHIMES – A Snapshot

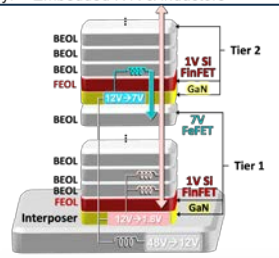
- Our vision driven by Emerging Applications
- Roadmap used to drive Research based on Targets
- Four Themes
- Team
  - 23 PIs from 15 Univs
  - 88 Students (includes post docs)
  - 24 Research Tasks
  - 160+ Industry Liaisons

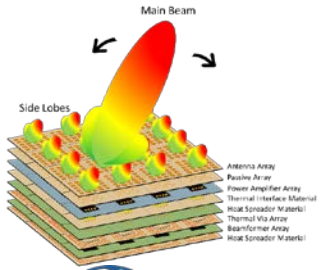
Ultra-dense Heterogeneous Interconnect & Assembly (Theme III)

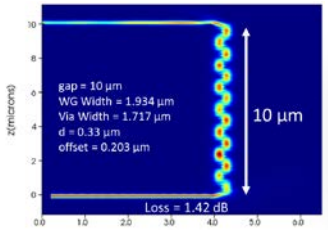


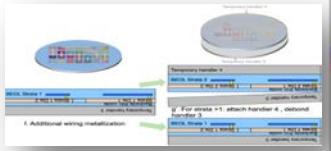


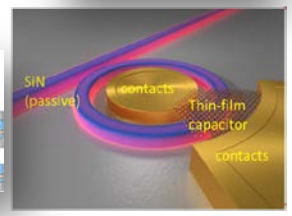






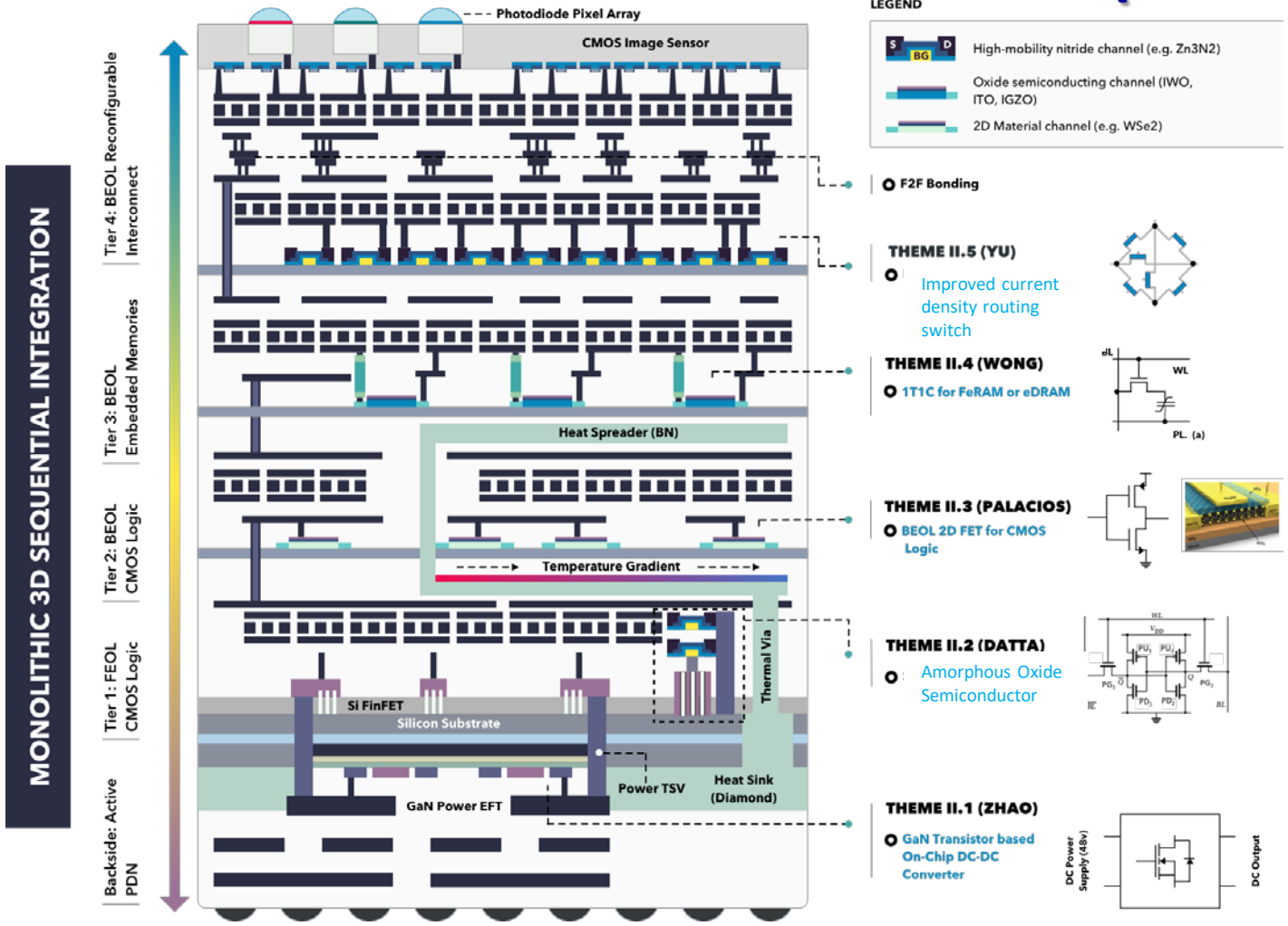






Metric & Drivers	Metric (10 Years)	State of the Art (SOTA)
Electrical IC Parallelism & Volume Scaling (AI, DC, M)	IO density 16M/mm^2	IO density 10K/mm^2
	BW Density > 500Tbps/mm^2; <0.01 pJ/bit	BW density 28Tbps/mm^2; 0.021 pJ/bit (ARM/GT IEDM 2020)
Cooling & Power Delivery (S, C, H, AI)	Power 1000W; Current density 2–5A/mm^2; Efficiency >80% (HIR 10 year)	Power 400W; Current Density 1A/mm2; Efficiency <70%
	Current 50 KAmps; Power 50kW; PDN Power <1KW (2%); Efficiency>80%	Current 18 KAmps; Power 10KW; PDN 5KW (33%); η <67% (Tesla Dojo)
Wireless IC & I/O (C, S, H)	Insertion Loss <1dB (PA output to Antenna input) @ 0.3 – 1THz; DARPA ELGAR 1dB	Insertion Loss >5dB in D-Band (110-170 GHz) (ComSenTer)
	Antenna efficiency >90% @ 0.3–1THz	Antenna efficiency >90% (< 100GHz)
	SNR 30dB (128 QAM)	SNR 20dB (128 QAM) D-Band
Photonic/Optic IC and Chiplet Communication (AI, C, DC)	Coupling loss < 0.9dB; Misalignment; +/−1mm	Coupling Loss ~ 1dB (O-Band)
	100 (Tbps/mm)/(pJ/bit) (link-level)	1 (Tbps/mm)/(pJ/bit) (DARPA PIPES)
	Bandwidth (BW) Reconfigurable ICs between chiplets; 0.5-5Tbps aggregated BW	NA
	Optical gain/laser integration via photonic wire bonds (PWB) and/or mono-int. (DARPA LUMOS)	Laser is off-chip → requiring packaging (costly & not reliable)
Reconfigurable Circuits & Modules (AI, S, DC)	100 TOP/J, 1ns latency, infinite bit-resolution MAC ops (DOD Labs e.g., AFRL, ARL)	<5 TOP/J, 1000+ns latency, 4-12 bit
	AI accelerator: 10–100 fJ/MAC, 1–50 TMACs/mm^2, 1ns–25 ps operation (Google X)	0.5–1 pJ/MAC, 0.5–1 TMAC/s/mm^2, 0.5–1 GMVM/s, and 1–2 us per MVM
Active & Passive Devices for Heterogeneous Integration (C, S, DC)	EO Modulator: ER > 12dB; BW > 15GHz per channel; (next Gen AIM Photonics components)	NA
	Interposer Waveguides; losses < 0.1dB/cm	1.5dB/cm
	Interposer Filters for WDM: filter sharpness > 15dB over < 0.2nm BW (AIM Photonics Foundry)	NA

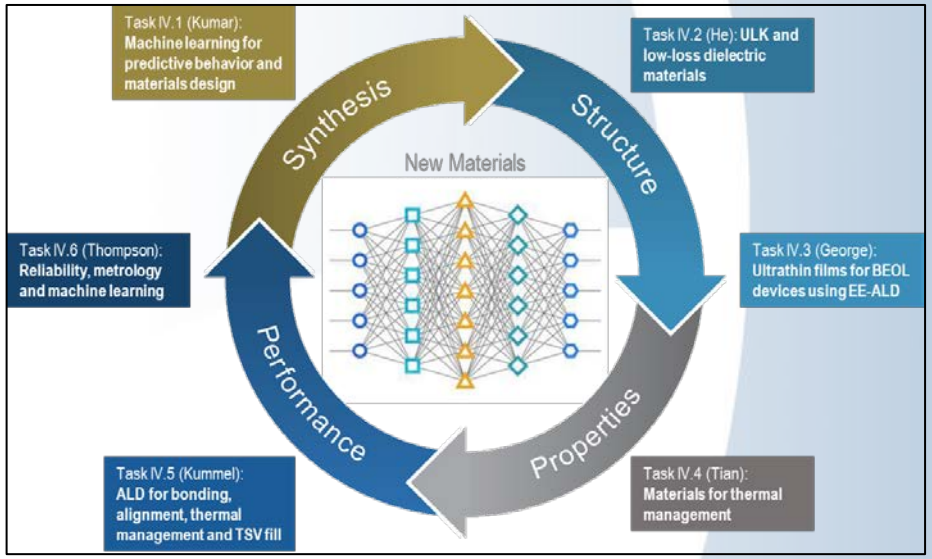
Monolithic 3D (M3D) Densification and Diversification on Silicon Platform (Theme II)

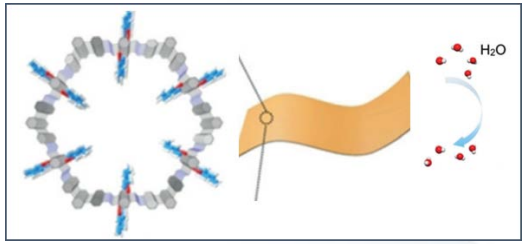


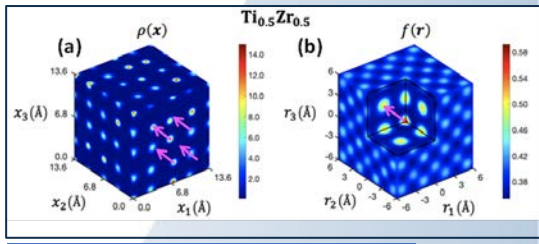
Metrics & Drivers	Center Proposed Metrics	State of the Art (SOTA)
Technology (AI, S, DC, M)	High-density 3D SRAM cell area (2CPP×3MP)	FinFET SRAM cell area (2CPP×8MP) CPP: contact-poly-pitch, MP: M1 pitch
	Mobility for BEOL transistor (2D, oxide, nitride)>100 cm^2/Vs	IWO transistor mobility ~20 cm^2/Vs (from JUMP 1.0)
	Drive current for BEOL memory access at 3V (>2mA/μm)	IWO drive current at 3V ~500μA/μm (from JUMP 1.0)
	BEOL thermal budget < 400°C (e.g. for Zn_3N_2)	GaN growth (~1000°C)
	GaN p-type FET drive current (>1A/mm)	GaN p-type FET drive current (>100mA/mm)
In-pixel Processing System Workloads (AI, S, DC, M) (TOPS normalized by 1b×1b MAC)	Efficiency >50,000 TOPS/W (M3D stack-level)	~5,000 TOPS/W (TSMC ISSCC 7nm SRAM CIM, 4kb 2D macro-level)
	Compute > 5,000 $TOPS/mm^2$ (M3D stack-level)	~500 TOPS/mm2 (at 2D macro-level)
	Power density <1 W/mm^2 (M3D stack-level)	~0.4 W/mm^2 (at 2D macro-level)
	Max runtime temperature (<85°C) (M3D stack-level)	2D circuit runtime temperature <85°C

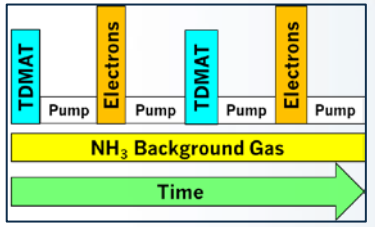
Materials Behavior, Synthesis, Metrology, And Reliability (Theme IV)

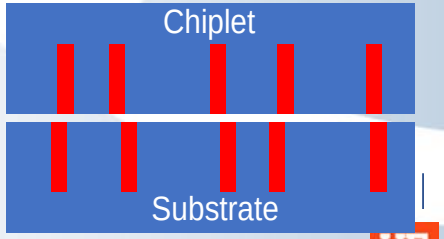
Metrics & Drivers	Metrics (10 Years)	State of the Art (SOTA)
Ultra-low K Dielectrics AI, C, DC, M)	Permittivity < 2.5, Loss 0.01 @ 1THz, Thickness: 1µm – 100µm, CTE: <30 ppm/C	Permittivity 3.0, Loss 0.05 @ 150GHz, Thickness: 5mm, CTE: 30-40 ppm/C
Interconnects (AI, DC, M)	For BEOL Devices: 100nm pitch, 50nm dia., aspect ratio 2-10 for 2-5 tiers for via bottom-up fill.	400nm pitch, 200nm dia., aspect ratio up to 5 (selective ALD for Co from ASCENT)
	TSVs: 100 nm diameter, 250 nm pitch; aspect ratios >30:1	9 µm pitch and ~2µm diameter [AMD 3D V-cache]
	Misalignment-tolerant bonding process for inter-layer interconnects at 250 nm pitch	5.5 µm pitch using face-to-face hybrid bonding [ARM/GF]
Thermal (AI, C, S, DC, H)	TIM: 200W/m-K; Thickness <30µm; CTE 20 ppm/C	TIM: 25-100 W/m-K; CTE 55-200 ppm/C
	Heat Spreader: - cBN 200 W/mK at 100 nm thick, 500W/mK at 1 µm - Diamond 400 W/mK at 1 µm, 1500 W/mK at 10 µm, 2000 W/mK at 50µm.	Heat Spreader: Cu 400 W/mK bulk
	Ultra-low interface thermal resistance, e.g. GaN/diamond 3 m^2K/GW, Si/diamond 3 m^2K/GW	GaN/diamond 6.5 m^2K/GW Si/diamond 9.5 m^2K/GW
	Thermal isolation materials: 0.02 W/m-K, dielectric constant < 1.5, thermally stable above 300°C	Thermal isolation materials (SiCOH): 0.6 W/m-K, dielectric constant 1.8-2.5, and thermally stable above 300°C





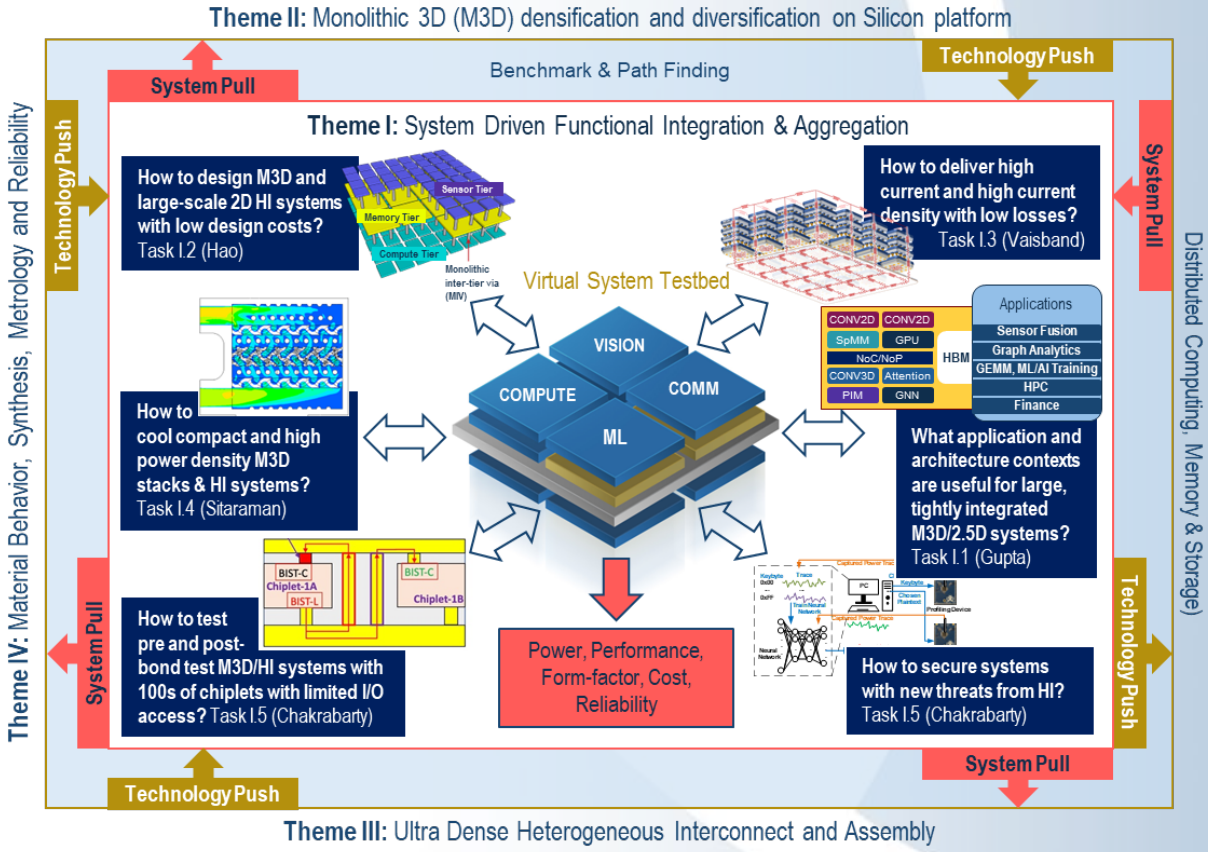






System Driven Functional Integration & Aggregation (Theme I)

Metrics & Drivers	Metrics (10 Years)	State of the Art (SOTA)
Benchmarking (AI, C, S, DC, M, H)	Automated cross-layer pathfinding framework with Power, Performance, Form-factor, Cost and Reliability (PPFCR) prediction for full systems + applications.	Pathfinding limited to technology or technology + circuit only; limited automation.
Co-Design (AI, C, S, DC, M, H)	Physical design tools for M3D chiplets integrated on systems spanning > 20,000mm^2	No tools for M3D; interposer tools limited to ~2000mm^2
Power Delivery (AI, DC, H)	Power 1000W; Current density 2-5A/mm^2; Efficiency >80% (HIR 10 year)	Power 400W; Current density 1A/mm^2; Efficiency <70%
	Current 50 kAmps; Power 50kW; PDN Power <1kW (2%); Efficiency>80%	Current 18 kAmps; Power 10kW; PDN 5kW (33%); Efficiency <67% (Tesla Dojo)
Thermal (AI, C, DC, H)	Chiplet: Background heat flux (entire die) 2kW/cm^2; hot spot heat flux (0.1mm x 0.1mm) 30kW/cm^2; Vol. removal 2kW/cm^2 mm; Thermal time constant 1µs	Background heat flux (entire die) 200W/cm^2; hot spot heat flux (1mm x 1mm) 1kW/cm^2; Vol. removal 200W/cm^2 mm; Thermal time constant 20µs
	Stack: Thermal isolation ratio 0.95; TIM specific resistance 0.3 mm^2 K/W for 30 µm; k 200 W/mK, elastic modulus 30 MPa	Thermal isolation ratio 0.5; TIM specific resistance 1 mm^2 K/W (DARPA NTI)
	Interposer: Heat spreader effective k 10,000 W/mK; Heat spreader thickness 0.2mm	Heat spr. effective k 4000 W/mK; Heat spreader thickness 2mm (DARPA TGP)
	Server (1U): Volumetric R_{th} 0.015 °Ccm^3/W	Volumetric R_{th} 0.03 °Ccm^3/W
Electrical/Optical Test (AI, DC)	Fault coverage >99% (Short/Open) & >95% (device/components)	<95% coverage (Short/Open), devices/components (no test or BIST)
	10X reduction in test cost (Package BIST)	(Relative) test cost growing
Hardware Security	Probability of trojan evasion >99%	No universal security metrics available
	Probability of reverse engineering <1%	No universal security metrics available
	Split manufacturing based on fine pitch HI	Not available



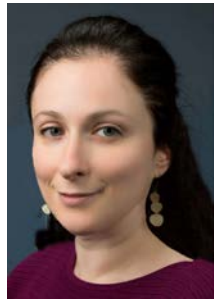
Research Output 2023

- Papers: 89
- Invited & Keynotes talks: 84
- Awards: 24
- Software releases: 3

Major PI Awards & Recognitions

IEEE VLSI Technology and Circuits' Test of Time Award and IEEE Andrew S. Grove Award

2023 SPIE Maria Goeppert-Mayer Award
IEEE Fellow



NSF CAREER Award

2024 IEEE Rao R. Tummala Electronics Packaging Award
2023 NAI Fellow

IEEE Fellow Intel Outstanding Researcher Award
Promoted to Professor

2023 Johnson & Johnson WiSTEM2D Award
2023 Moore Inventor Fellow

NSF CAREER Award

DARPA Young Faculty Award
2023 APL Rising Star

Director, NAPMP – CHIPS Act

CTO, SWAP HUB @ ASU
DoD Microelectronics Commons

Clarence J. LeBel Chair in Electrical Engineering and Computer Science

Director, PRC

Center Plans for 2024

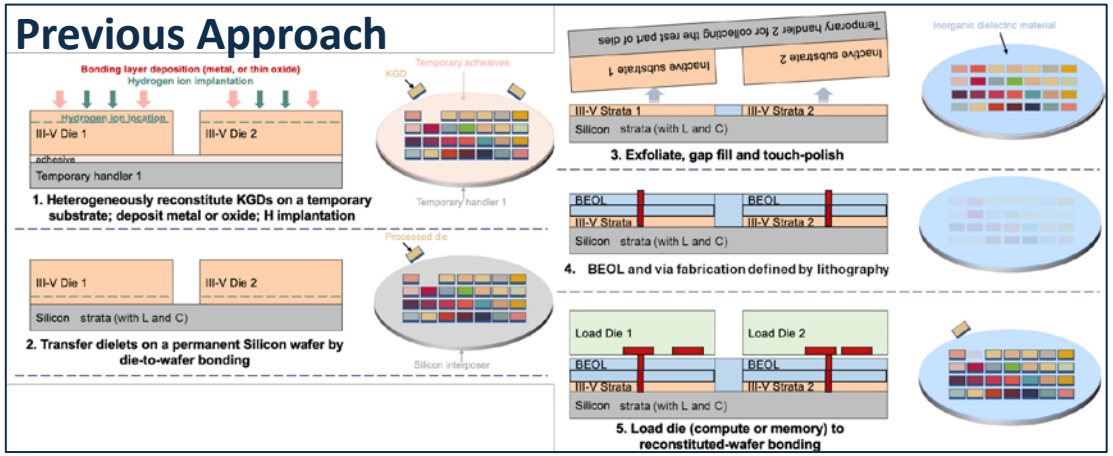
Realignment of Task ID: 3136.017

Acting PI: Puneet Gupta and Madhavan Swaminathan (Technical Direction)

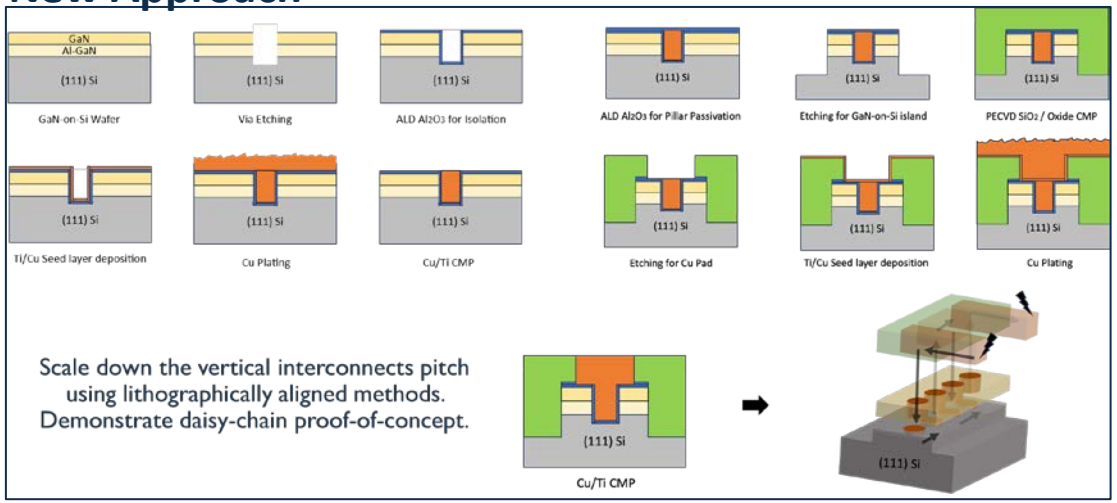
Objective: Scale down vertical interconnect pitch in 3DHI to sub µm level using lithographically aligned methods

Subu S. Iyer
2 Year Leave of absence to serve as Director, NAPMP

Previous Approach



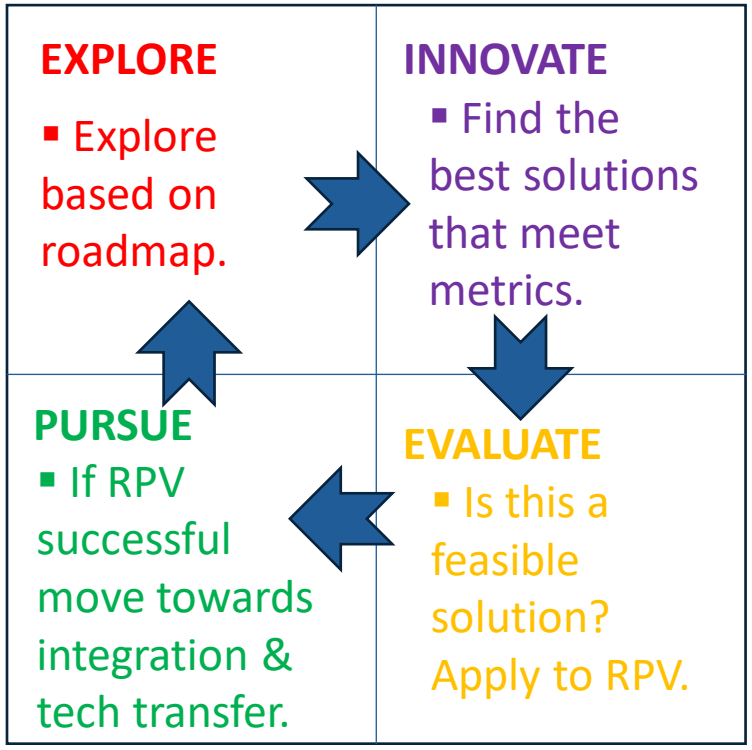
New Approach



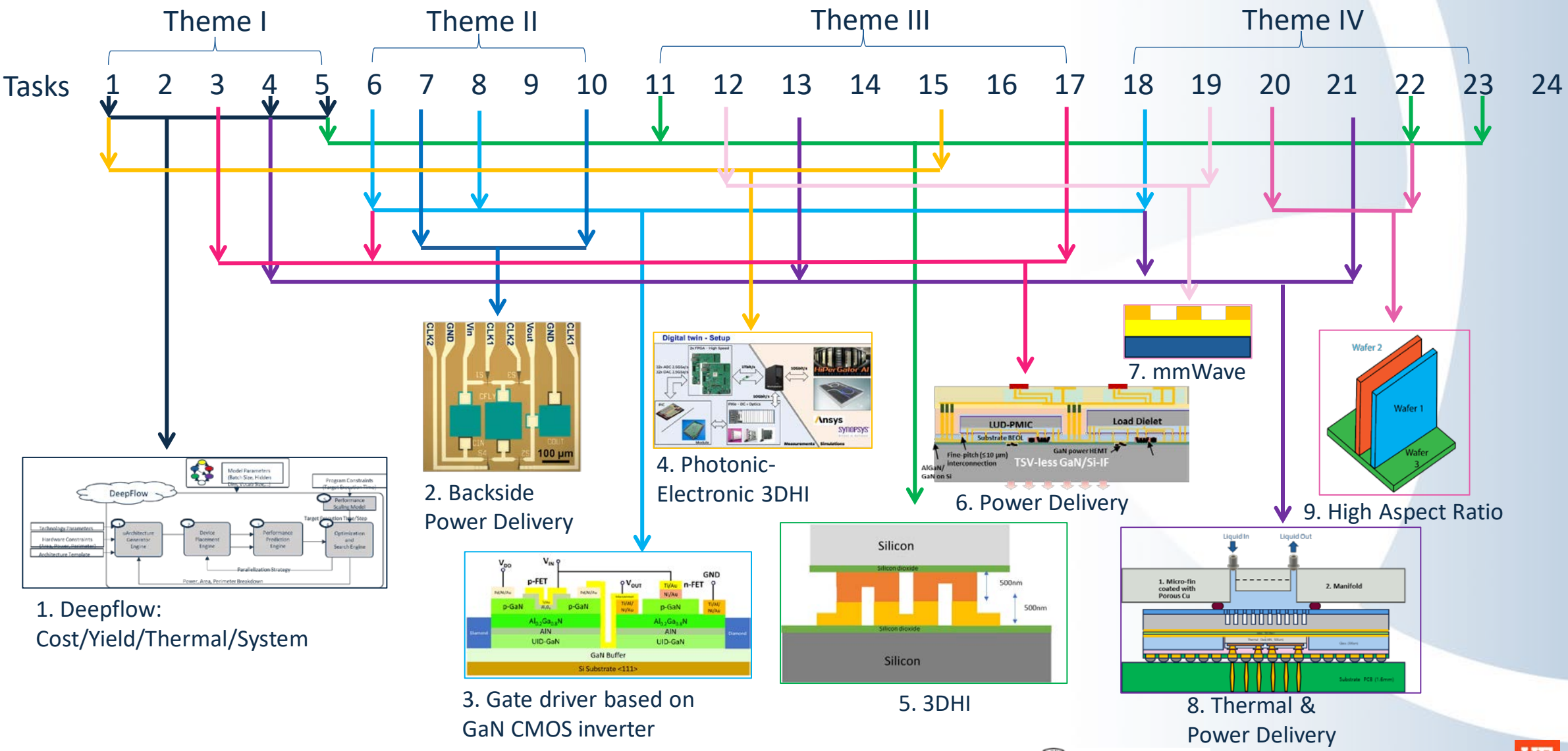
- High-quality 3D strata stacking technology was recently developed
- On-shelf 4-inch GaN on Si wafers are available for the demonstration of the proposed method
- **Hydrogen exfoliation is not needed in phase 1 (solely for generating the thin GaN strata)**
- Will apply Hydrogen exfoliation method in phase 2 on other III-V materials that can not be easily grown into large-size
- The heterogeneous power delivery platform is a good prototype to demonstrate the proposed approach
- The heterogeneous power delivery structure using lithographically defined vertical connections and fine-pitch bonding connections features:
- Small PDN impedance: micron-level distance
- Vias are massively fabricated on the same wafer by lithography
- High vertical interconnection density

Rapid Prototype Vehicle (RPV)

- Bulk Material or Component properties need to be achieved.
- However, it is the interfaces and integration that are the challenge in Heterogeneous Integration.
- Purpose of RPV is to evaluate new technologies early in the cycle and only pursue ones that are promising.
- Enables natural collaboration between tasks and centers!

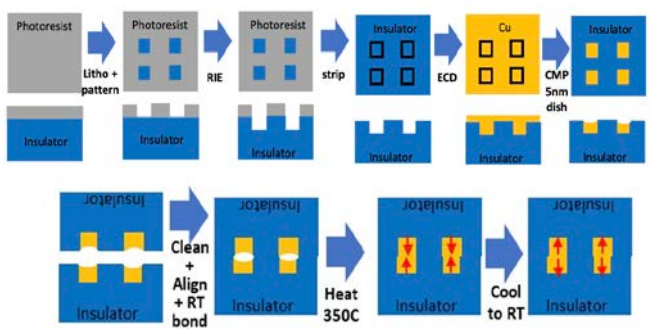


Task Collaborations through Rapid Prototype Vehicle (RPV)

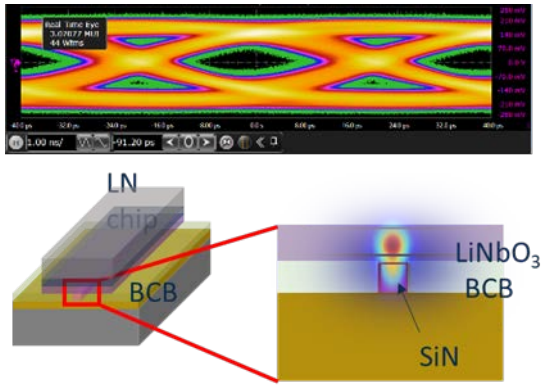


Specific Collaboration with other JUMP Centers

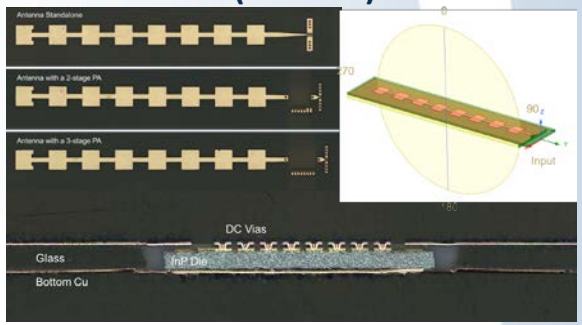
ALE for Hybrid Bonding
Steve George (SUPREME) & Andrew Kummel (CHIMES)

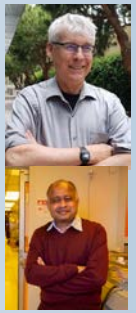


Photonics Heterogeneous Integration in a Datacom Link
Keren Bergman (CUBIC) & Michal Lipson (CHIMES)

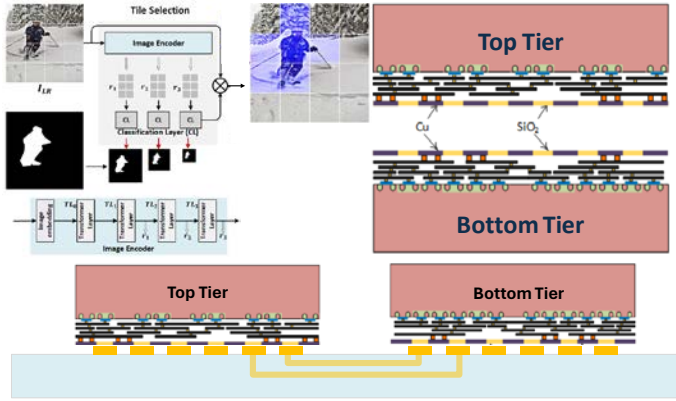


Advanced Packaging for Communications
Mark Rodwell (CUBIC) & Madhavan Swaminathan (CHIMES)

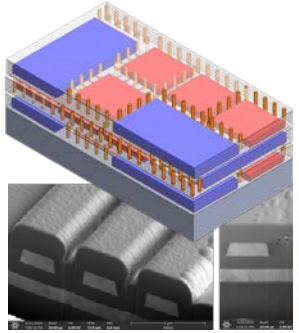


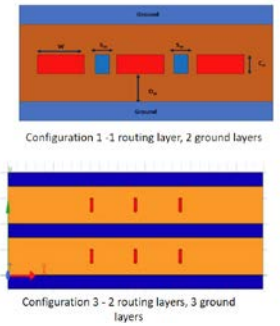


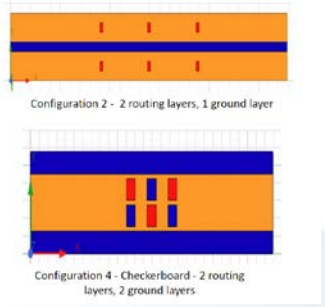
3D In-Sensor Computing
Yu Cao (CoCoSys) & Muhannad Bakir (CHIMES)

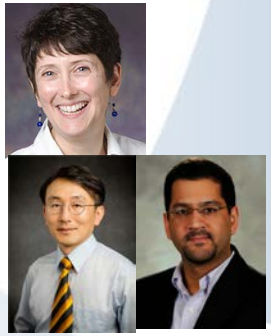


Design and Analysis of UCIe Interface for Reconstituted Chiplet Technology
Elyse Rosenbaum & Nam Sung Kim (PRISM) & Muhannad Bakir (CHIMES)









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CHIMES
Center for Heterogeneous Integration of Micro Electronic Systems

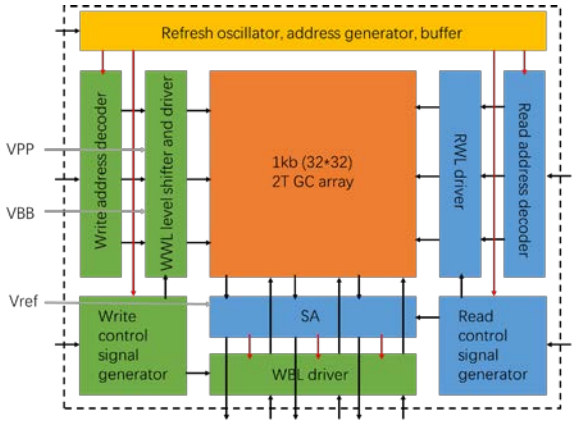
PennState · Georgia Tech · UCLA · Columbia University in the City of New York · Cornell University · ASU Arizona State University · UC Davis University of California · UF University of Florida · MIT Massachusetts Institute of Technology · Stanford University · UC San Diego · Rice University · UIC University of Illinois Chicago · University of Hawai'i · University of Colorado Boulder

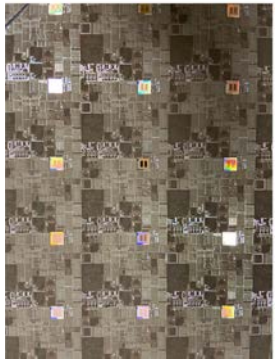
Specific Collaboration with other JUMP Centers (cont.)

PRISM (P. Wong) & CHIMES (P. Wong) (Hybrid Gain Cell)

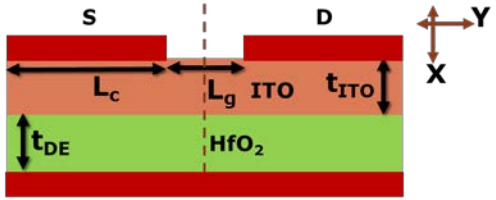
CHIMES: Hybrid gain cell tape-out

TSMC 40-nm chip

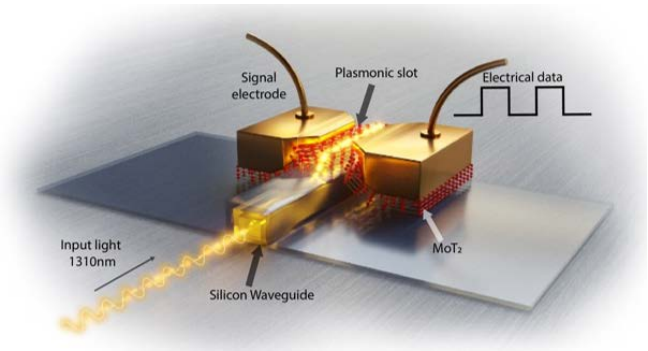


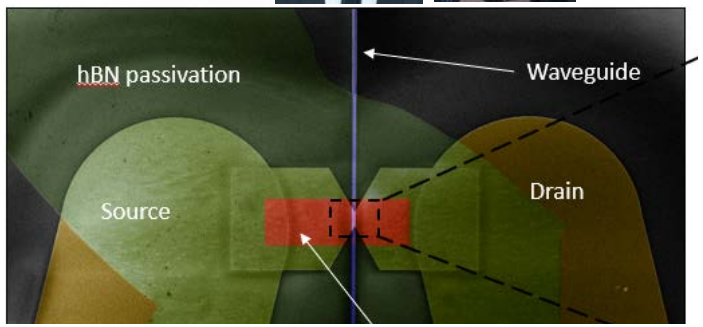


PRISM: ITO Device Modeling

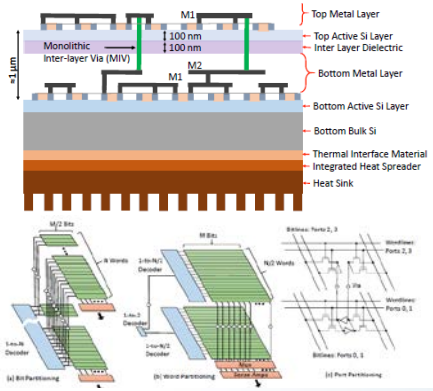


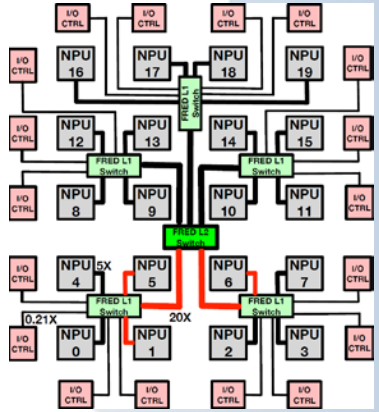
SUPREME (V. Sorger) & CHIMES (T. Palacios) (Photonic SiN WG w/ TMDC)





ACE (J. Torrellas, T. Krishna) & CHIMES (P. Gupta) (Wafer Scale Networks)



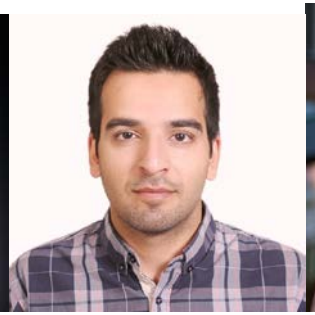


Collaborations with Sponsors (In Progress)
Opportunities for Tech Transfer

Tomás Palacios	Working with IBM to develop stealth dicing and advanced packaging capabilities to build 3DIC solutions for W-Band
	Working with Raytheon to develop a lab-to-fab 200 mm GaN MMIC process for G-Band
Volker Sorger	Engaging with Intel on photonic interconnects in glass substrates.
	GlobalFoundries' UPP program co-developing Fourier-based convolution neural network ASICs
Philip Wong	Collaborating with TSMC to heterogeneously integrate oxide semiconductor high density gain cell memory on Si CMOS logic platform (CMOS+X)
Shimeng Yu	Working with TSMC on device modeling and applications of back-end-of-line oxide semiconductor transistors
Andrew Kummel	High speed sputtering technique should get traction from Intel and TSMC
Zhiting Tian	Working with EMD to validate the thermal conductivity of the new TIM she is developing
Madhavan Swaminathan	Working with EMD on Liquid Crystals for mmWave
	Working with Intel and Qorvo on glass substrates

Broadening Participation (BP)

Victor Wang
UCSD



Ramin Rahimzadeh Khorasani, PSU

Alexander Graening, UCLA

Zhiting Tian, Cornell, BP Champion

Shuhan Liu, Stanford

Sriharini Krishnakumar, UIUC

Shriddha Chaitanya, Columbia

Myriam Bouzidi
GT - President

- ❑ CHIMES Pledge (https://www.chimes.psu.edu/broadening-participation.aspx)
- ❑ Flipped Panel at 2023 Annual Review – "Ask the Students"
- ❑ Student resume book (60 Resumes)
- ❑ 23 Students invited to participate at the PI Meeting in Chicago June 7, 2024
  - One student per PI selected to participate
  - Get them involved in "Roadmap Discussions". Roadmaps are never static but need to be dynamic and have to evolve with time.
  - Planning for 2024 Annual Review
- ❑ Aug 5, 2024 (1pm – 5pm) Student Networking (1 day prior to Annual Review)

Expanding our Footprint
Introducing MASH (Mid-Atlantic Semiconductor Hub)

- Semiconductor Hub created to respond to CHIPS Act Funding Opportunities
  - 10 Founding Univs (Total: 20 Univs)
  - 180 Companies
  - 300 Workforce Development Organizations
  - Access to 40 facilities
  - University, Industry, Government partnership
  - https://mash-semiconductors.org/
- **CHIMES – CUBIC Partnership**
  - Leading effort on Semiconductor packaging and Photonics
- Responded to recent NOFO on Materials & Substrates (NAPMP)
  - Several sponsors and partner univs on the team
- Part of NGMM (3DHI), DARPA

CHIMES Receives Gifts for Expansion

- Anonymous Donor: $4M
  - Name a new semiconductor packaging manufacturing laboratory @ Penn State for CHIMES

- Anonymous Donor: $1M
  - Support to the Center for Heterogeneous Integration of Micro Electronic Systems ("CHIMES"), or successor center. Expenditures shall be made in accordance with University policy and may include, but are not limited to, facility renovations and improvements, scholarships/awards for graduate and undergraduate students associated with CHIMES, assistantships, research expenses, guest speakers, and/or equipment purchases.

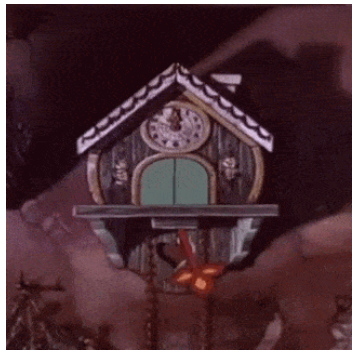
- Announcements expected soon

Center Year 2 Goals & Progress

Goal	Status
1. Better Communication with Industry Liaisons. Increase collaboration with sponsors.	✓ Each theme meeting every 6 weeks. 1.5 hours - Overview by Theme Leader & 3 Student Presentations. Identified specific sponsor collaborations. Develop methods to expand.
2. Develop Rapid Prototype Vehicle (RPV) to foster collaboration between tasks.	✓ 9 Vehicles defined. Need to focus on implementation. Presentation at Annual Review after discussion at PI meeting.
3. Increase Inter-center collaboration. Several centers asking for support on packaging.	✓ 5 significant collaborations identified. Requested SRC to help organize a workshop to discuss and strategize on support for packaging.
4. Broadening Participation – Increase involvement of students in CHIMES to make them future leaders.	✓ Established Student Council. Involving students in roadmaps. Quarterly Open House with students "Ask the Director". Developing strategy to involve UG Students.
5. Expand CHIMES National & Global footprint.	✓ Leading Semiconductor Packaging Efforts for NAPMP Funding Opportunities. Several keynotes & invited talks. Participating in India Semiconductor Mission (ISM). CHIMES Team Visit to Korea & Taiwan in Oct '24. MoUs.

Summary

CHIMES continues to CHIME! Positioning ourselves to become the Global Academic Leader in Semiconductor Packaging.



Center Newsletters

2024
- Quarter 1

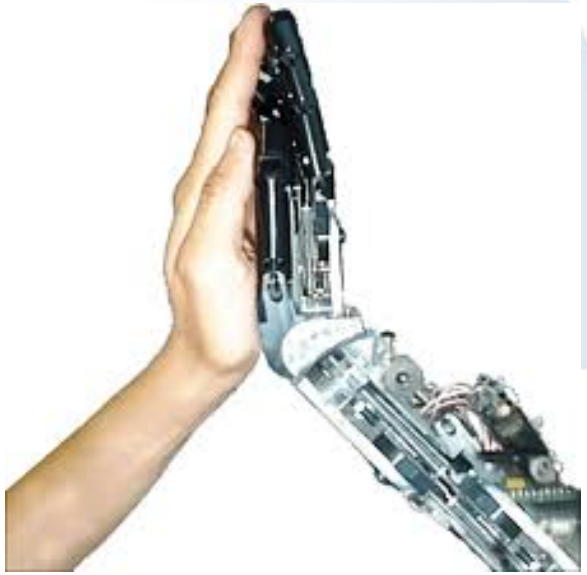
2023
- Quarter 1
- Quarter 2
- Quarter 3
- Quarter 4

www.chimes.psu.edu

- Hope you are receiving the CHIMES Quarterly newsletters
- It has a wealth of information

See y'all Aug 6-7 for the Next Annual Review @ Georgia Tech!

Thank you



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Center for Heterogeneous Integration of Micro Electronic Systems

PennState Georgia Tech UCLA Columbia University in the City of New York Cornell University ASU Arizona State University UC Davis University of California UF University of Florida

MIT Massachusetts Institute of Technology Stanford University UC San Diego Rice University UIC University of Illinois Chicago University of Colorado Boulder