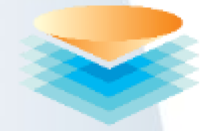


# Center for Ubiquitous Connectivity

## SAB Center Meeting

April 24, 2024

**Director: Keren Bergman**, Columbia University
**Co-Director: Ali Niknejad**, UC Berkeley

# Cloud to Edge Connectivity Challenges

**Explosive Growth in Data Communication Demands**

**Cloud Connectivity Challenges:**
- Orders of magnitude gap between on-chip/off-chip BW
- Strong distance-dependent communication energy
- Scalability limited by energy and bandwidth tapering
- Massive heterogeneity – compute/memory/accelerator

**Edge Connectivity Challenges:**
- Driving mm-Wave capacity to meet data demand with robustness, reliability, mobility, and low cost
- Massive densification, power, loss, thermal cooling
- Long-range links - back-haul, long range front-haul, airborne links - limited by output power

**System Connectivity Challenges:**
- Seamless connectivity between edge and cloud for optimized cross-layer performance
- Reconfigurable, adaptable connectivity to accelerate heterogeneous applications
- Secure and resilient connectivity across edge and cloud

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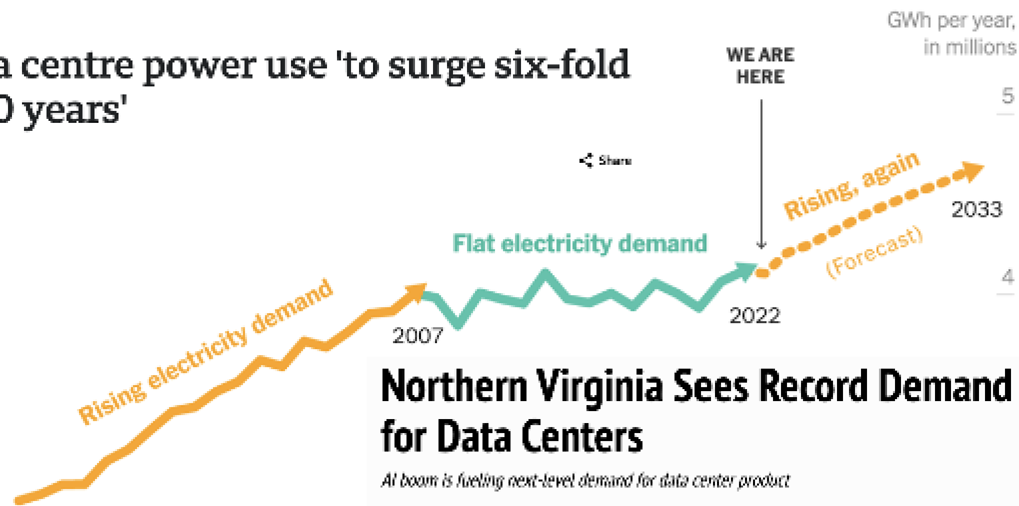
# Global Energy Footprint of AI




**The boom in artificial intelligence (AI) and quantum computing will drive a spike in energy use, the National Grid has predicted.**

## A New Surge in Power Use Is Threatening U.S. Climate Goals

A boom in data centers and factories is straining electric grids and propping up fossil fuels.

In part, demand is being driven by a surge in data centers. Data center electricity consumption is expected to triple by 2030, equivalent to the amount needed to power around 40 million US homes, according to a Boston Consulting Group analysis.

CLIMATE TECHNOLOGY FUTURE PERFECT

## AI already uses as much energy as a small country. It's only the beginning.

The energy needed to support data storage is expected to double by 2026. You can do something to stop it.

But all that computing power comes at an environmental cost. Some studies have warned that the AI industry alone could consume as much energy as a country the size of the Netherlands by 2027.

Official data showed that in the Republic of Ireland, which is home to the European headquarters of several big tech firms such as Google and Facebook-parent Meta, data centres accounted for nearly a fifth of all electricity used in 2022.

The amount of electricity being used by data centres in the country has risen by 400% since 2015 and ignited debate about capacity.

One reason for such an increased demand for data centers in the U.S. is the dramatic rise of generative artificial intelligence (AI), which requires power on a scale not seen before, —as much as 300 to 500 MW, according to the JLL report.

With tech giants like **Microsoft**, **Facebook** and **Google** all investing more in AI, and services like OpenAI and ChatGPT garnering hundreds of millions queries each day, the demand is expected to get even greater. AI is already benefiting the office market, as well.

A recent analysis by the International Energy Agency calculated electricity consumption from data centers, cryptocurrencies and AI could double over the next two years. The sector was responsible for around 2% of global electricity demand in 2022, according to the IEA.

The analysis predicted demand from AI will grow exponentially, increasing at least 10 times between 2023 and 2026.

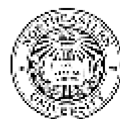
# CUbiC Vision

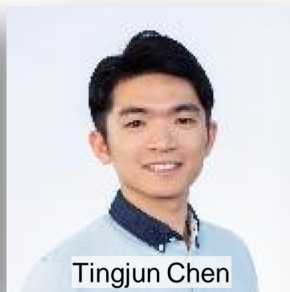
Flatten the computation-communication gap at both the Edge and the Cloud to deliver seamless Edge-to-Cloud connectivity with transformational reductions in the global system energy consumption.

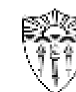
## Grand Challenge:

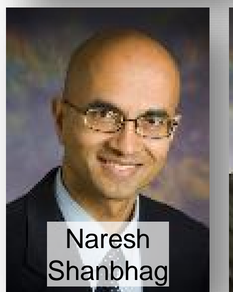
**Realize robust, scalable Edge to Cloud connectivity at > 10 Tbps with sub-pJ/bit energy efficiencies while enhancing bandwidth densities by >100X over capacity-constrained channels**

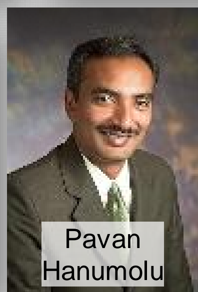
# CUbiC’s 23 PIs from 15 Universities

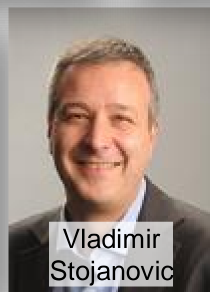


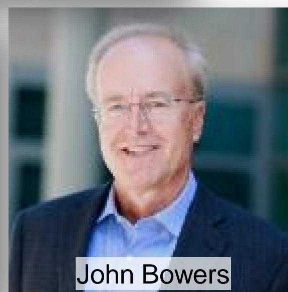


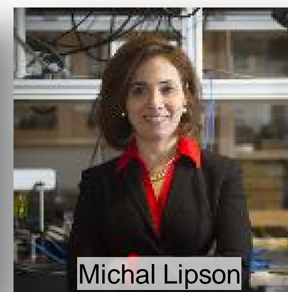


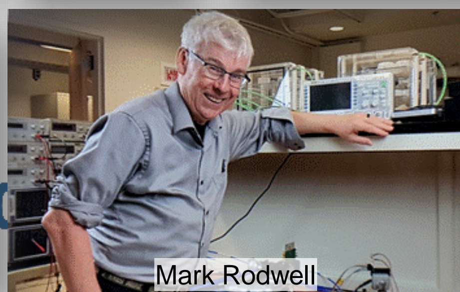


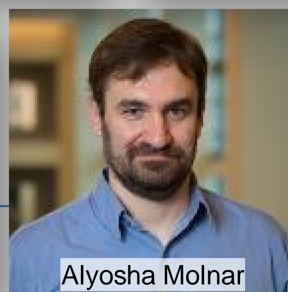











# CUbiC – Year 1 Overview

- Currently 98 graduate students, 12 postdoctoral fellows, and 17 undergraduate students
- Keynotes and Invited Talks: 45
- Publications: 42
- Awards Received: 10
- Internships and Employments (SRC Company): 14
- Internships and Employments (non-SRC Company): 6

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# CUbiC - Key Accomplishments

| Goal | Accomplishment |
|---|---|
| 1. Comprehensive benchmarking metrics: system level to uncover bottlenecks, and drive advancements in wireline and wireless technologies. | ✓ **Excellent Progress:** Benchmarking metrics identified across all task and theme levels |
| 2. Provide SRC scholars immersive training within the framework of JUMP 2.0 for broad understanding of technical challenges from industries and stakeholders. | ✓ **Excellent Progress:** Initiated scholar-led workshops – direct training, close interactions with industry partners, and deep understanding of technical challenges |
| 3. Establish robust connections for synergy with other JUMP 2.0 centers, inform on technical approaches of CUbiC and gather external feedback on use cases | ✓ **Progress:** Fostered strong collaborations across other JUMP 2.0 centers, including PRISM, CHIMES, ACE, COGNISENSE, and COCOSYS. |
| 4. Integrate photonic switching and connectivity into the Socket-to-Socket Distributed AI/ML/HPC Fabric Platform (SoSFab) to drive system-level performance. | ✓ **Progress:** CUbiC Retreats - Developed a comprehensive plan to integrate photonic switching and connectivity into SoSFab testbed. |
| 5. Prototype essential testbed components, such as baseband processing and beamforming units, utilizing local testbeds, and expand the CUbiC Real-time Antenna-to-Compute Testbed (ReACT) for comprehensive experimentation. | ✓ **Progress:** CUbiC Retreats - Developed a detailed plan to prototype essential wireless components leveraging the ReACT testbed. |

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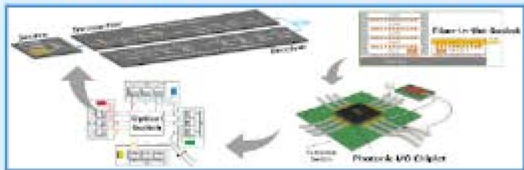
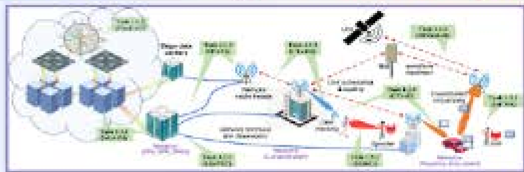
# Vertically Integrated Research Organization

**Theme 2: Wireline and Lightwave Interconnects**



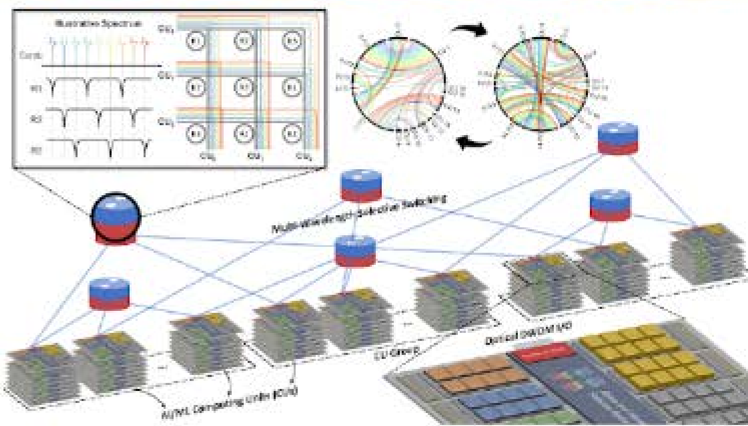
**Theme 1: Connectivity Networks and Systems**

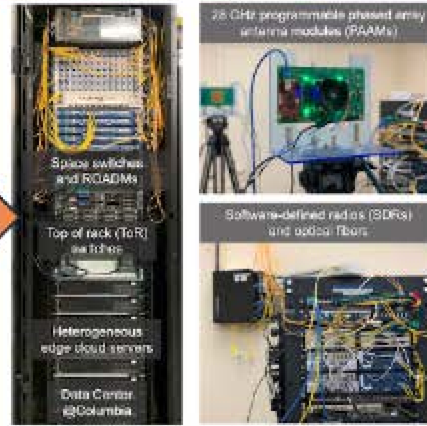


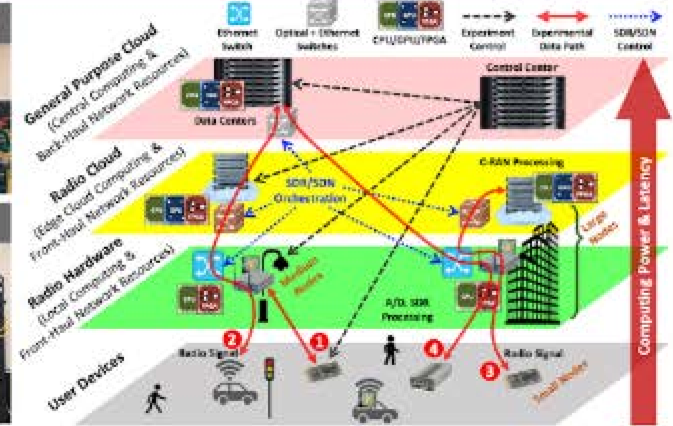
**Theme 3: Wireless Circuits and Technology**

- 1.1 Terabit/s PHY Systems
- 2.1 Systems & Algorithms for Connectivity
- 3.1 Large-Scale Millimeter-wave Arrays
- 2.2 Circuits & Architectures for Links
- 3.2 Wideband HDR Analog Signal Processing Interfaces
- 2.3 Circuits & Architectures for Switches
- 1.2 Cross-layer Design of Terabit/s Networks
- 3.3 High-Dimensional DSP for Emerging Wireless
- 1.3 Security and Resiliency
- 2.4 Photonic Devices for Connectivity
- 3.4 Heterogeneous Technologies for Next Generation Wireless
- 1.4 System Connectivity Platforms

**SoSFab** **ReACT**





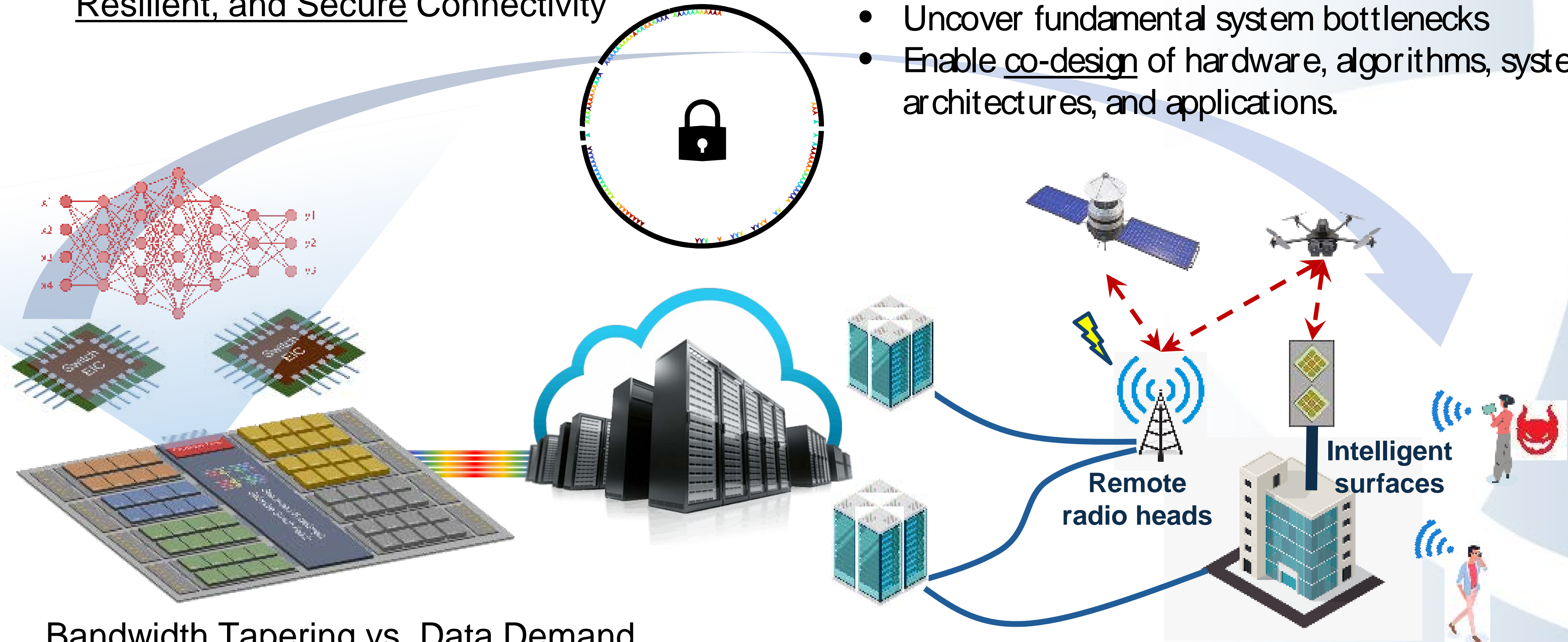



# Theme 1: Addressing System Connectivity Challenges

Enabling Cross-Layer Seamless, Adaptable, Resilient, and Secure Connectivity

**System applications driven connectivity challenges:**

- Inform and drive technologies in Themes 2 and 3
- Uncover fundamental system bottlenecks
- Enable co-design of hardware, algorithms, system, network architectures, and applications.




Bandwidth Tapering vs. Data Demand
Informing Theme 2

Edge Ubiquity vs. High-Frequency Challenges
Informing Theme 3

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# Theme 1 – Technical Highlights

## Photonic Networks

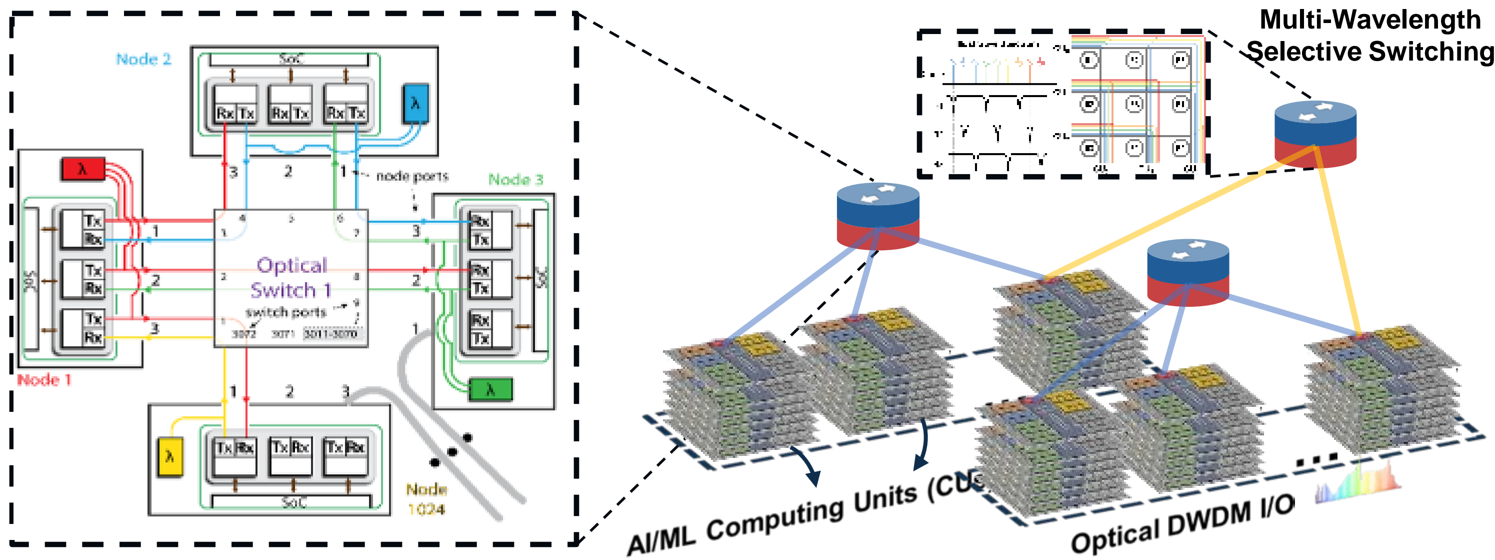
- **FlexPAC:** Photonic-enabled memory pooling architecture and mode-wavelength division multiplexing enabled optical multicasting.
- **ALfrEd**: Develop the algorithmic and systems foundations for building application-aware clusters.

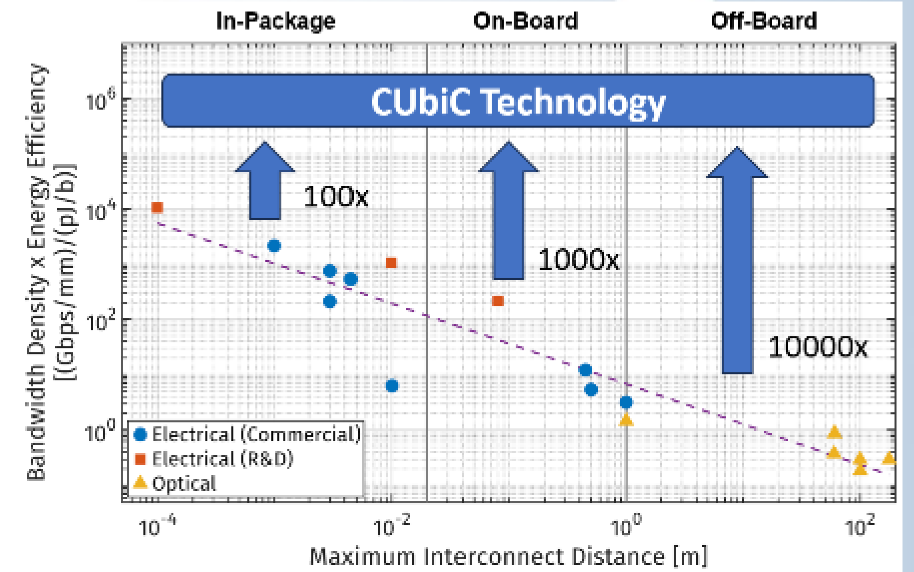
## Wireless Networks

- **CLaRA**: assessed Intel's vRAN accelerator's decoding throughput and energy consumption, then integrated it with a CPU-based baseband processing framework.
- **ReACT**: developed a 1 GSa/s real-time wideband transmission system utilizing the RFSoC Gen-3 ZCU216 evaluation board.

OFDM symbols with 256 QAM send by the RFSoC board

# Theme 2: Addressing Connectivity Challenges Within the Cloud




| Performance | SOTA | CUbiC 2024 | CUbiC 2028 |
|---|---|---|---|
| Shoreline BW density | 0.1 Tb/s/mm | 5 Tb/s/mm | 10Tb/s/mm |
| Link Energy Efficiency | 5 pJ/b | 0.5 pJ/b | 0.1pJ/b |
| per-fiber bandwidths | 0.8 Tb/s | 1.6Tb/s | 10Tb/s |
| Off-package bandwidth | 3 Tb/s | 50Tb/s | > 200Tb/s |

- The CUbiC Approach: **a pervasive socket-to-socket photonic connectivity** across 10,000s of GPUs
  - Photonic connectivity is both ultrafast and energy-efficient
- Advanced Technology Portfolio: >100s of wavelengths comb lasers, MEMs optical switches, coherent modulation, low-latency error correction, secure energy efficient DSP

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# Theme 2: Wireline Metrics and CUbiC's Goals

| Copper | Technology Comparison | Total Data Rate [Tbps] | Size [mm × mm] | BW Density (Shoreline) [Gbps/mm] | BW Density [Gbps/mm$^2$] | Energy [pJ/b] |
|---|---|---|---|---|---|---|
| Chip-to-Chip (mm to cm) | SOTA[1] | 9.984/32 | 1.0 × 1.5 | 8000 | 5333 | 0.44 |
| | **CUbiC** | **19.96/64** | **1.0× 1.5** | **16000** | **10666** | **0.1** |

| Copper | Technology Comparison | Per Lane Data Rate [Gbps] | Loss [dB] | BW Density (Shoreline) [Gbps/mm] | BW Density [Gbps/mm$^2$] | Energy [pJ/b] |
|---|---|---|---|---|---|---|
| Board-to-Board (cm to 10m) | SOTA[2] | 112 | 48 dB | N/A | 244 | 4.63 |
| | **CUbiC** | **224** | **60 dB** | **N/A** | **488** | **1.5** |

[1]SOTA for chip-to-chip are iso-area; [2]SOTA for board-to-board are for DSP-based links (high-loss channels)

| Photonic | Technology Comparison | Total Data Rate [Tbps] | Size [mm × mm] | BW Density (Shoreline) [Gbps/mm] | BW Density (Area) [Gbps/mm$^2$] | Energy [pJ/b] |
|---|---|---|---|---|---|---|
| Board-to-Board (cm to 10m) | SOTA | 0.8 | 89.4*18.35 | 44 | 0.5 | 17.5 |
| | **CUbiC** | **16.4** | **8.1 × 8.62** | **2024** | **234.8** | **0.8** |
| Long Distance (10m to km) | SOTA | 3-8 | 10-20 each side | 200-800 | < 150 | 2-6 |
| | **CUbiC** | **> 16** | **< 8 × 8** | **> 2000** | **> 5000** | **< 0.8** |

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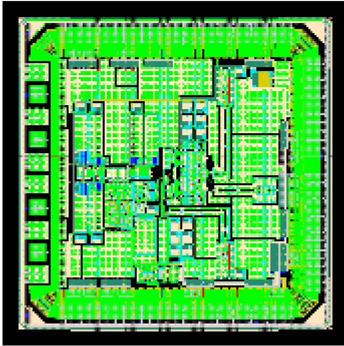
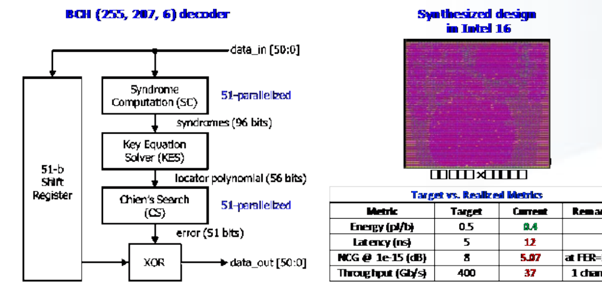
# Theme 2 - Electrical Connectivity Highlights

## Coherent Optics in the Data Center



**Highlight:** Designed and Taped out a 100Gb/s SP-16QAM receiver in 28nm CMOS. Chip estimated highly power-efficient, using only 3pJ/bit.

## Programmable Energy-efficient DSP Architectures

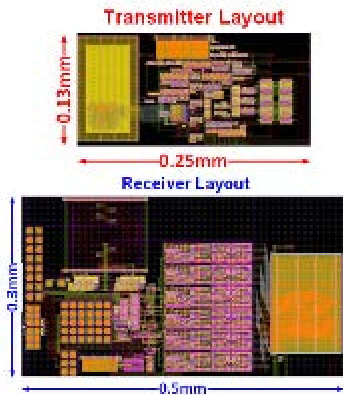



Target vs. Realized Metrics

| Metric | Target | Current | Remarks |
| --- | --- | --- | --- |
| Energy (pJ/b) | 0.5 | 0.4 | |
| Latency (ns) | 5 | 12 | |
| NCG @ 1e-15 (dB) | 8 | 5.07 | at FER=1e-6 |
| Throughput (Gb/s) | 400 | 37 | 1 channel |

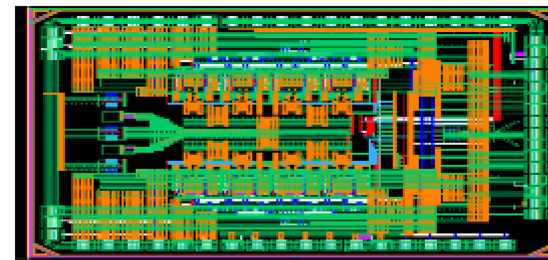
**Highlight:** designed a hard-decision decoder achieving energy-efficiency of < 0.5 pJ/b at a single channel throughput of 37 Gb/s and a coding gain of 5dB in Intel 16 (Tape-out - December'23)

## Machine Learning-inspired High-Speed Links




**Highlight:** designed and taped-out a PAM-4 50Gb/s transmitter and two versions of receiver in Intel 16nm targeting a FOM of 90 fJ/b/dB

## Adaptive Low-Cost High-Speed ADC



**Highlight:** designed a single channel ADC achieves a 56dB SNDR at ~5GHz input frequency, and 52dB SNDR at ~10GHz input frequency, with a power consumption of 27mW.

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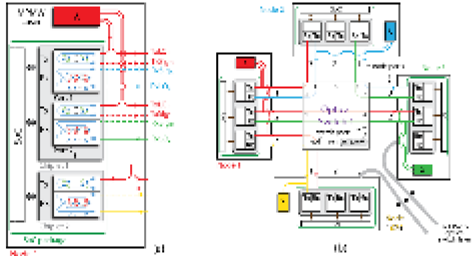
# Theme 2 - Lightwave Connectivity Highlights

## SuperFabric IO

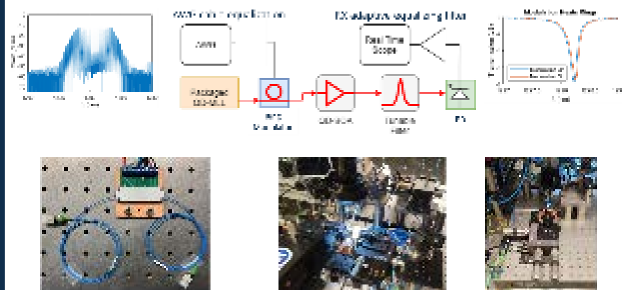


**Highlight:** developed laser-clock-forwarded coherent DWDM link, a pod architecture with a 1024-port optical switch, and a fast-lock simulation framework for DWDM receivers at 256Gb/s-to-1 Tb/s.

## SuperSwitch Controller

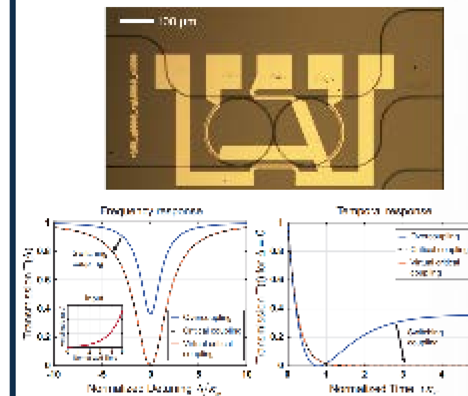
**Highlight:** The new SuperSwitch Controller is in the late stages of design in TSMC's 180nm BCD Gen2 high voltage process and the tapeout is scheduled to complete May 8th.

## Fiber-In-The-Socket



**Highlight:** demonstrated modulation link experiment with a packaged comb source and 1 Tbps DWDM silicon photonics components to achieve BER=2.9e-5

## High-bandwidth via Mode Coupling




**Highlight:** designed compact, broadband, and robust, multimode bends with insertion loss < 0.4 dB, and crosstalk < -12 dB for all 5 supported modes over a BW of > 200 nm; and a new photonic mode converter to converted fromTE0 to TE13

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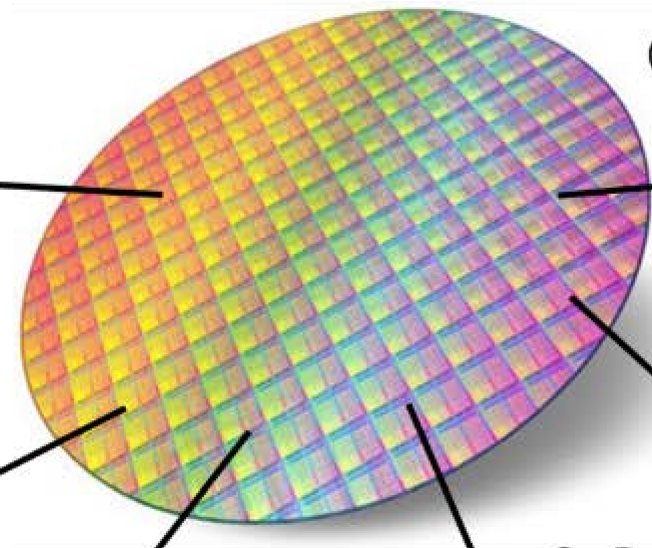
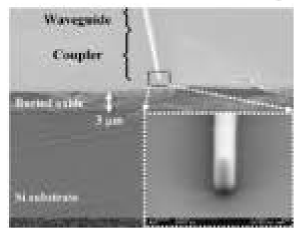
# Silicon Photonics Fabrication

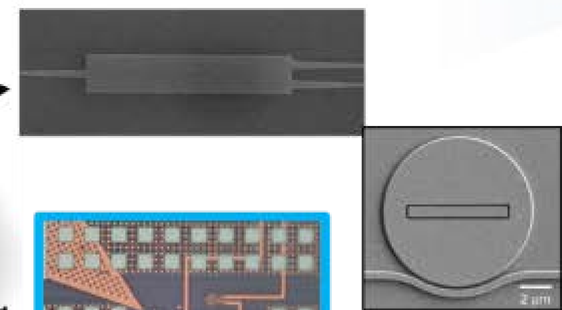
300 mm SOI Wafers



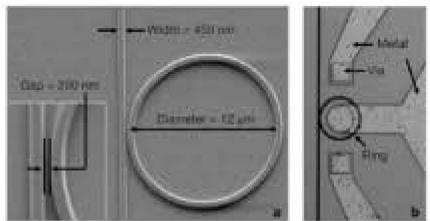
Low Loss
Chip Coupling



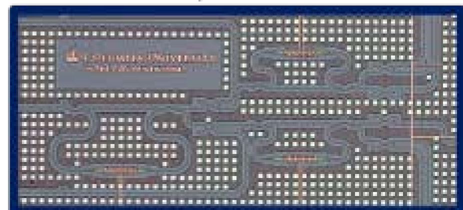

High Performance Passives
(splitters, filters, polarization control)



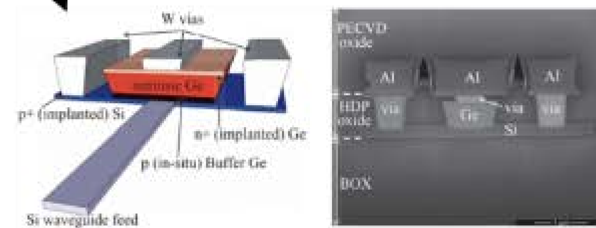

High Speed Modulators



Wavelength
interleaving



Ge Detectors



# Willow: CUbiC Full Photonic 300mm Wafer Tapeout

Stojanovic

Bergman

Low Loss Photonic Computing for ML

Pacakged Optical Switch

Reconfigurable Tranceiver for Space-Based Communications

Ring Assisted MZMs

128 Channel TX with Custom Disk Modulators

Silicon Nitride Kerr Combs

Updated MCM for 100 and 200 GHz Channel Spacing

MEMS Based Optical Switches

Custom Modulators:
a) Interleaved Junction Disk
b) Ridge Coupled Disk
c) THB Disk
d) Coaxial Junction Disk
e) Segmented PAM-4 Disk
f) Over coupled Ring Phase Shifter
g) Interleaved Disk with Half Etch Heater

Intel PIPES Multi-Tbps Tranceiver

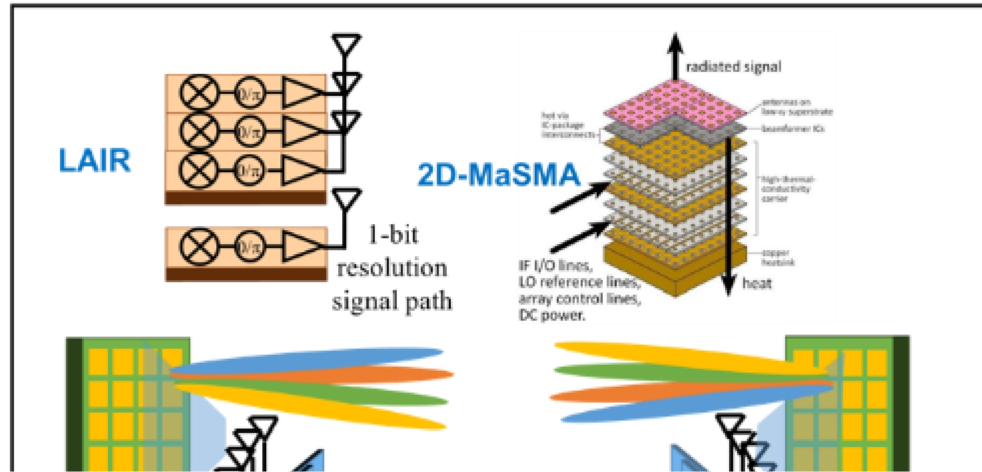
MDM + WDM Tranceivers

Lipson

Wu

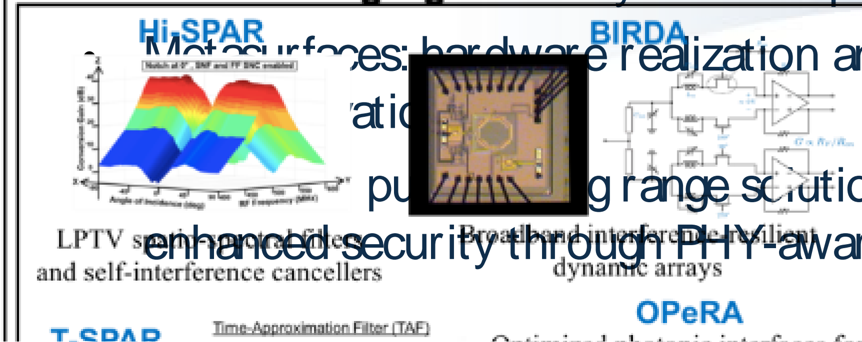
# Theme 3: Wireless Circuits and Technology

**Large-Scale Millimeter-Wave Arrays**




**Wideband High-Dynamic Range Analog Signal Processing Interfaces and High-Dimensional Digital Signal Processing for Emerging Wireless**

- Massive 1D and 2D arrays: RFIC + packaging
- Metasurfaces: hardware realization and system-




- ... range solutions with enhanced security through PHY-aware O-RAN

- Drive innovation in III-V technology for higher gain, output power and efficiency
- Thermal cooling to enable compact integrated solutions at sub-wavelength pitch

- ... dynamic ... arrays for reduced cost & power
- ... critical ... erence
- Cooling schemes for ... performance at low energy

**Heterogeneous Technologies for Next Generation Wireless**

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# Theme 3: Wireless Metrics and CUbiC's Goals

| **Single-channel transceivers** | Freq. GHz | Rate Gb/s | Range, m* | Modulation | Tech | Pout dBm | Noise dB | Transceiver Integration (WG=waveguide) | ele-ments | Who, when |
|---|---|---|---|---|---|---|---|---|---|---|
| JUMP1.0 | 202 | 36 | 7** | 16QAM | InP HBT | 15 | 8.5 | Integrated TX & RX ICs; antenna-in-package | 1 | UCSB, 2024 |
| **JUMP2.0** | **210** | **320** | **30** | **16QAM** | **InP HBT** | **17** | **8.5** | **integrated TX, RX ICs, antenna-in-glass** | **4x4 MIMO** | **CUBIC, 2025** |
| SOTA | 300 | 120 | 9.8 | 16QAM | InGaAs HEMT | 12 | 15 | multiple waveguide modules: 1 small IC in each | 1 | NTT, 2020 |

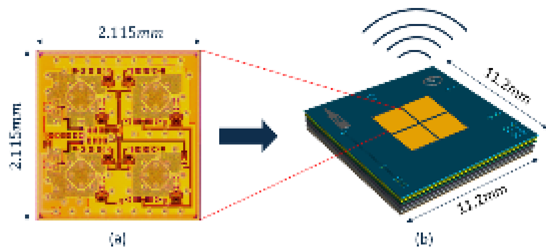
| **Single-beam arrays** | Freq. GHz | Rate Gb/s | Range, m | Modulation | Tech | Pout dBm | Noise dB | Transceiver Integration (WG=waveguide) | ele-ments | Who, when |
|---|---|---|---|---|---|---|---|---|---|---|
| **JUMP2.0** | **75** | **10** | **1200** | **QPSK** | **SOI CMOS** | **7** | **4** | **16 ICs, each 32 elements, antennas on PCB** | **512** | **CUBIC 2026** |
| **JUMP2.0** | **140** | **10** | **N/A** | **QPSK** | **SOI CMOS** | **10** | **5** | **4 ICs, 64 antennas in LTCC package** | **64** | **CUBIC 2026** |
| SOTA | ~ 64-element arrays at 75 GHz, no non-JUMP arrays at 140 GHz | | | | | | | | | |

| **MIMO HUBs** | Freq. GHz | Rate Gb/s | Range, m | Modulation | Tech | Pout dBm | Noise dB | Transceiver Integration (WG=waveguide) | ele-ments | Who, when |
|---|---|---|---|---|---|---|---|---|---|---|
| JUMP1.0 | 140 | 2.2 | 120 | QPSK | InP/CMOS | 20 | 7 | InP and CMOS ICs on LTCC | 1x8 | Samsung/UCSB |
| JUMP1.0 | 140 | 140 | 1 | 64QAM | CMOS | 17 | 8 | CMOS ICs on organic interposer | 1x4 | BWRC |
| **JUMP2.0** | **140** | **180** | **10** | **64QAM** | **CMOS** | **8** | **8** | **CMOS IC's with on-chip antennas (> 30 dBm EIRP)** | **4x4** | **CUBIC 2025** |
| **JUMP2.0** | **140** | **10** | **N/A** | **QPSK** | **SOI CMOS** | **10** | **5** | **64 elements (4 ICs)** | **64** | **CUBIC 2026** |
| **JUMP2.0** | **75** | **16x10** | **700** | **QPSK** | **CMOS** | **7** | **4** | **16 CMOS ICs, each 32 elements** | **512** | **CUBIC 2027** |
| SOTA | No MIMO arrays demonstrated outside the JUMP1.0 and JUMP2.0 programs above 100 GHz | | | | | | | | | |

*with single-channel transceivers, increased antenna gain increases range but makes aiming harder: instead compare $P_{out}$ and Noise.
**Room-limited, needed beam attenuator to prevent RX overload

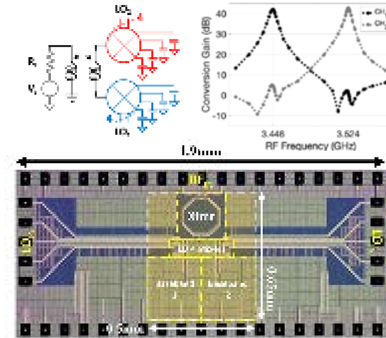
# Theme 3 – Technical Highlights

## Large Scale Millimeter-Wave Arrays



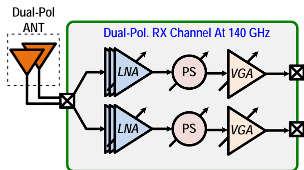

- **LAIR**: 4 Rx and Tx channels, are realized in small footprint of 2.1mm by 2.1mm
- **BIRDA**: Radar testing at 140 GHz to demonstrate the ability to cancel nearby reflections

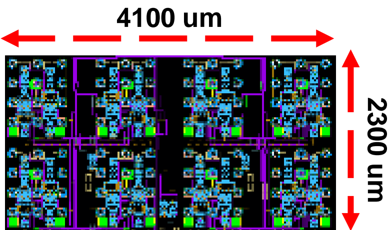
## Wideband High-Dynamic-Range Analog Signal Processing Interfaces




- **HI-SPAR**: Highest performance and lowest power 8-Phase mm-Wave mixer published, RFIC'24
- **T-SPAR**: Proposed Asymmetric Poly-Phase LO RX with Nonuniform Multi-level Time Approximation Filter

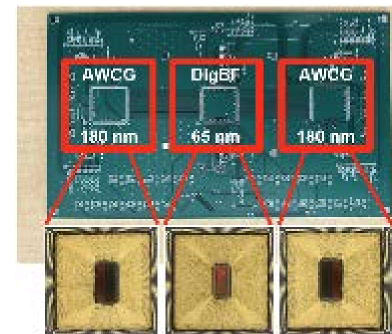
## Active and Reflect Arrays




- **2D-MaSMA**: Demonstrate first 2x64 element array with dual-pol with ~100 Gbps;
- **RE-AIM**: Creation of an active metasurface tile, utilizing on-chip antennas for ease of scalability and addressing its challenges

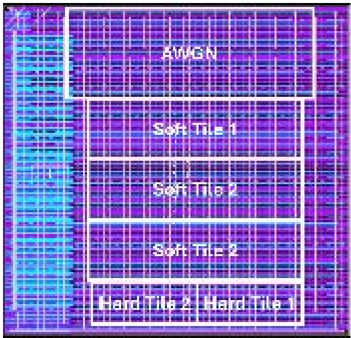
## RF-to-Photonic Interface for MIMO Arrays




- **OPeRA**: For Massive MIMO with ~1000 receivers, use photonic link with WDM to converge to DSP. Test using with Arbitrary MU-MIMO Waveform Generator with QAM modulated users.

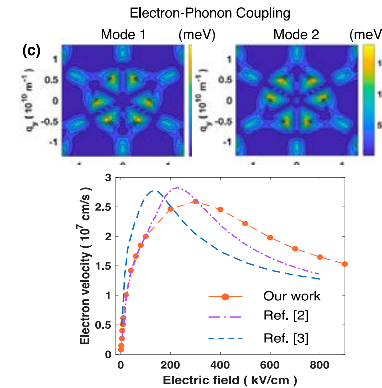
# Theme 3 – Technical Highlights

## High-Dimensional DSP for Emerging Wireless



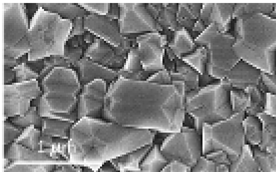

- **ADAPT:** Established tiled parallel processing architecture for massive MU-MIMO and demonstrated the efficiency of beamspace processing
- **PAYGO:** Demonstrated SOTA open FEC (OFEC) decoder chip (11.4mm2 in Intel16):40.2 Gbps at 17.4 pJ/b/iter.

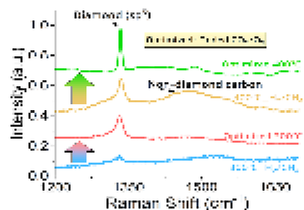
## High Power GaN Transistors




- **EVO:** Development of a gate-first process to enable aggressive lateral scaling of N-Polar GaN HEMTs to improve RF performance, and of in-house full band Monte Carlo simulator for GaN which matches published data.

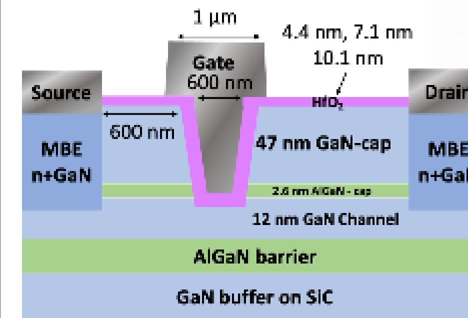
## Diamond-based Thermal Management for GaN and InP






- **D-Therm:** Lowering the growth temperature from conventional growth temperature (650-700℃) to 350-400℃. Achieved high quality and isotropic diamond grain structure with enhanced thermal conductivity.

## Heterogeneous Technologies for Next-Gen Wireless




- **EVO:** Record single transistor output power at W-band
- **GOG:** A record high electron mobility of 2000 $cm^2/Vs$ has been achieved near pinch off (charge density of $2x10^{12}$ $cm^{-2}$)

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# CUbiC System Connectivity Platform 1: SoSFab: Distributed AI/ML/HPC Fabric

- **Vision:** A system-wide energy-efficient demonstration of CUbiC data center platform
- **Approach:** Co-optimize and co-design from applications to devices to exploit synergies across the system stack, application requirements, and device capabilities.
- **Outcome:** End-to-end application demonstration CUbiC's ubiquitous connectivity that scales to meet the needs of emerging distributed data-centric applications, such as machine learning training and inference.

- Only known platform that enables adjusting the network topology, communication collective, parallelization strategy, and workload scheduling for AI/ML/HPC workloads.
- Cooperation with the JUMP2.0 ACE Center (UIUC)

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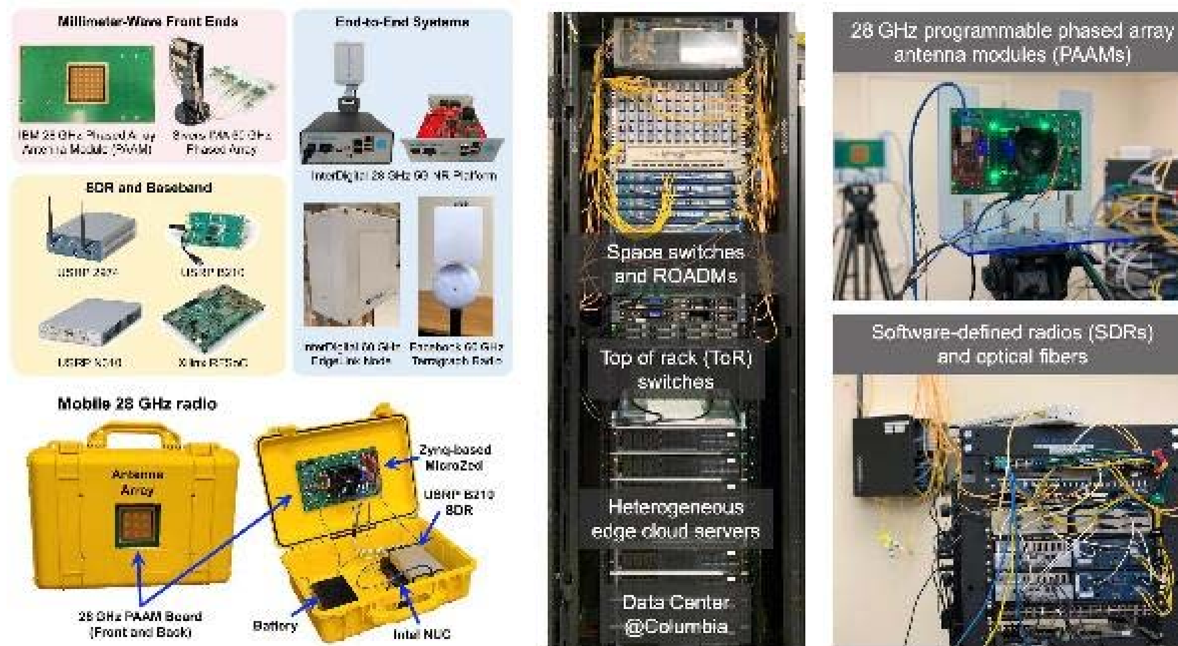
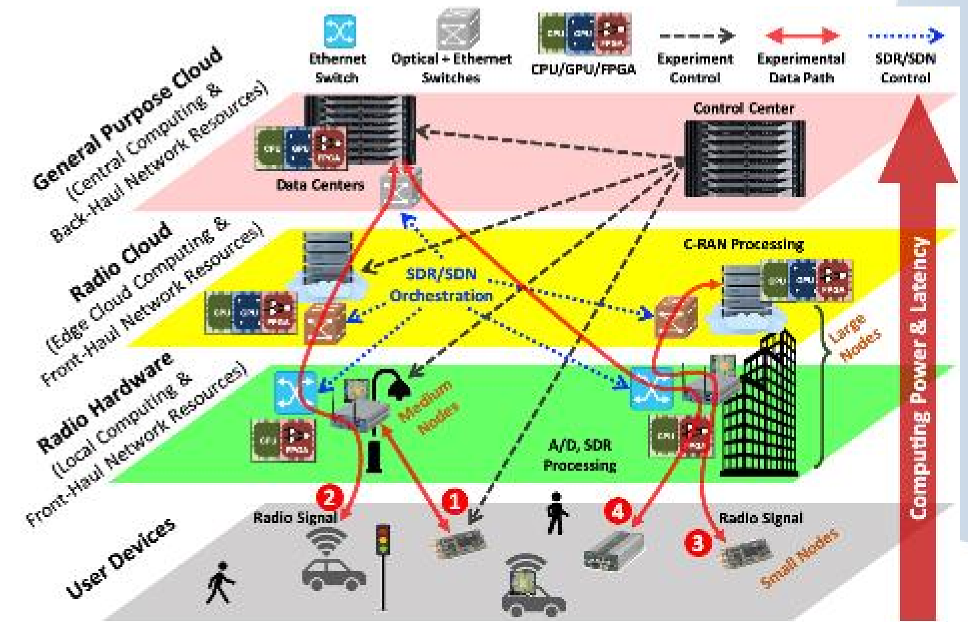
# CUbiC System Connectivity Platform 2: ReACT: Realtime Antenna to Compute

- **Vision:** a center-wide demonstrations of wireless connectivity from antenna to compute
- **Approach:** translation from advanced mm-Wave ICs developed in CUbiC labs to a programmable radio platform, O-RAN for system-level evaluation and network-level experimentation.
- **Outcome:** center-wide demonstrations that will take a holistic system approach to integrate the unique mm-Wave frontend and digital circuits, and provide the evaluation of the advanced algorithms and control plane – robust, secure

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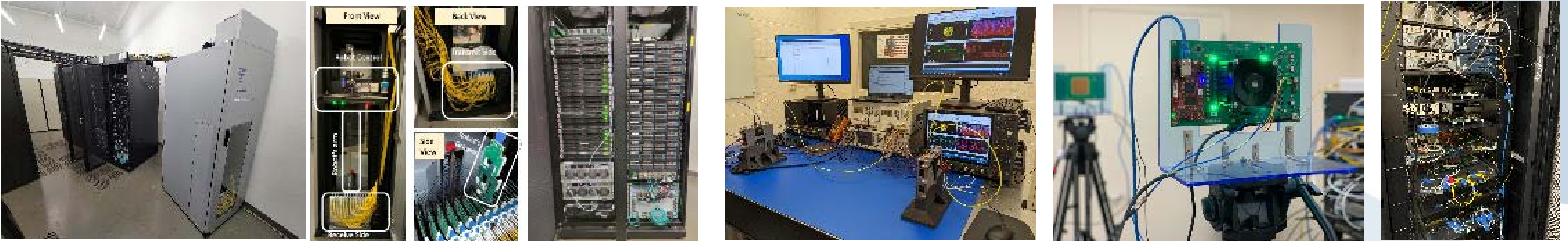
# 2 Retreats – Building on Intra-CUbiC Collaborations

- CUbiC organized two virtual winter retreats on January 19th and 26th, 2024
- Facilitated discussions on Theme 1 combined with Theme 2, as well as Theme 1 combined with Theme 3, focusing particularly on testbed explorations.
- Critical for strategy alignment and progress tracking on tasks
- Retreat insights served as guidance for the execution of tasks within the center
- Each retreat attracted over 100 attendees joining from across the center.

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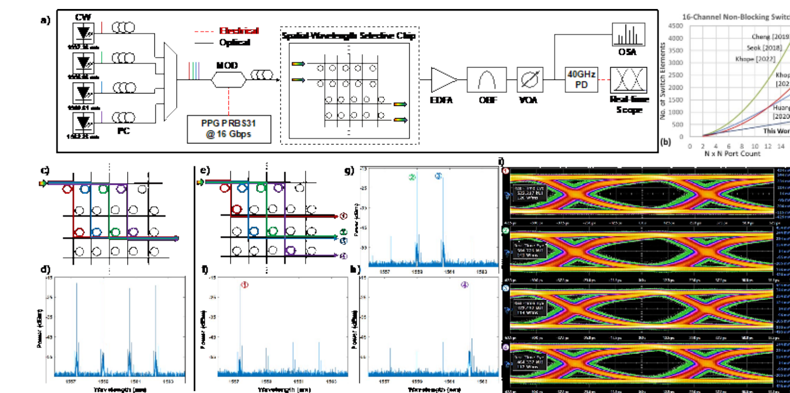
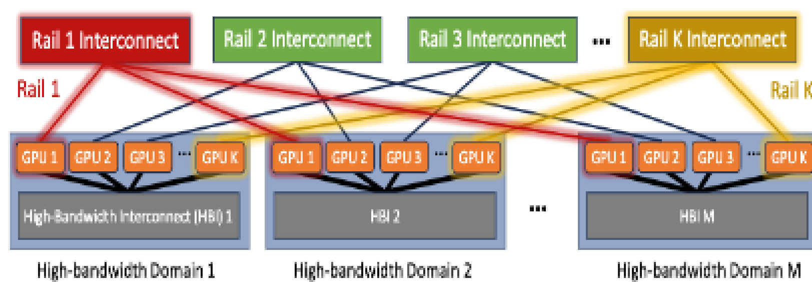
# Intra-CUbiC collaboration via SoSFab testbed

- Testbed system with adaptable photonic switch fabric – demonstrating scaled applications speedup
- T1/T2 Collaboration – Insertion of MEMs switch fabric, Optical NIC, and Wavelength-selective switching
- Reshaping landscape AI/ML scaling, data center efficiency, and network optimization




**SoSFab platform: Optical Network Interface**

PIC – 2 x 16-Channel

Ceramic Interposer

PCB – RF and Low-Speed Routing

Fibre

PIC

EIC

Interposer

ONIC PCB

FMC FMC

FMC FMC

PCI Express Gen4 Development Platform PCB with FPGA

HTG 930 – PCIE to Host Server

Receiver BER < $10^{-12}$ up to 25Gbps/λ

**First optically-packaged ONIC, connected to HTG 930**

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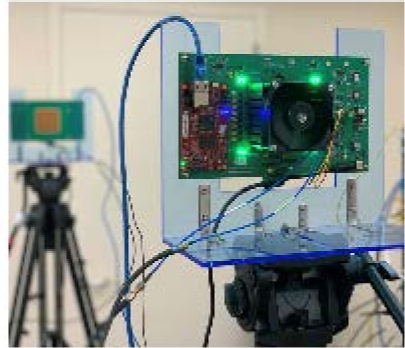
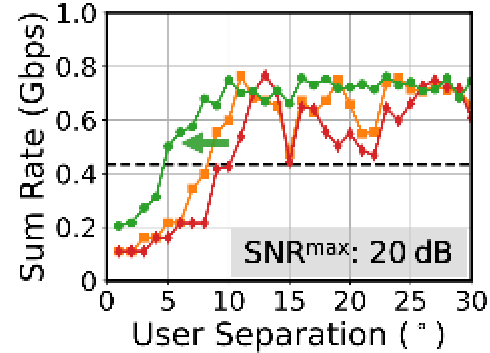
# Intra-CUbiC collaboration via ReACT testbed

- Ongoing algorithm development & experiments with Testbed (with current state of the art hardware)

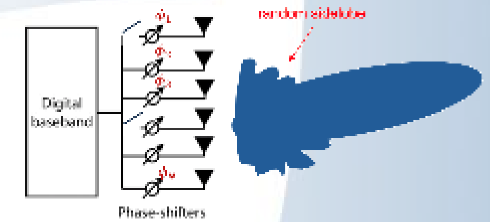
Interference-free MU-MIMO with closely spaced users






**IBM 28-GHz PAAM connected to USRP SDRs**

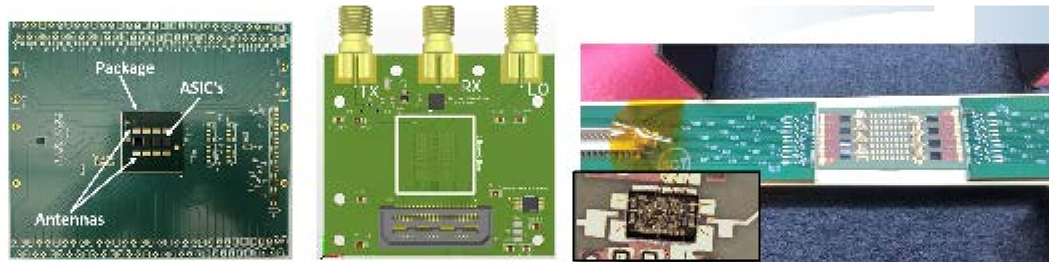
Array calibration and compressive tracking




**Sivers 60 GHz arrays**

**T1/T3 collaboration for Phase 2 Testbed**

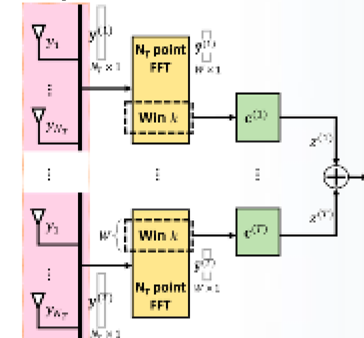
Integrating CUbiC hardware

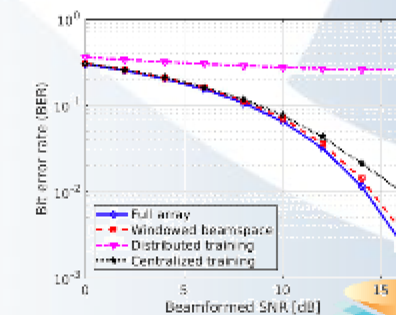



All-CMOS 140GHz MIMO Hub Module (Niknejad) | 8x8 140GHz TRX Module with 50dBm EIRP (Rebeiz) | Gen-II 140GHz MIMO Hub Module (Rodwell)

**T1/T3 collaboration between SPATS/ADAPT tasks**

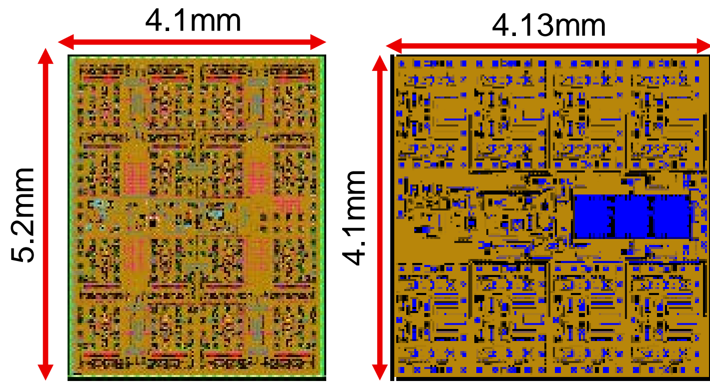
Beamspace DSP for tiled massive MU-MIMO



# Intra-CUbiC collaboration via ReACT

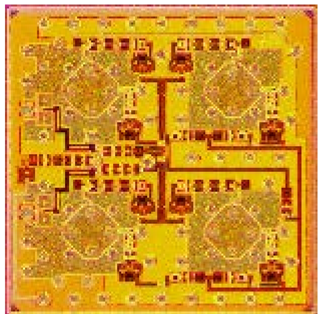
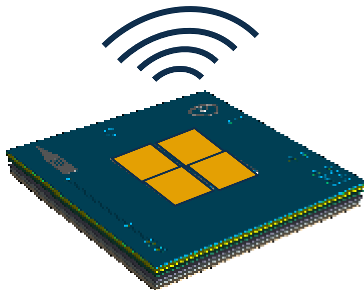
- Prototyping advanced system with integration of CUbiC hardware (Phase 2)



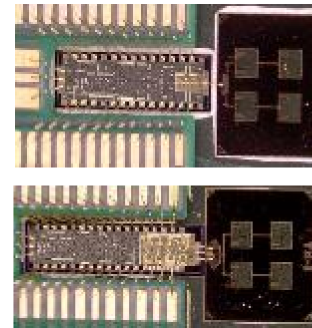

Columbia 140GHz 4x4 Beamforming TX Array (Under measurement)

UCSD 140GHz Link Demonstration

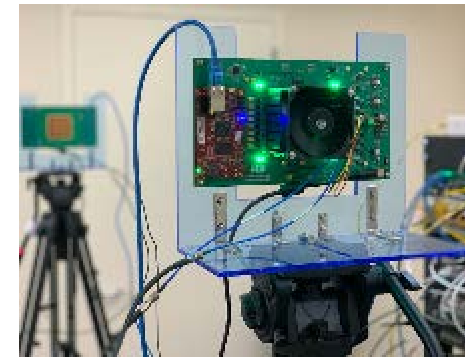
UCSD 140GHz Link Demonstrated at Columbia at the Annual Review Meeting (Collaboration between UCSD and Columbia)

Berkeley 140GHz Cobra LAIR Array (Under measurement)



UCSB 200GHz 4x4 MIMO Link Demonstration



A real-time 28GHz polarization MIMO link demonstration (collaboration between Duke, Columbia and IBM)

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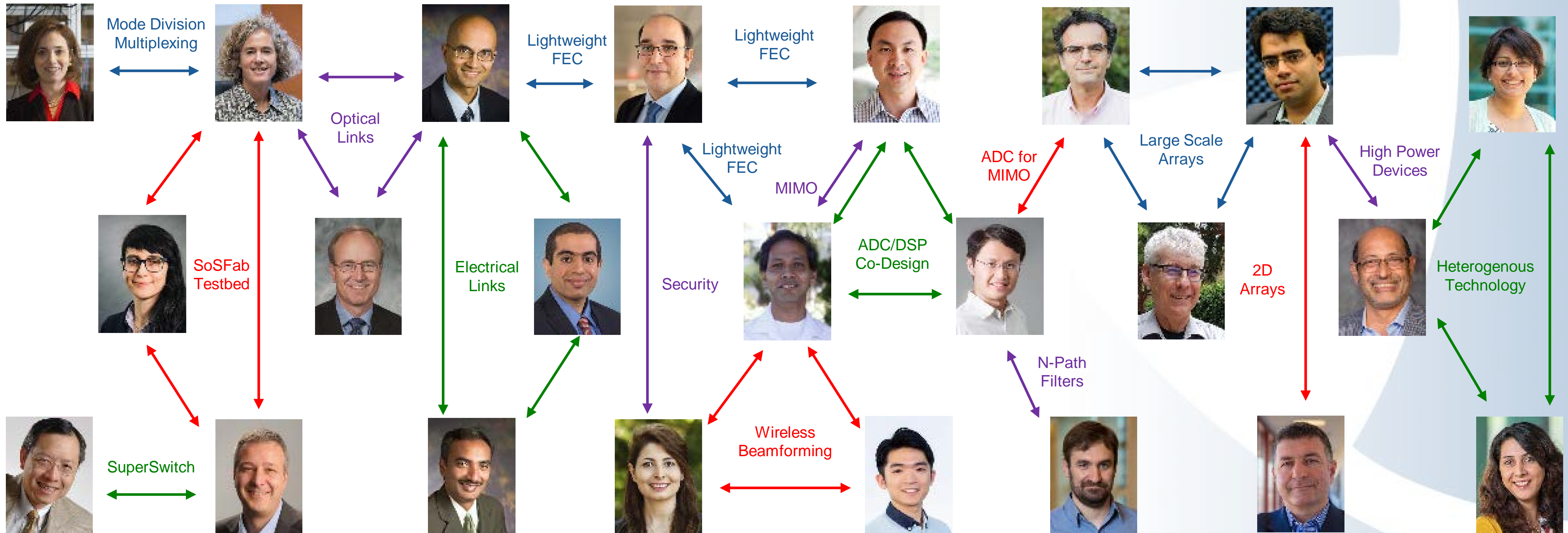
# Intra-CUbiC Collaborations

- Integrated collaborations between CUbiC PIs established and will keep growing.

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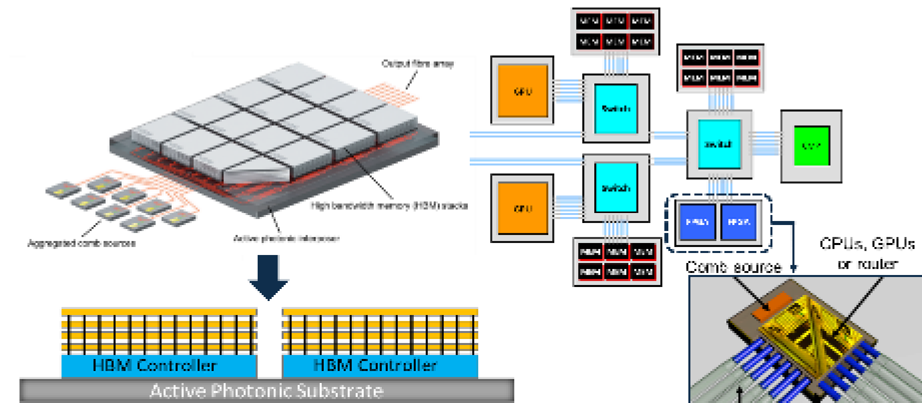
# Cross-Center Collaborations

## PRISM – CUbiC
Photonic Connected Memory

- Partner with PRISM (PIs: Zhao and Kim) for high-bandwidth photonic memory connectivity.
- Implement deeply disaggregated connectivity architectures



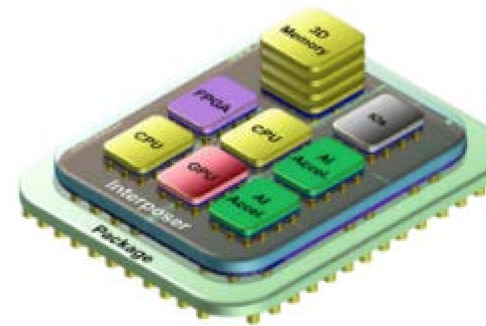
Bergman

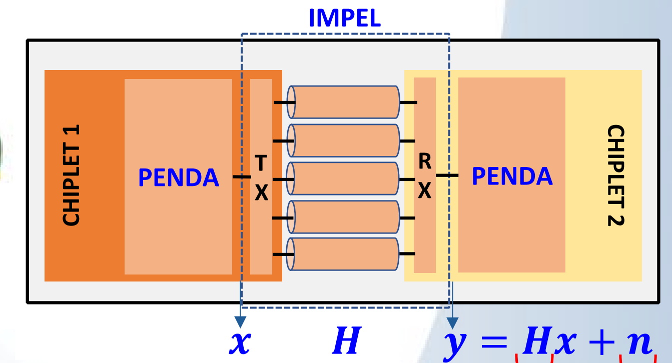
Zhao

Kim

## CHIMES – CUbiC
Enabling Dense Die-to-Die Interconnect

- Collaborate with CHIMES (PI: Bakir), Samsung, ADI, and Intel to develop 2.5D/3D package models.
- Explore advanced packaging options in partnership with Intel and A*Star to enhance packaging technologies.



Shanbhag

Kumar

Bakir

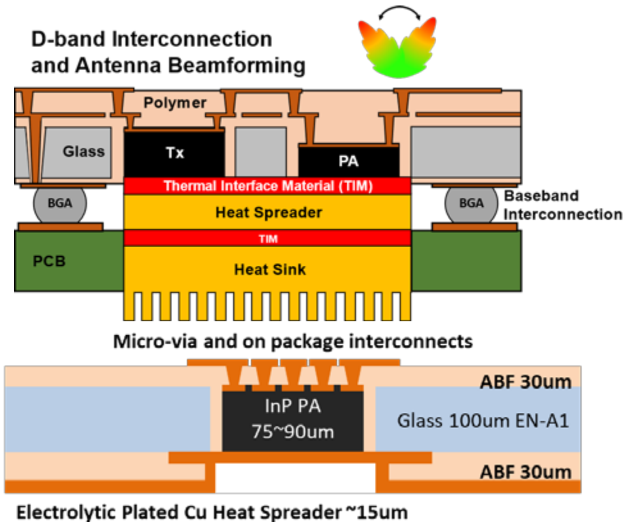
# Cross-Center Collaborations

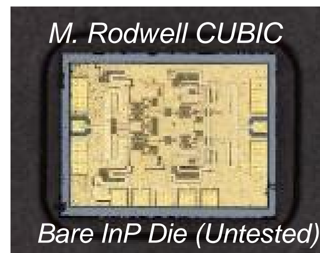
## CHIMES – CUbiC
### Packaging for high frequency wireless

- CUbiC-CHIMES: Collaboration continuing to demonstrate functional module with beamforming.
- First demonstration of functional packaged PA @ 140GHz using embedded InP dies in glass.

Swaminathan

Rodwell

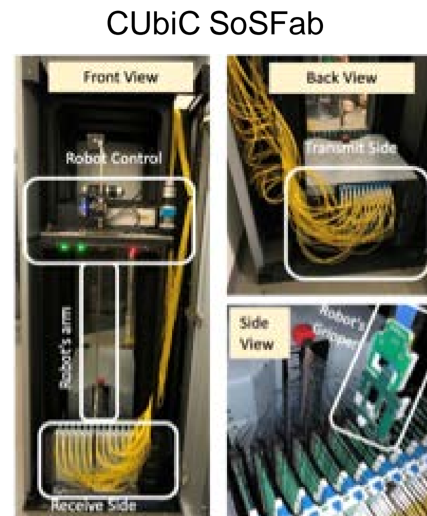


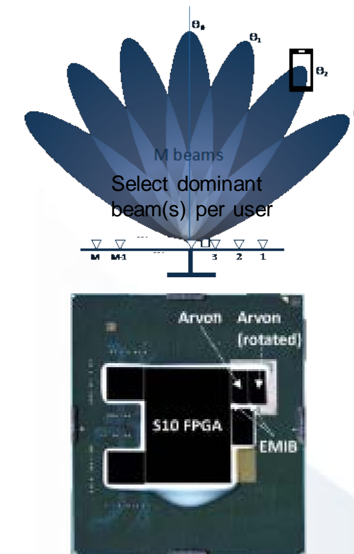



## ACE – CUbiC
### Photonic interconnection networks & Intel/Arvon co-packaged compute platform

- CUbiC-ACE collaboration drives reconfigurable datacenter architectures to accelerate AI/ML/HPC applications
- ACE task produces heterogeneously integrated compute platforms for the CUbiC wireless DSP workloads

CUbiC SoSFab



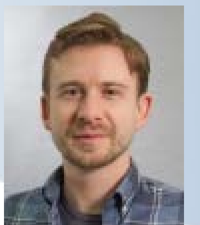




Intel FPGA + Arvon DSP co-packaged compute platform

Ghobadi

Krishna

Zhang


Belay

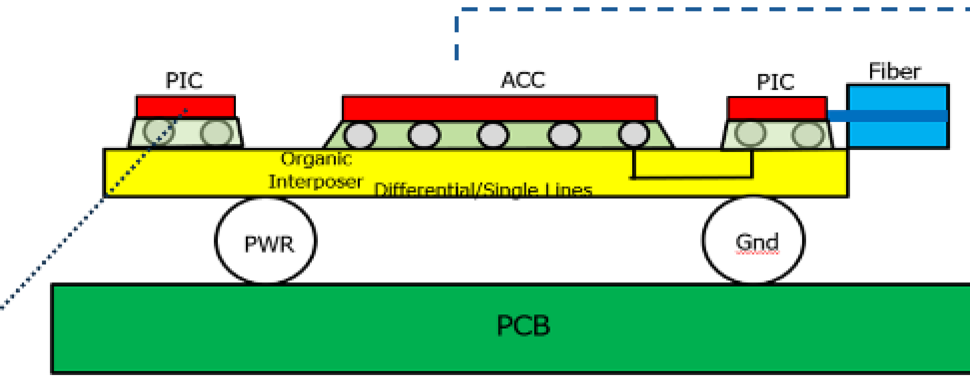
# Cross-Center Collaborations

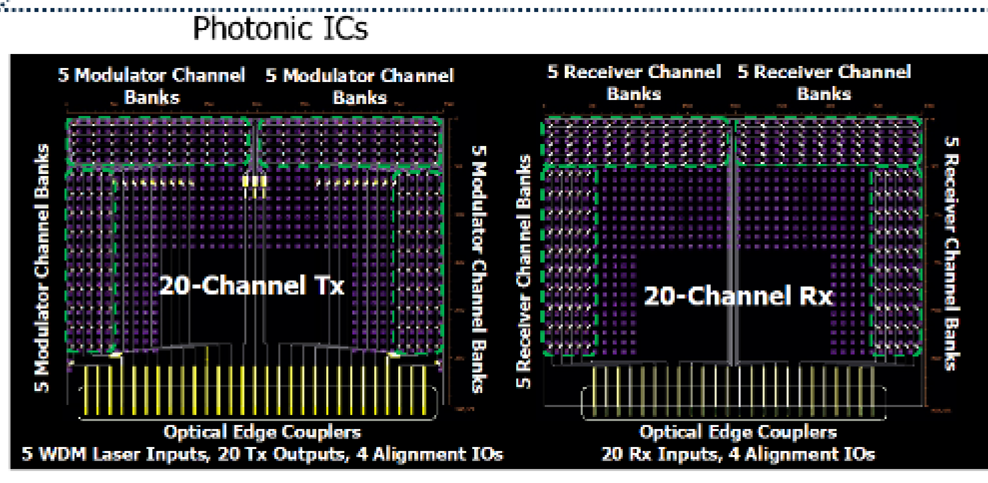
**COGNISENSE – CUbiC**
Photonic ASIC Integrated Accelerator

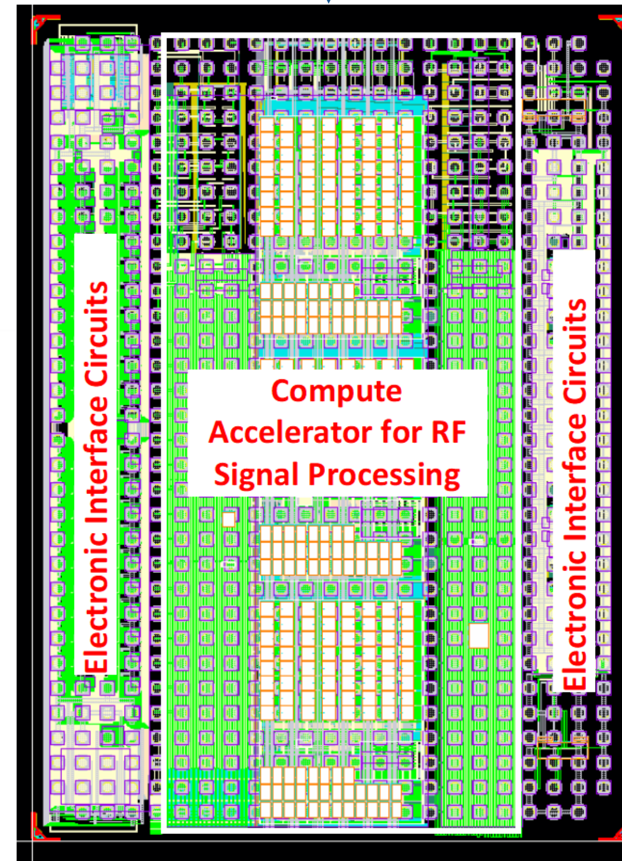
Mukhopadhyay

Seok

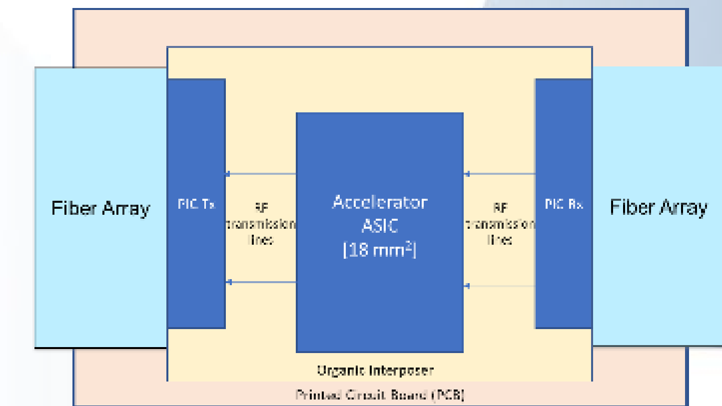
Bergman



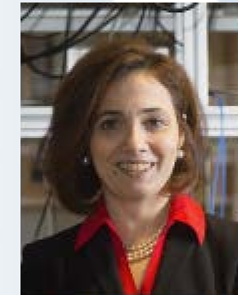




- Partner with COGNISENSE (PIs: Mukhopadhyay and Seok) on HI platform with co-integrated accelerator ASIC and PIC IO
- Building on DARPA DRBE collaboration (PM John Davies)
  - Mukhopadhyay, Romberg,
  - Pande, Swaminathan, Krishna
  - Bergman, Seok, Carloni



# CUbiC Broadening Participation Initiatives


Michal Lipson

Alex Meng

**Broadening Participation Pledge**

At CUbiC, our goal is to enrich and uphold the involvement of a diverse student population in research and educational endeavors. The CUbiC Principal Investigators are committed to cultivating an inclusive environment for students, regardless of their race, gender, place of birth, or academic level.

- CUbiC Scholar Leadership Council - Established scholar leadership council for the strategic management of workshops and the facilitation of BP initiatives.
- Summer Research Program - Designed for undergraduate students to advancing the needs of underrepresented groups in semiconductor-related research.
- Undergraduate Research - Initialize the integration of undergraduate students into CUbiC tasks. Several current undergraduates already admitted to graduate programs at CUbiC affiliate institutions.
- Joint Mentorship for Minority HS Students - Partnership with Science Honors Program, Summer Academic Program, and Young Women's Leadership Programs.

# Liaison Meetings and Scholar Workshops

- CUbiC has three themes, each holds Liaison Meetings every 6 weeks
- CUbiC has launched Student-Led Workshops in 2024 (held 20+ so far):

- **Dynamic Engagement:** Hosting 7 workshops every month, one per subtheme, with ~20-60 participants in each session, spanning diverse disciplines and industry.
- **Post-Workshop Interactions:** Presentations are posted on Pillar for post-workshop knowledge sharing, sparking over 50 discussions, and fostering collaborations.
- **Empowering Future Leaders:** Nurturing scholars potential through impactful sessions and industry-academia bridges for sustainable impact.

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# CUbiC's Integrated Team

Keren Bergman
Columbia
Center Director

Ali Niknejad
Berkeley
Center Co-Director

## Theme 2: Wireline and Lightwave Interconnects

- Pavan Hanumolu, UIUC
- Tejasvi Anand, Oregon State
- Naresh Shanbhag, UIUC, Theme Lead
- Vladimir Stojanovic, Berkeley
- John Bowers, UCSB
- Ming Wu, Berkeley
- Michal Lipson, Columbia
- Mike Chen, USC

## Theme 1: Connectivity Networks and Systems

- Manya Ghobadi, MIT, Theme Lead
- Tingjun Chen, Duke
- Upamanyu Madhow, UCSB, Theme Co-Lead
- Keren Bergman, Columbia, Center Director
- Yasaman Ghasempour, Princeton
- Hessam Mahdavifar, UMich

SoSFab — Leads: M. Ghobadi & V. Stojanovic

ReACT — Leads: T. Chen & H. Krishnaswamy

## Theme 3: Wireless Circuits and Technology

- Harish Krishnaswamy, Columbia, Theme Lead
- Ali Niknejad, Berkeley, Center Co-Director
- Mark Rodwell, UCSB
- Zhengya Zhang, UMich
- Gabriel Rebeiz, UCSD
- Umesh Mishra, UCSB
- Alyosha Molnar, Cornell
- Elaheh Ahmadi, UMich
- Srabanti Chowdhury, Stanford

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# Summary

- CUbiC will strive to flatten the computation-communication gap, delivering seamless Edge-to-Cloud connectivity with transformational reductions in the global system energy consumption.

- Vertically integrated research agenda cross-cutting 3 technical themes
- Outstanding team of 23 PIs from 15 Universities
- 37 Research Tasks
- Currently 98 graduate students, 12 postdoctoral fellows, and 17 undergraduate students

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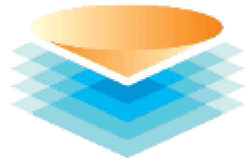
CUbiC

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