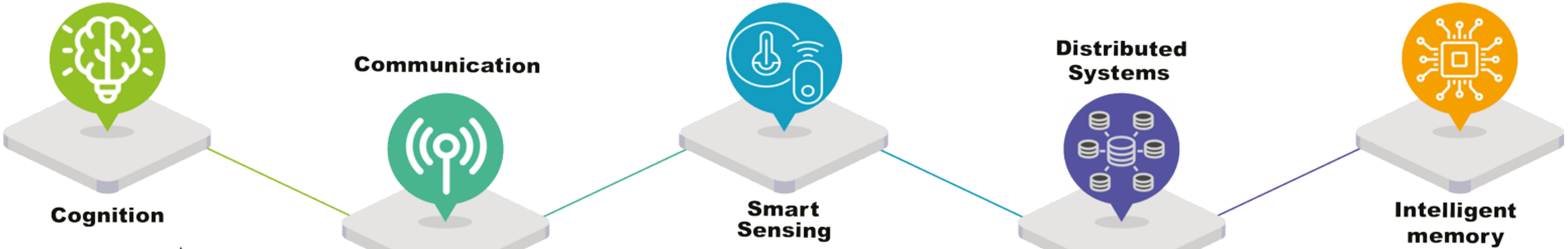
Semiconductor
Research
Corporation

SUPeRior Energy-efficient Materials and dEvices

April 24, 2024
SRC Leadership F2F Meeting, Samsung @ San Jose
Grace Huili Xing (Cornell), Center Director
Tomás Palacios (MIT), Co-Director
Chris Hinkle (ND), co-Lead on High-Throughput
Elton Graugnard (BSU), Thrust Lead on Advanced Processing
Thomas Dienel (Cornell) Managing Director, Jenna LaMendola (Cornell) Administrative Assistant

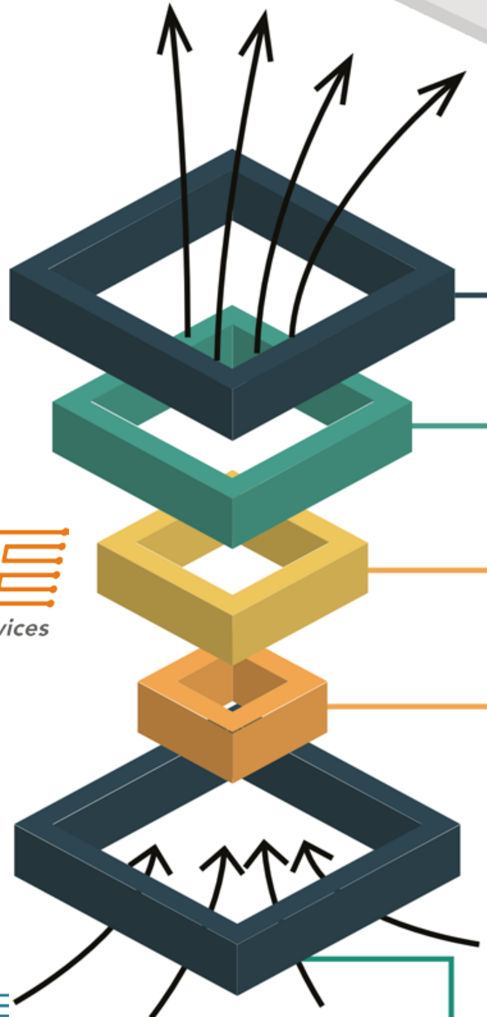
Cornell University · MIT · TEXAS The University of Texas at Austin · Rensselaer · CU · Yale · ND · Georgia Tech · UCSB · Stanford University · BOISE STATE UNIVERSITY · Northwestern University · NC State

SUPREME
SUPeRior Energy-efficient Materials and dEvices



Center Vision

SUPREME
SUPeRior Energy-efficient Materials and dEvices



Seismic Shifts *Bridging the gap and enabling the seismic shifts in ICT.*

Application-level Benchmarking *Meeting the workload demands of the future.*

Machine Learning & Artificial Intelligence
- -Hyperdimensional Computing models
- -Transformer Networks — GPT-3 and beyond
- -Recommendation Systems
- -Perception and Autonomy

Associative Memories
- -Key Value Storage
- -RF Intelligence
- -Bioinformatics

Physics-based Computing

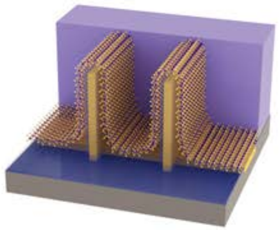
Augmented Memory Hierarchy

Impacts of Interconnects

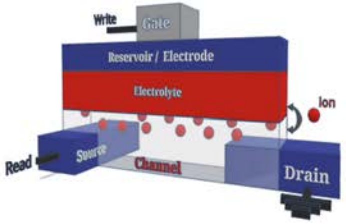
Secure Processing
- -Trusted execution environments
- -Homomorphic encryption

Devices & Interconnects *Accelerating innovations in Analog, Digital, Memory, Storage Devices, & Interconnects*

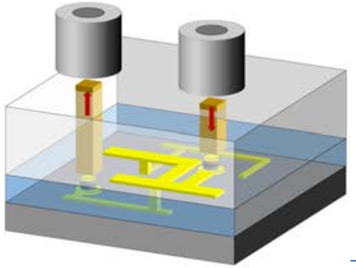
① **Analog & Digital**



② **Memory & Applications**



③ **Interconnects & Metrology**



④ **Materials Discovery & Processing:** *Taming new materials and new physics.*

25 PIs – One SUPREME

Chris Hinkle

Elton Graugnard

H. Grace Xing

Tomas Palacios

SUPREME Goals and Accomplishments—Year 1.3

Goal	Accomplishment
1. Center Management: Ensure that all partners meet the 95% spending goal annually, establish subawards timely, enable purchase of capital equipment to provide unique tools and capabilities for future success of the center, establish Pillar Science to disseminate all results, create a center website and newsletters for outward facing communication, and effective communication both within and outside the Center on job opportunities, broadening participation, enable collaboration with other JUMP2.0 centers by creating seed funds, annual PI meeting & review etc	✓ **Accomplished** ✓ **New:** Semi-annual Center Newsletters are planned, and the 1st sent in January 2024; Inter-center Seed funds created, proposals are ready for evaluation
2. Team Collaboration (PIs and students): Enable collaborative atmosphere for PIs and their groups to be aware of each other's work, broaden participation on all levels though center-wide initiatives, and to develop intracenter collaboration across thrusts and individual projects.	✓ **Accomplished**. We are at ~180 students and postdocs; **New:** Established Grad travel funds to carry out research in labs of other Center PIs
3. Team Collaboration (Liaisons, PIs, and students; other centers): Establish a culture that liaisons are extended researchers and mentors of the Center. Ensure that Liaisons and PIs are well-connected, including all team members (students, postdocs, etc.) to ensure a smooth exchange of ideas and facilitate outreach to other JUMP 2.0 centers for joint interest and expertise.	✓ **Excellent progress made**; topic-focused meetings help to increase coherence and connections between materials and device projects; **New:** Seed $
4. The SUPREME Materials Palette: The materials palette is the unique identity of SUPREME, central to all aspects of the Center research thus most effective in connecting all projects, all researchers, all liaisons and research methods. Learn how to manage a dynamic materials palette, implement the cycle of materials discovery combining theoretical predictions, experimental realization, and thorough characterization to expand or down-select the materials palette. Update and present the updated Materials Palette at the annual center reviews, or other venues if applicable.	✓ **Excellent progress made** ✓ Top Goal for Year 2: Continuously updating the materials Palette, single document listing metrics
5. New research methodologies: Implement new ways of research including machine learning and artificial intelligence (ML/AI) approaches towards high-throughput methods and automated materials discovery, explore inverse design for device design whenever applicable.	✓ **Good progress made** ✓ Top Goal for Year 2: to organize topical workshops

Highlights – Year 1.3

1. Growth of Center during year 1.3

- Students and Postdocs joined: 185
- Sponsor Liaisons at SUPREME projects: 107
- 11 FT hires, 15 interns at sponsors

2. Annual Review August 2-3, 2023

- 165 attendees at Cornell University

3. Annual Review June 11-12, 2024

- To be hosted at MIT, Building 45
- Planning for 150 on-site participants

4. Liaison Meetings weekly—exception apply

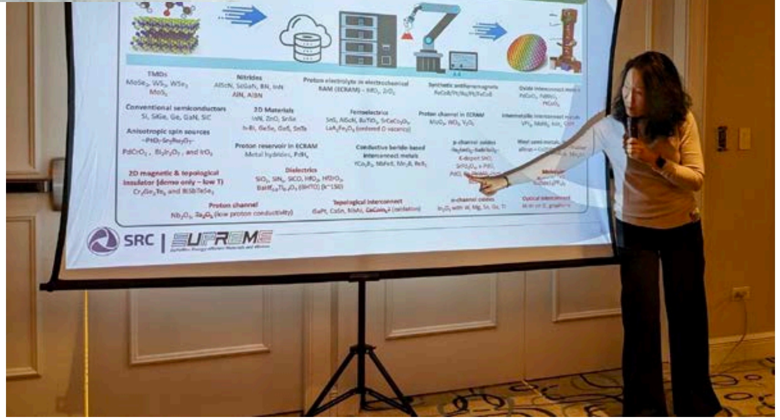
- Rotating through Thrusts/Topics of SUPREME
- Held 36 meetings, presentation materials on Pillar Science (TOC in Notes)
- At alternating times to balance time zones and availability

5. Broadening Participation

- Two BP Champions guide SUPREME's efforts
- Two awards established since 2023Q2/Q3
  - SUPREME Undergraduate Microelectronics Fellows (7 awarded)
  - SUPREME Undergraduate Travel Grant (4 awarded)
- Total number of undergrads working on SUPREME projects: 24

2023 August – annual review

2024 April - PI meeting



6. **Publications (on Pillar Science)**: 130+
7. **Keynotes**: 70+
8. **Awards**: 25+

24 Undergraduate Students


Deniz Erus (MIT)

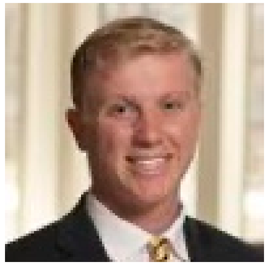

Jack Coyle (RPI)


Yufan Feng (Cornell)


Thomas Hieber (Notre Dame)


Andi Qu (MIT)


Clayton O'Dell (Notre Dame)


Andrew Hennessee (Notre Dame)


Anna Arnett (Notre Dame)


Michelle Campbell (Northwestern)

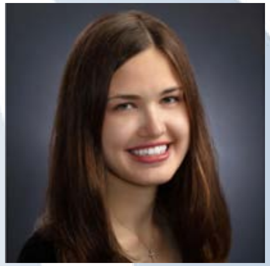

Tomas Kraay (Cornell)


Molly Sullivan (Notre Dame)


Benjamin Bailey (Boise)


Kathryn Zhang (Cornell)


Finley Donachie (RPI)


Rena Steele (Notre Dame)


Zach Erling (Notre Dame)


Icelene Leong (Boise)


Husayn Mukadam (RPI)


Sophia Chou (Notre Dame)


Michael Bhopaul (MIT)


Emma Sponga (RPI)


Sivagya KC (Boise)


Luis Martinez (MIT)


Ambrose Yang (Cornell)

Sponsor interactions outside Liaison Meetings (tallied till Dec 2023)

Lowlights in Year 1 & improvements in Year 2

1. **Growth of Center during year 1**
   1. Slow process of completing subawards (last finalized October 2023)
   2. Need to help improve PI's KPI, especially for those who are new to SRC - improvements are expected in Year 2 thanks to Adam Knapp to present on KPI in 2024Q1!
2. **Varying efficiency of Liaison Meetings**
   1. Improve schedule to achieve larger Liaison attendance – potentially consider a fixed time over 2 alternating times
   2. Encourage student attendance
   3. Continue combination of deep dive presentations and short updates
   4. Move beyond thrust boundaries with focus on topical areas
3. **Leveraging resources**
   1. PIs attempted to access the HPC systems via the DOD high-performance computing modernization program (HPCMP), but clearance seems to be a bottleneck
4. **Meaningful connections with other JUMP 2.0 center to improve benchmarking & understand impacts**
   1. Need to be driven by PIs' genuine research needs – Seed funds help spur interests and converge topics
   2. PIs need to have bandwidth – incentive helps

Soliciting help from the SAB!

1. Seed funds to be evaluated by mid-May 2024

SUPREME – PRISM
SUPREME – CHIMES
SUPREME – CUBiC
SUPREME - CoCoSys

2. Our **NSF REU proposal** was strong but NSF said "insufficient funds at NSF" ….

Year 2 - Top Plans

4 **Materials Discovery & Processing:** *Taming new materials and new physics.*

Accelerated Materials Discovery | **AI-assisted Synthesis & Manufacturing** | **Processing & Metrology**

1. Implement and improve fail-fast approaches
2. Identify target demonstrations to focus center achievements (seed $ with system centers)
3. Understand system-level impacts

$MoSe_2$,

Conven

Si,

Anisotr

~~PtO~~,

$PdCrO_2$, $Bi_2Ir_2O_7$, and IrO_2

ReB_3

K-doped SnO, $SrPd_3O_4$, a-PdO

PdO, ~~Ba_2PbWO_6~~ (not BEOL)

tals

als

2D magnetic &
topological insulator
(demo only – low T):
~~Cr_2Ge_2~~Te_6 and BiSbTeSe$_2$

Dielectrics
SiO_2, SiN_x, SiCO, HfO_2, $HfZrO_2$.
$BaHf_{0.6}Ti_{0.4}O_3$ (BHTO) (k~150)

Topological interconnect
GaPt, CoSn, NbAs, ~~$CeCoIn_5$?~~ (oxidation)

Molecules
$Ru(pap)_3(PF_6)_2$, $Ru(bpy)_3(PF_6)_2$

Proton channel:
Nb_2O_5, ~~Ta_2O_5~~ (low proton conductivity)

N-channel oxides
In_2O_3 with W, Mg, Sn, Ga, Ti

Optical interconnect
III-Vs on Si, graphene

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Defining feature of SUPREME

4 Materials Discovery & Processing: *Taming new materials and new physics.*

Accelerated Materials Discovery AI-assisted Synthesis & Manufacturing Processing & Metrology

TMDs
$MoSe_2$, WS_2, WSe_2
MoS_2, MoSeS

2D Materials
AlN, ZnO, SnSe
h-Bi, ~~GeSe, GeS~~ (low h mobility), SnTe

Conventional semiconductors
Si, SiGe, Ge, GaN, SiC

Processing Materials
Organics, ASD Resist

Materials for Ohmic Contacts

Nitrides
GaN, AlScN, GaScN, BN, InGaN, AlN, AlBN, TiN, AlLaN, AlYN

n-channel oxides
In_2O_3 with W, Mg, Sn, Ga, Ti, Zn, Ta, Ga_2O_3

p-channel oxides
~~Ta_2SnO_6, $BaBiTaO_6$~~
K-doped SnO, $SrPd_3O_4$, a-PdO, PdO, ~~Ba_2PbWO_6~~ (not BEOL by MBE)

Thermal materials
BN, AlN, diamond

Ferroelectrics
SnSe, AlScN, HZO, $BaTiO_3$, $SrCaCo_2O_5$, $LaA_2Fe_3O_8$ (ordered O vacancy), Ln_4Pn_2O

Dielectrics
Al_2O_3, SiO_2, SiN_x, SiCO, HfO_2, $HfZrO_2$, BN, $BaHf_{0.6}Ti_{0.4}O_3$ (BHTO) (k~150), SiC, AlN, hr-Si

Anisotropic spin sources
PtO, ~~$Sr_3Ru_2O_7$~~ (not yet grown)
$PdCrO_2$, ~~$Bi_2Ir_2O_7$, and IrO_2~~ (low efficiency), $SrRuO_3$

Synthetic antiferromagnets
FeCoB/Pt/Ru/Pt/FeCoB

Proton electrolyte in electrochemical RAM (ECRAM) – npr HfO_2, npr ZrO_2

ECRAM channel
MoO_3, WO_3, V_2O_5 , Nb_2O_5, ~~Ta_2O_5~~, IGZO

Proton reservoir in ECRAM
Metal hydrides, PdH_x

Molecules
$Ru(pap)_3(PF_6)_2$, $Ru(bpy)_3(PF_6)_2$

2D magnetic & topological insulator (demo only – low T)
$Cr_2Ge_2Te_6$ and $BiSbTeSe_2$

Weyl semi-metals, Heusler alloys – Co_2MnGa, Mn_3Sn, Mn_3Ir

Oxide interconnect metals
$PdCoO_2$, $PdRhO_2$, $PtCoO_2$

Intermetallic interconnect metals
VPt_2, $MoNi_2$, $NiIr_3$, CoPt

Conductive boride-based interconnect metals
YCo_3B_2, NbFeB, Mn_2B, ~~ReB_2~~

Topological interconnect
GaPt, CoSn, NbAs, ~~$CeCoIn_5$~~ (oxidation), ~~FeSn~~, $CoIn_3$, ~~$CoIn_2$, NiTe, $RhIn_3$~~ (high R in NWs)

Optical interconnect
III-Vs on Si, graphene, TMDs, Nitrides, BTO, SnSe

Materials in the proposal; Materials added/~~tabled~~ in Year 1; Materials added/~~tabled~~ in Year 2

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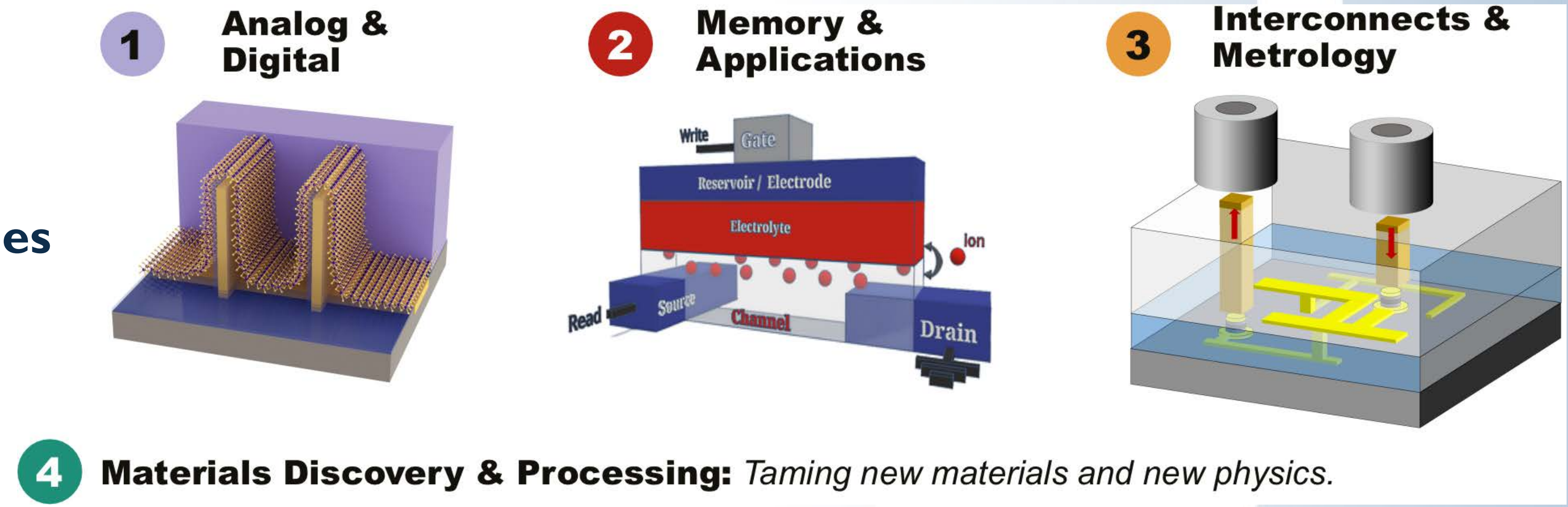
Topics in SUPREME

1. 2D materials & devices
2. Nitride materials & devices
3. Oxide materials & devices
4. Ferroelectric memories & benchmarking
5. Spintronic materials & devices
6. Ionic materials & devices
7. Electrical interconnects
8. Optical interconnects
9. Metrology
10. High-throughput materials discovery
11. Advanced processing
12. High-k dielectrics & ferroelectrics



Topics in SUPREME (highlighted today)

1. **2D materials & devices**
2. Nitride materials & devices
3. **Oxide materials & devices**
4. Ferroelectric memories & benchmarking
5. Spintronic materials & devices
6. Ionic materials & devices
7. Electrical interconnects
8. Optical interconnects
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10. **High-throughput materials discovery**
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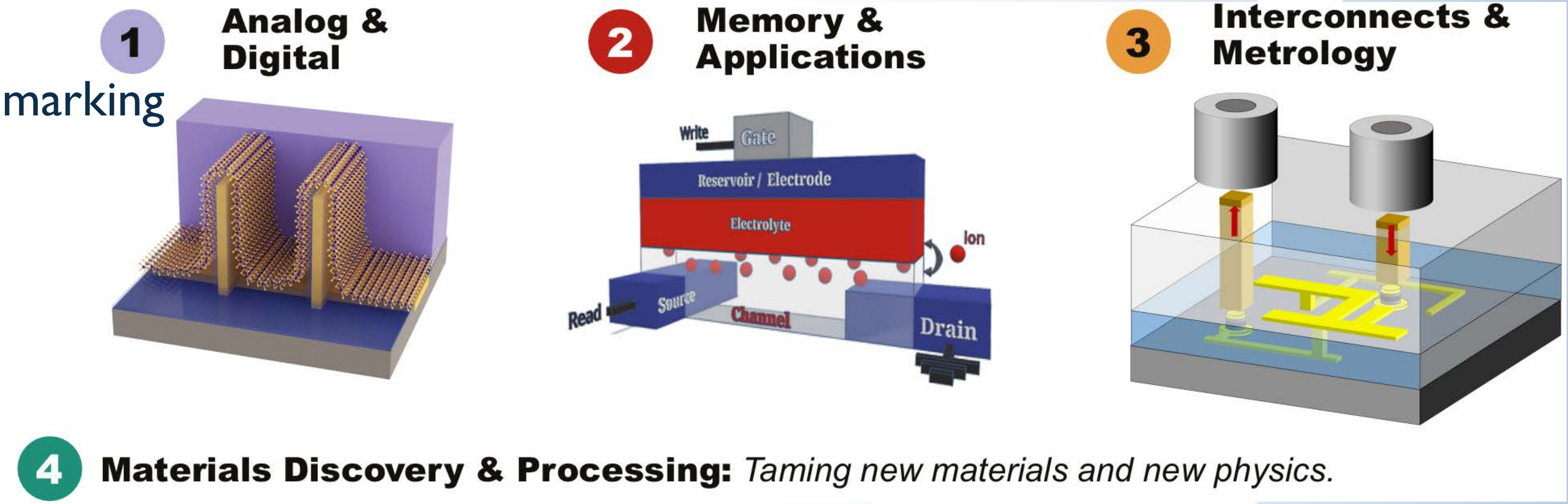
① **Analog & Digital**

② **Memory & Applications**

③ **Interconnects & Metrology**

④ **Materials Discovery & Processing:** *Taming new materials and new physics.*

Topic: 2D materials & devices for high-density logic and memory

1. **PIs:** Feliciano Giustino, Jing Kong, Tomas Palacios, Eric Pop, Farhan Rana, Elton Graugnard, Steve George
2. **Tasks**: **3137.001, 3137.028, 3137.029, 3137.030, 3137.031, 3137.043**
3. **Application:** High-density logic and memory
4. **Objectives:**
    a. To identify and realize 2D materials with high carrier mobility
    b. To develop synthesis strategies to obtain high quality 2D materials at BEOL compatible temperatures
    c. To demonstrate multi-channel 2D-nFET outperforming silicon at 1 nm node and beyond
    d. To improve 2D-pFET doping, lower defects, compare 1L vs. 2L, target $I_D > 750$ µA/µm, $R_C < 200$ Ω·µm
5. **SOTA:**
    a. Mobilities of TMDs are < 50-100 cm^2/Vs at RT
    b. Bi ohmic contacts to MoS_2 with low contact resistance (123 Ω·µm) and high current density (1135 µA/µm)
    c. 8” wafer-scale low-temperature (<300 °C) by MOCVD
    d. Gate-all-around transistor based on MoS_2 nano-ribbon (TSMC 2022)
    e. 2D-pFETs are far behind 2D-nFETs
6. **Approaches with feedback loops:**
    a. High-throughput search for high-mobility candidates using the *ab initio* Boltzmann transport equation
    b. ML-advised automation of 2D materials synthesis & characterization
    c. Improve p-type channel material quality
    d. Processing one atomic layer at a time: atomic layer etch of 2D materials
    e. 8” large-wafer highly-scaled devices (< 8 nm), self-aligned source/drain with multi-channels formed with one etching step

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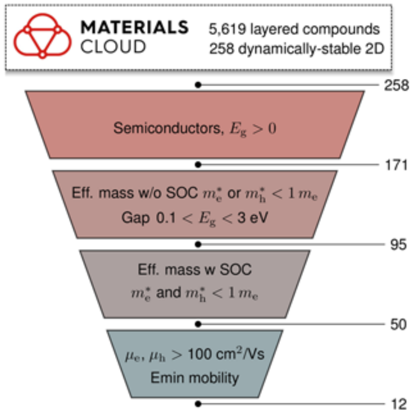
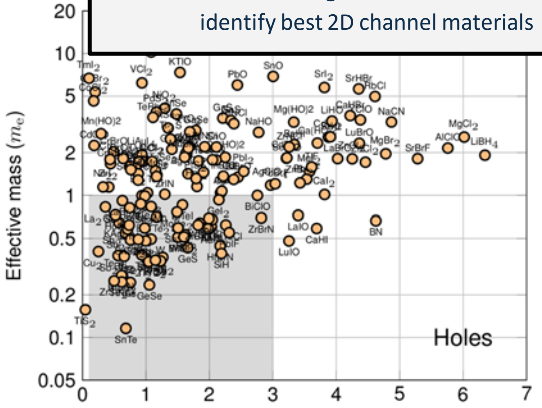
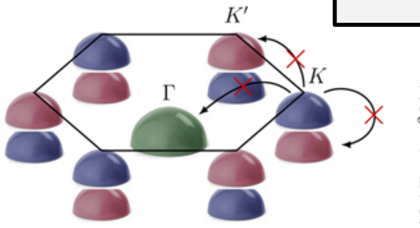
Topic (achievements): 2D materials & devices for high-density logic and memory

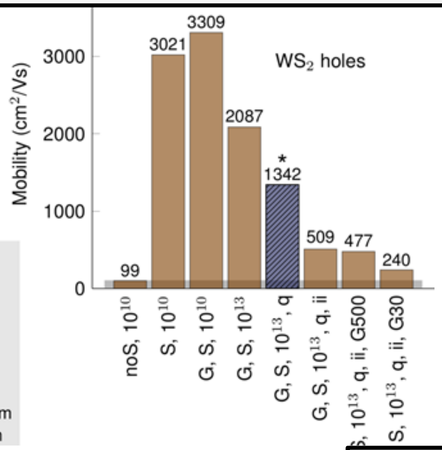


HT *ab initio* screening of 2D materials database to identify best 2D channel materials

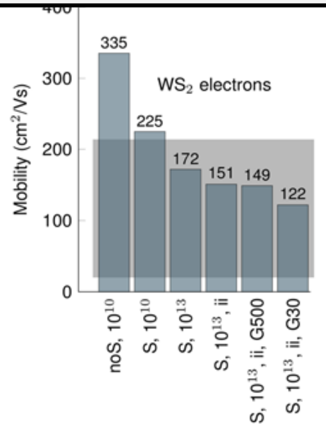


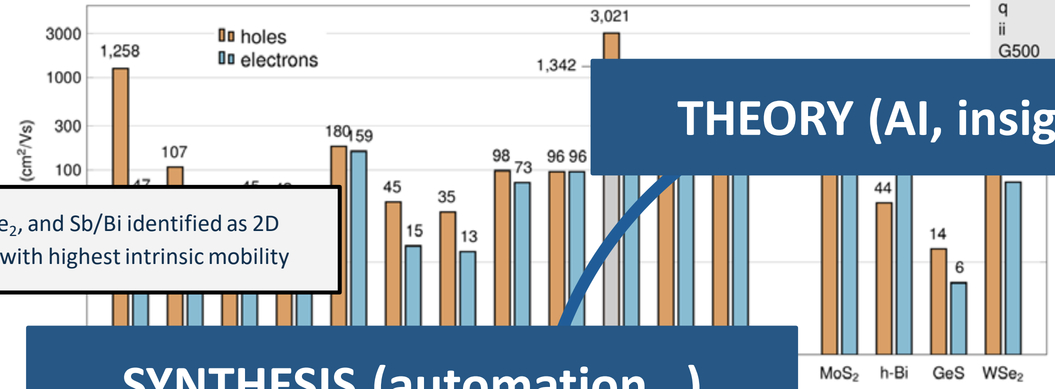
WS$_2$ shows exceptional promise due to spin-orbit coupling-forbidden intervalley scattering. Cause for low p-type experimental mobility likely defects and contacts (**Giustino**)





noS	no SOC
S	with SOC
10^{10}	carrier conc. in cm^{-2}
10^{13}	carrier conc. in cm^{-2}
G	with GW bands
q	with quadrupole correction
ii	with ionized-impurity scatt.
G500	with grain-boundary scatt., grain size 500 nm
	grain size 30 nm

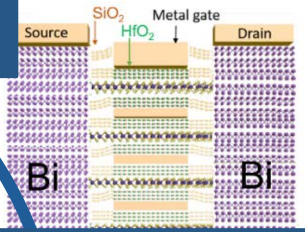


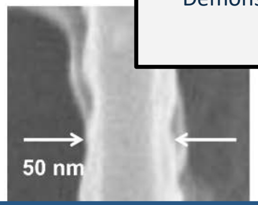


WS$_2$, WSe$_2$, and Sb/Bi identified as 2D materials with highest intrinsic mobility

THEORY (AI, insights…)

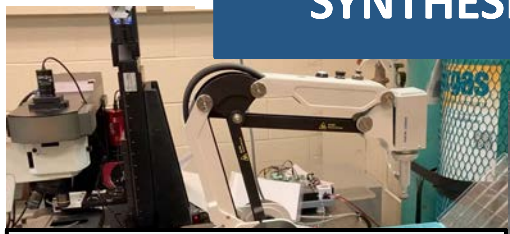
Demonstration of full fabrication of multichannel MoS$_2$ transistor on 8" process (**Palacios**)



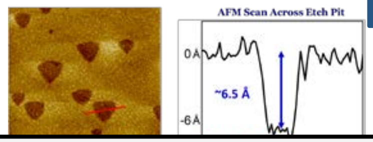


SYNTHESIS (automation…)

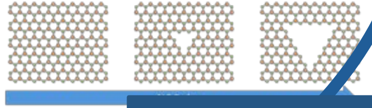
DEVICES (sub-10 nm, 8" wafers …)

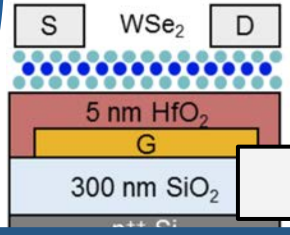


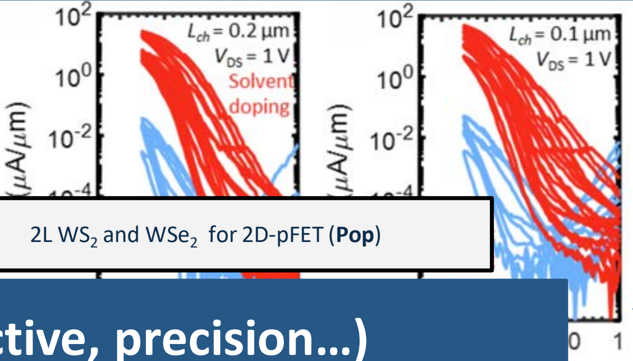
Autonomous synthesis setup ready for large-area 2D materials growth (**Kong**)



Atomic layer etch of MoS$_2$ (**George**)







2L WS$_2$ and WSe$_2$ for 2D-pFET (**Pop**)

METROLOGY (high throughput…)

PROCESSING (selective, precision…)

Topics in SUPREME **(highlighted today)**

1. **2D materials & devices**
2. Nitride materials & devices
3. **Oxide materials & devices**
4. Ferroelectric memories & benchmarking
5. Spintronic materials & devices
6. Ionic materials & devices
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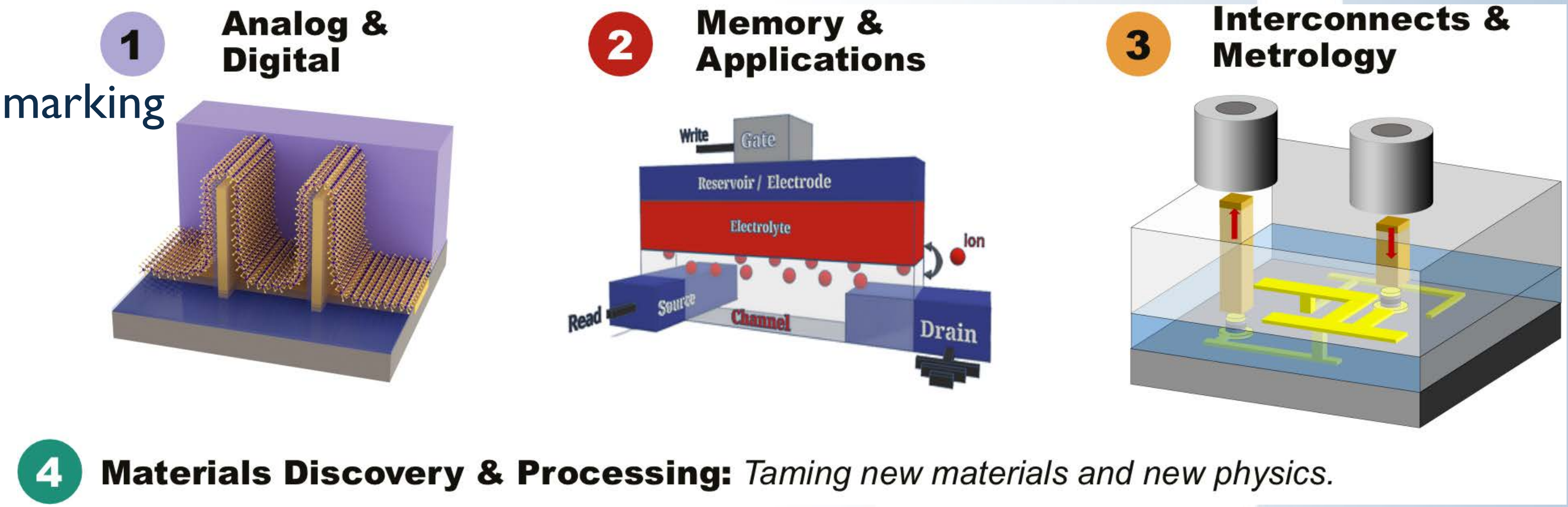


Topic: High-Throughput Materials Discovery

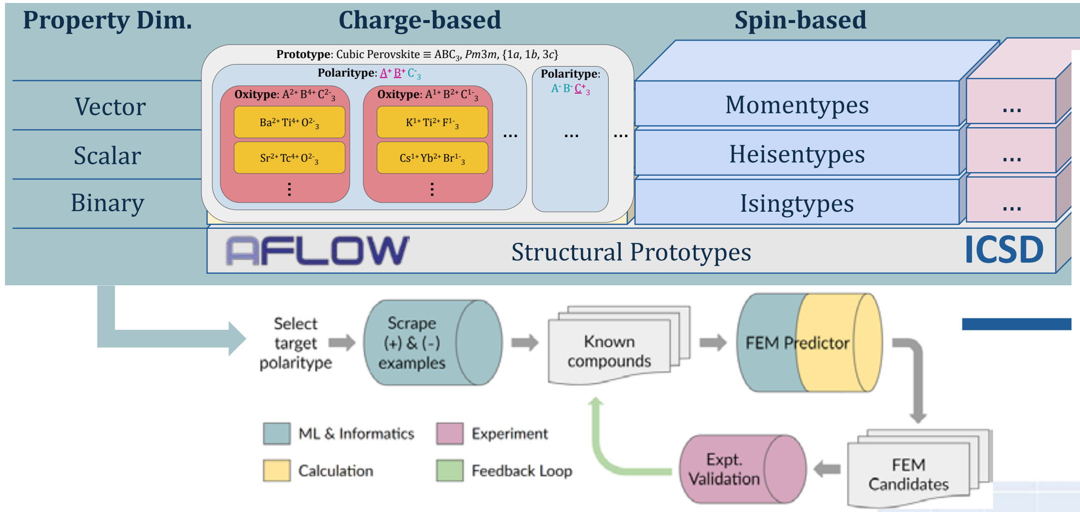
1. **PIs:** Christopher Hinkle, Jing Kong, James Rondinelli, Judy Cha, Farhan Rana
2. **Tasks**: **3137.020, 3137.025, 3137.030, 3137.037, 3137.038, 3137.046**
3. **Application:** Develop new synthesis, characterization, and predictive methods to accelerate materials discovery
4. **Objectives:**
   a. To identify new materials for interconnects, oxide semiconductors, and ferroelectrics
   b. To develop deep learning methods for accelerated materials characterization
   c. To develop new synthesis routes and automated synthesis
   d. To demonstrate superior electronic materials on an accelerated timeline
5. **SOTA:**
   a. Linear trial and error, expert intuition, and grid search experiment design
   b. 10 years to optimize new electronic materials

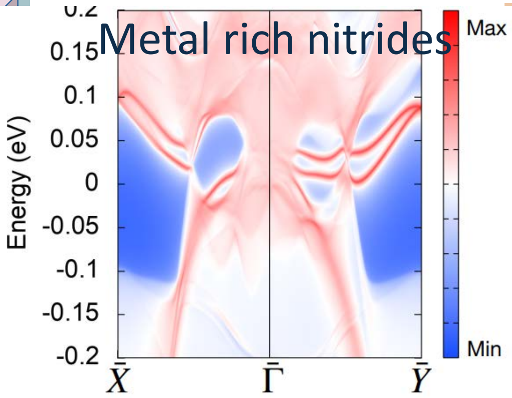
6. Approaches with feedback loops:
   a. First-principles computational search and design of new materials (Rondinelli)
   b. High-throughput thin film materials synthesis (Hinkle)
   c. Deep learning-aided materials characterization (diffraction, XPS, microwave reflectometry) (Hinkle)
   d. Automated 2D material synthesis with AI guided characterization and experiment design (Kong)
   e. Direct high-throughput wire synthesis through nanomolding (Cha)
   f. High-throughput defect spectroscopy using THz (Rana)

Topic (achievements): High-Throughput Materials Discovery

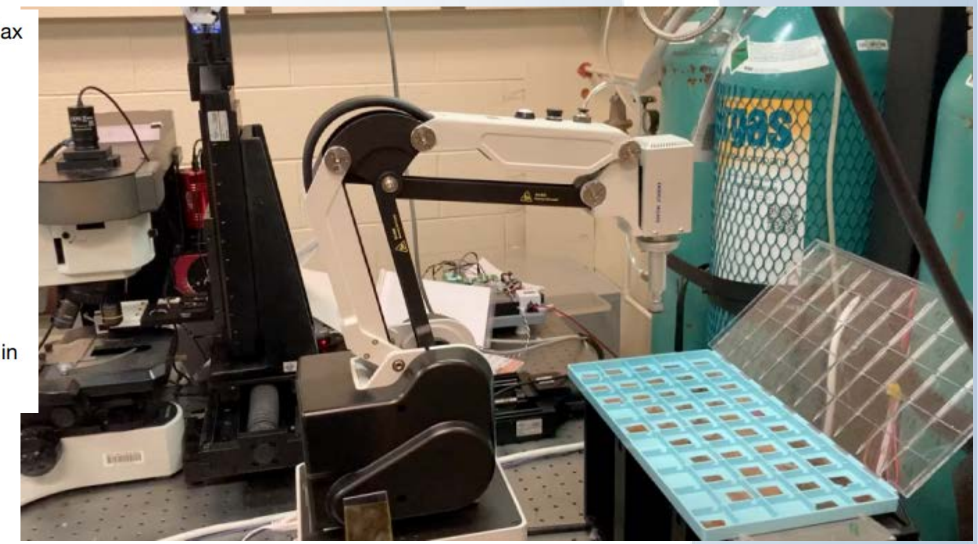
Machine Learning Aided Material Discovery

High-throughput ML+DFT workflow to predict new materials (Rondinelli)

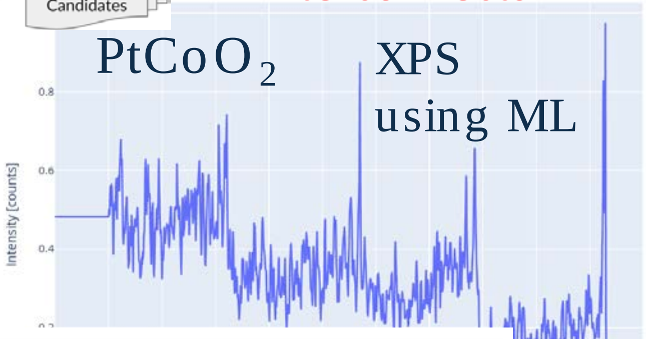




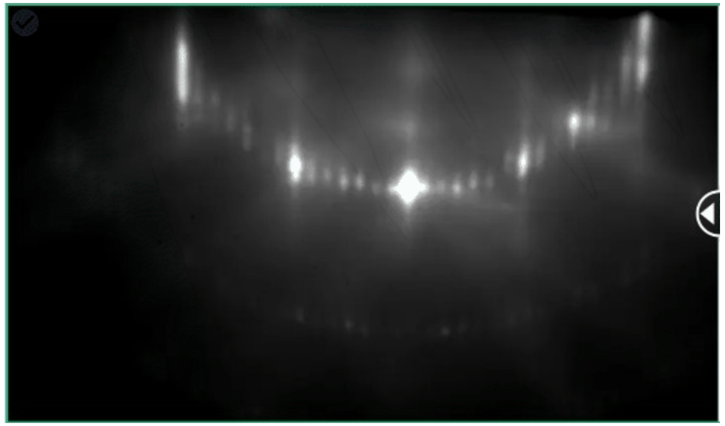
Autonomous CVD process with Robot arm (Kong)

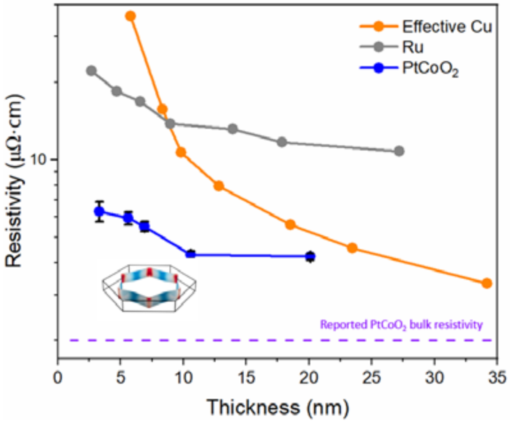


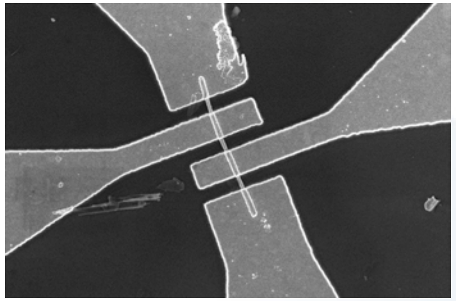
Interconnects



Diffraction Fingerprint Extraction (Hinkle)

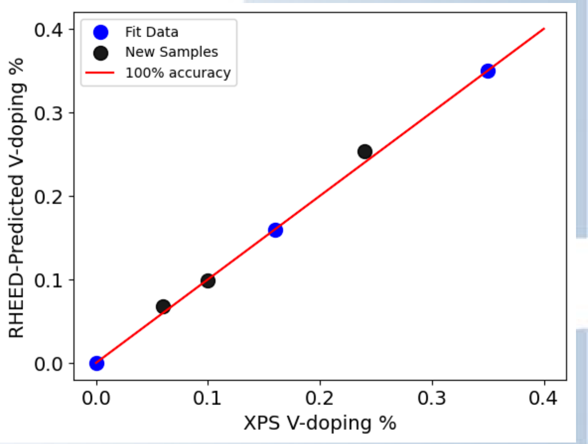






Nanomolding for interconnects (Cha)

Finding correlations in in-situ and ex-situ data from ML



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SUPeRior Energy-efficient Materials and dEvices

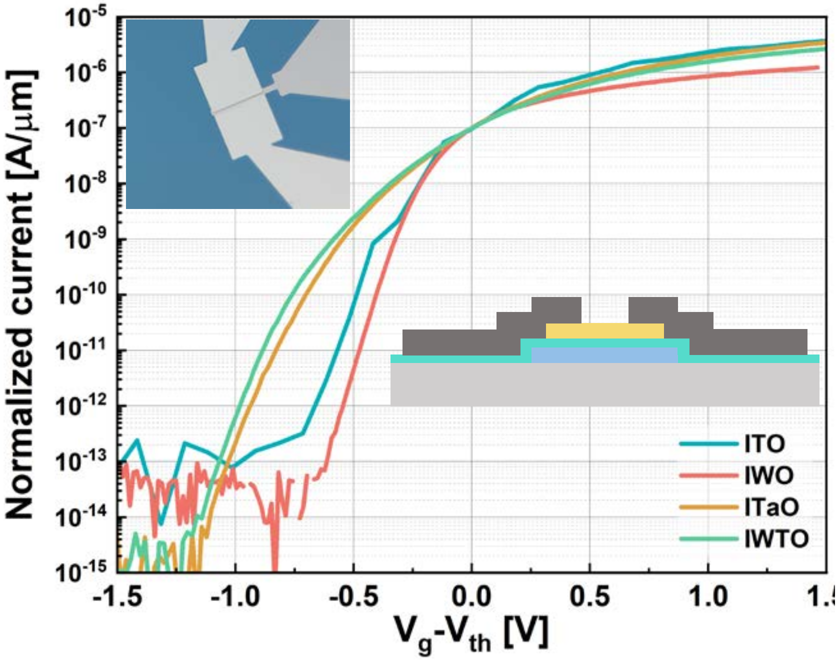
Topic: Oxide materials & devices for high-density logic and memory

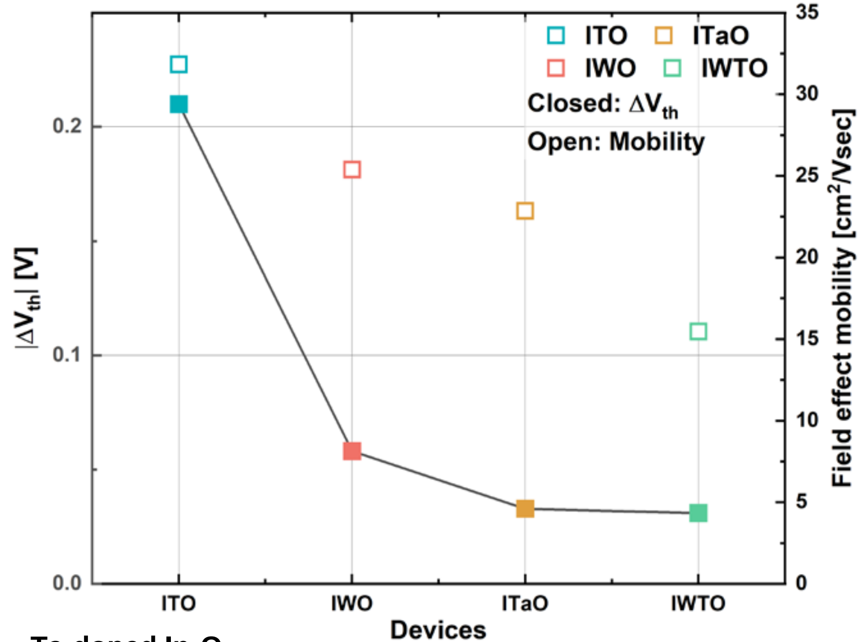
1. **PIs:** Christopher Hinkle, Kai Ni, Asif Khan, Darrell Schlom, Grace Xing
2. **Tasks**: **3137.011, 3137.013, 3137.037, 3137.033**
3. **Application:** Develop n-type and p-type oxide semiconductors with mobility >30 cm^2/V-s with better reliability
4. **Objectives:**
   1. Fabricate In_2O_3-based amorphous oxide semiconductors with various dopant/alloy species for n-channel
   2. MBE of K-doped SnO and PdO for p-channel
   3. Optimize processing conditions for each composition
   4. Compare performance vs. stability for different compositions
   5. Downselect most promising materials for further optimization/improvement
5. **SOTA:**
   1. IWO and In_2O_3 bilayer films with mobility >30 cm^2/V-s, but greater than 0.2 eV ΔV_{th} under bias stress
   2. SnO and CuO with mobility <10 cm^2/V-s

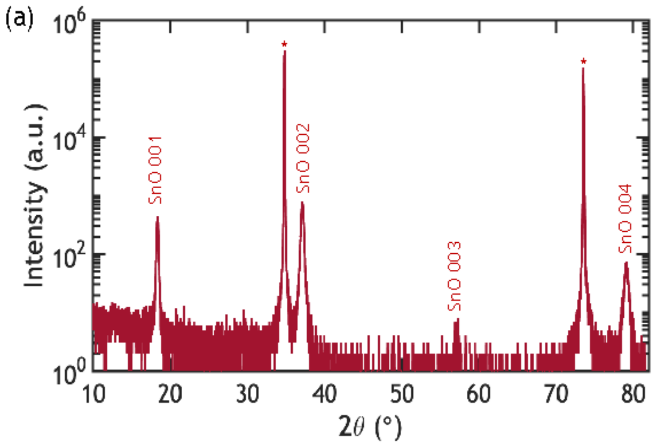
6. **Approaches with feedback loops:**
   1. High-throughput thin film materials synthesis including processing spread (Hinkle)
   2. MBE of K-doped SnO and PdO with Hall measurements (Schlom)
   3. Device fabrication on promising films to assess carrier density and mobility (Hinkle, Ni, Khan)
   4. BTS measurements and stability assessment (Hinkle, Ni, Khan)
   5. SMM measurements for contactless mobility measurements (Hinkle)

Topic (achievements): Oxide materials & devices for logic and memory

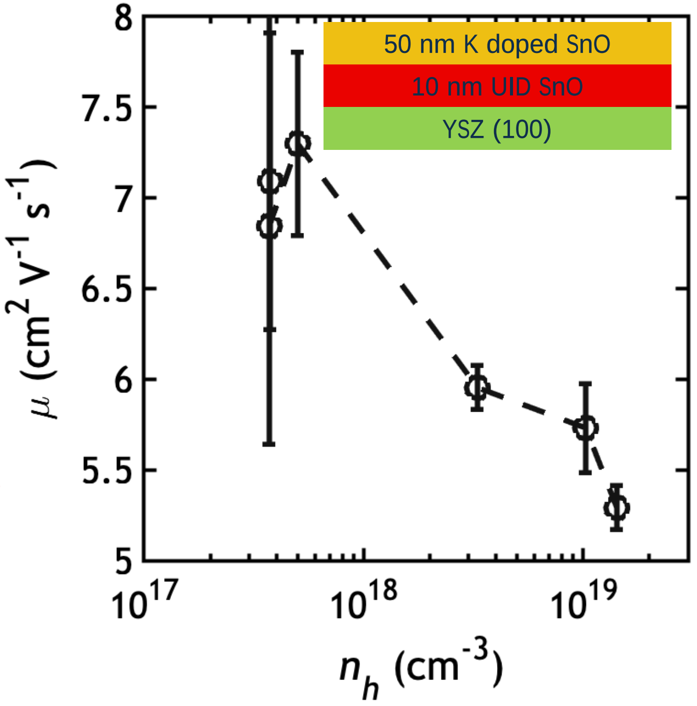
n-type and p-type oxide semiconductors





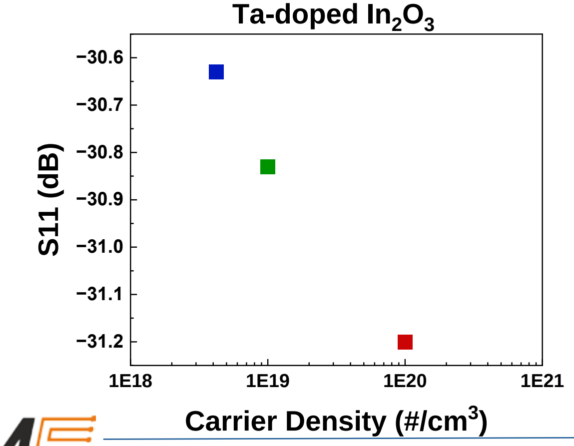


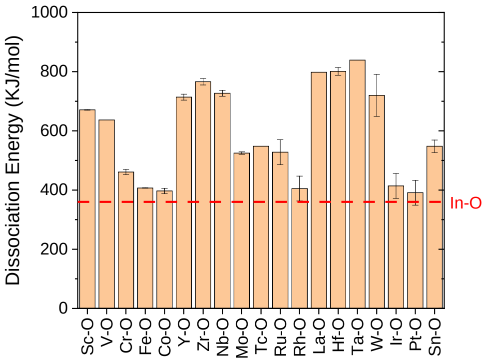
Hole mobility in K-doped SnO up to 7.5 cm^2/V-s



W-, Ta-, and Sn-doped In_2O_3, plus co-doped films (e.g., IWTO)

Improved V_{th} stability under bias stress





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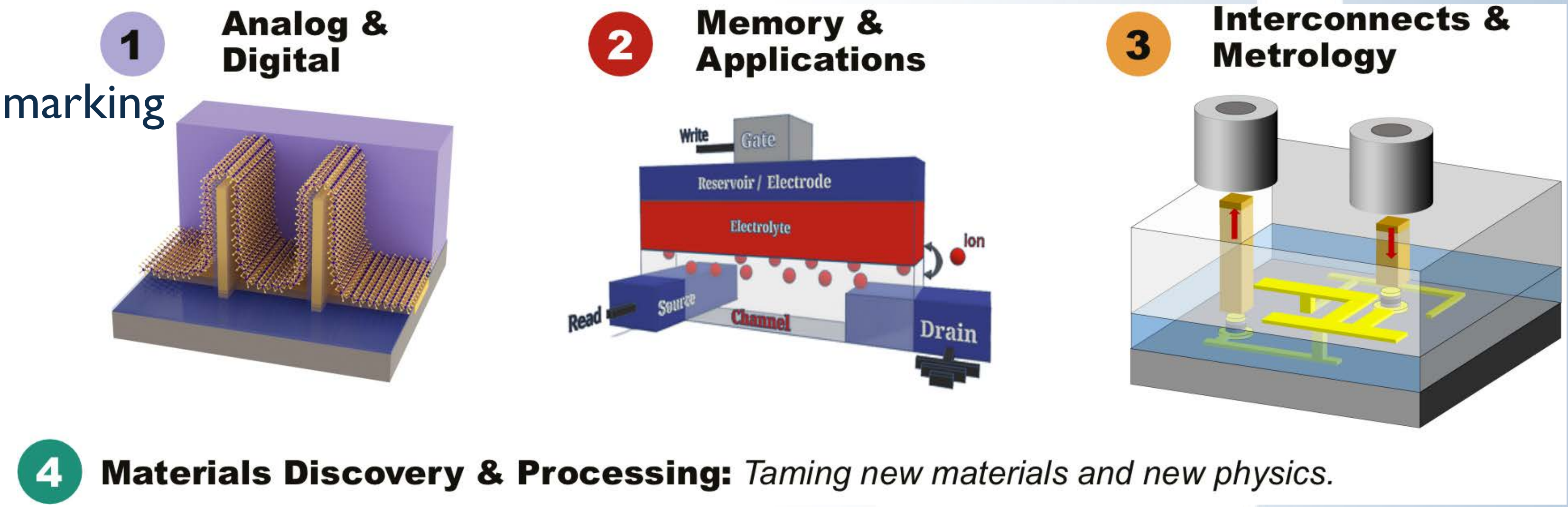
Topics in SUPREME (highlighted today)

1. **2D materials & devices**
2. Nitride materials & devices
3. **Oxide materials & devices**
4. Ferroelectric memories & benchmarking
5. Spintronic materials & devices
6. Ionic materials & devices
7. Electrical interconnects
8. Optical interconnects
9. Metrology
10. **High-throughput materials discovery**
11. **Advanced processing**
12. High-k dielectrics & ferroelectrics



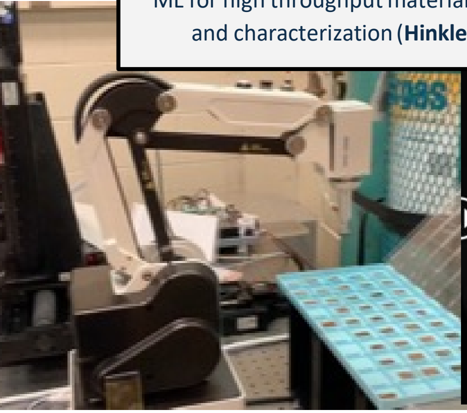
Materials Discovery & Processing: *Taming new materials and new physics.*

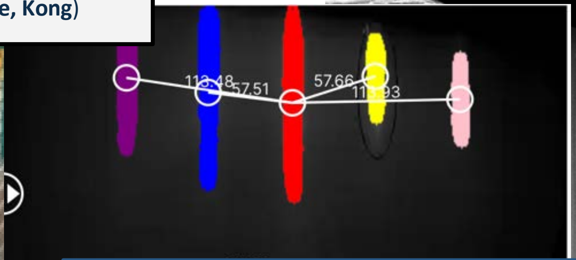
Topic: Advanced Processing for logic and memory device materials

1. **PIs:** Jing Kong, Elton Graugnard, Steve George, Greg Parsons, Judy Cha, Asif Khan, Chris Hinkle, Andy Kummel (CHIMES)
2. **Tasks**: **3137.011, 3137.020, 3137.038, 3137.041, 3137.029, 3137.030, 3137.031, 3137.039, 3137.040, 3137.042, (CHIMES: 3136.020, 3136.022)**
3. **Application:** Integration of materials into logic and memory devices against manufacturing constraints
4. **Objectives:**
    a. To develop synthesis strategies to obtain high quality 2D materials at BEOL compatible temperatures with thickness/layer control
    b. To enable ALD of ferroelectric materials beyond HZO and ultrahigh-k dielectrics
    c. To establish automated and high-throughput materials synthesis and characterization to accelerate processing for improved properties across materials classes (interconnects, dielectrics, 2D materials, etc.)
    d. To enable advanced integration strategies through area-selective deposition and etching
5. **SOTA:**
    a. 200 mm wafer-scale TMDs with low-temperature (<300 °C) by MOCVD and RT mobilities of TMDs are < 50-100 cm^2/Vs (SUPREME)
    b. 300 mm MoS_2 <300 °C by ALD with nanoscale grain size and mobility < 1 cm^2/Vs (industry R&D)
    c. Automated processing now applied to films and structural property correlation (SUPREME)
    d. Layer-by-layer etching of 2D materials demonstrated (SUPREME)
    e. Inherent area-selective processing without small molecules on chemically distinct surfaces (SUPREME)
    f. Ferroelectric films by PVD, limited ferroelectric oxides by ALD
6. **Approaches with feedback loops:**
    a. MOCVD of 2D materials with atomic layer etching for thickness control (Kong/George)
    b. ML-advised automation of 2D materials, novel interconnects and topological materials synthesis & characterization (Hinkle/Kong/Cha)
    c. Area-selective deposition on chemically-similar surfaces and for 2D materials by ALD (Parsons/Graugnard)
    d. Ferroelectric/dielectric ALD process development with atomic layer annealing (ALA) (Graugnard/Khan/Kummel)
    e. Proton transport solid state electrolytes and 2D channel materials for ECRAM (Bilge/Kong/Graugnard)

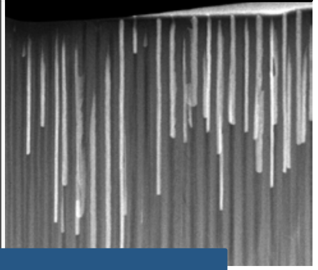
Topic (achievements): Advanced Processing

ML for high throughput materials synthesis and characterization (**Hinkle, Kong**)



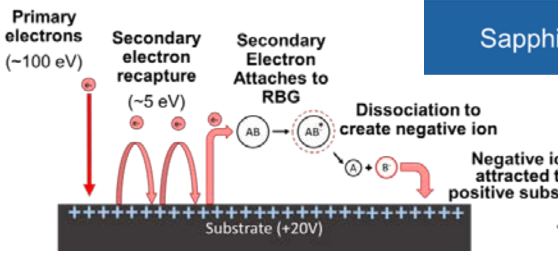


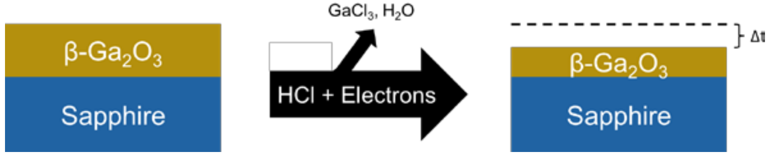
Molded nanowires (**Cha**)



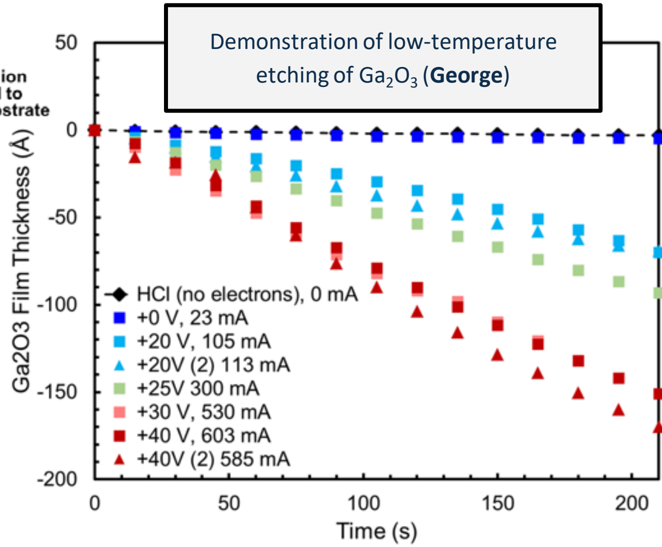
HIGH THROUGHPUT (ML/AI discovery, synthesis, properties…)

Novel electron-enhanced atomic layer etching and chemical vapor etching of 2D materials and wide band gap oxides (**George**)



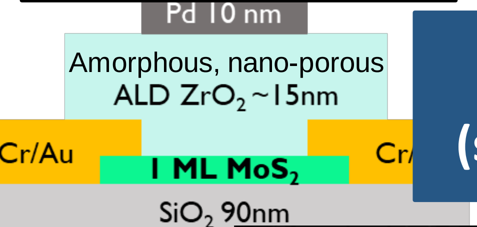


Demonstration of low-temperature etching of Ga_2O_3 (**George**)



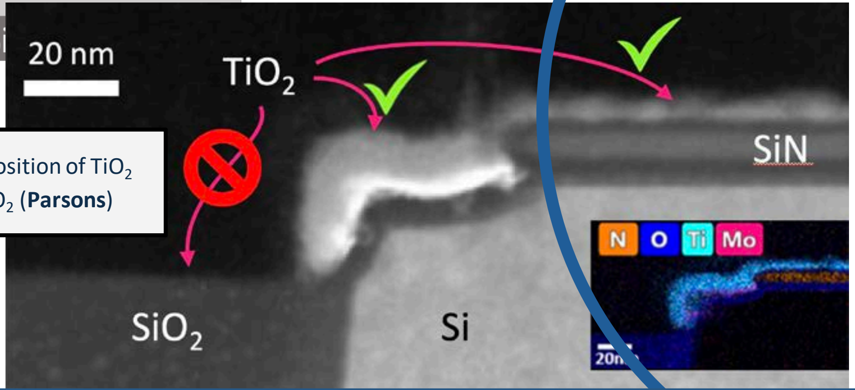
NOVEL PROCESSES (EE-ALE, EE-CVE…)

2D materials and ALD oxides for ECRAM (**Bilge, Kong, Graugnard**)

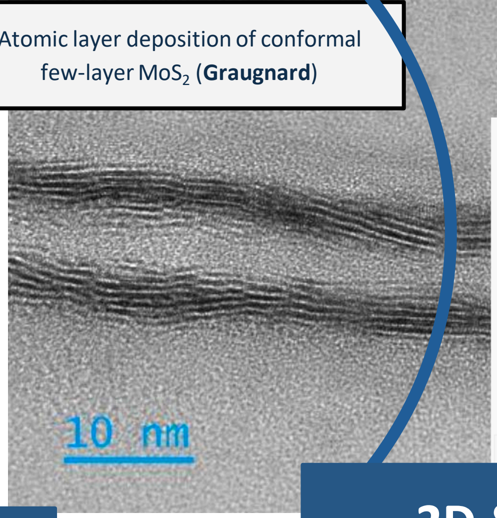


NOVEL MEMORY (scalable processes…)

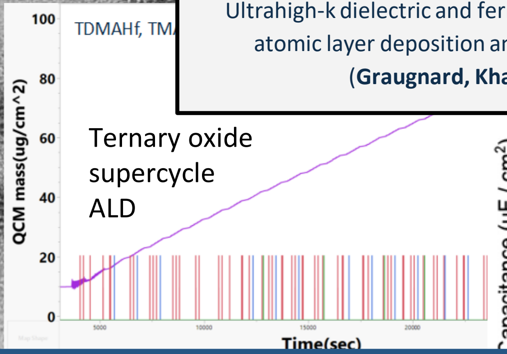
Area-selective deposition of TiO_2 on SiN_x versus SiO_2 (**Parsons**)

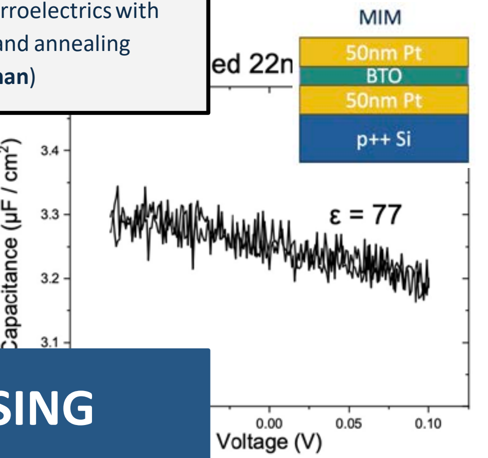


Atomic layer deposition of conformal few-layer MoS_2 (**Graugnard**)



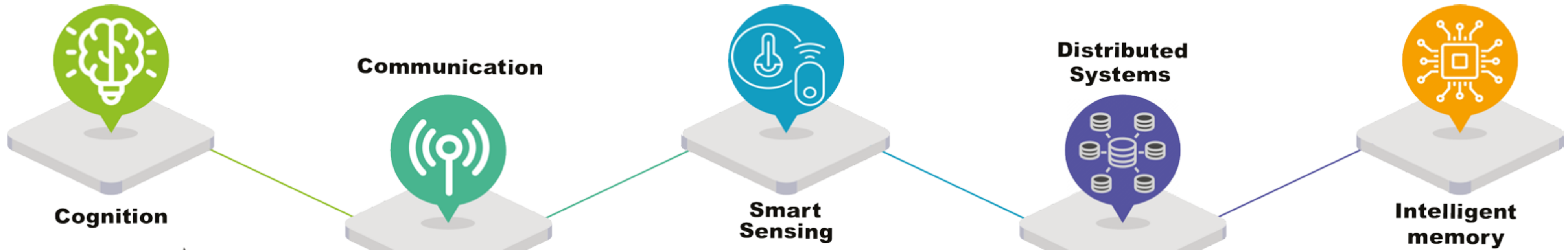
Ultrahigh-k dielectric and ferroelectrics with atomic layer deposition and annealing (**Graugnard, Khan**)





AREA-SELECTIVE PROCESSES (self-aligned…)

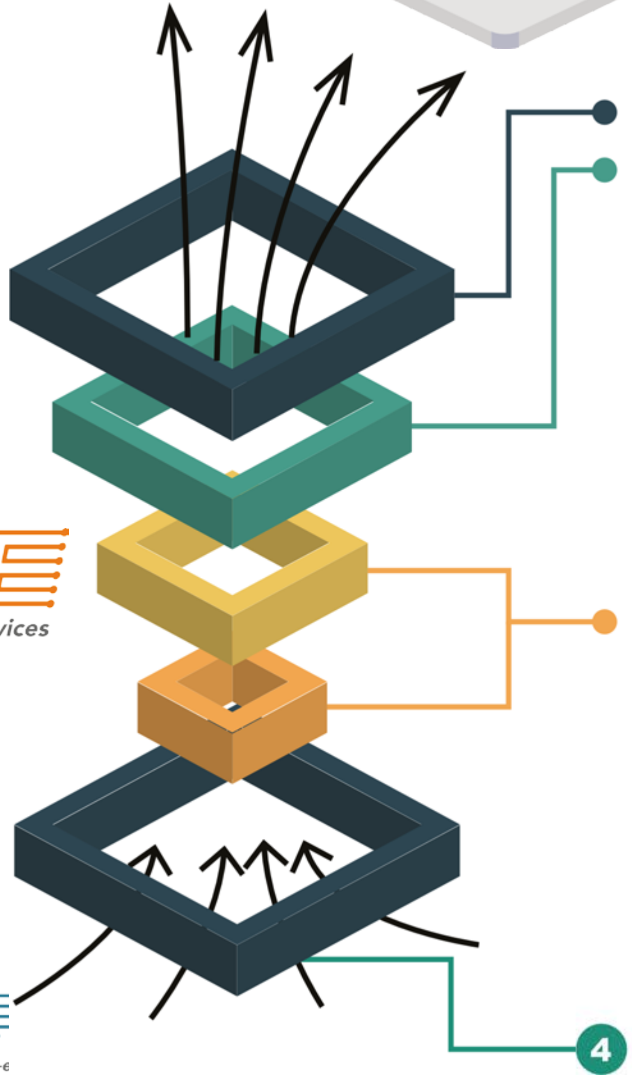
2D & DIELECTRIC PROCESSING (stoichiometry, phase, properties…)



Center Vision

SUPREME

SUPeRior Energy-efficient Materials and dEvices



Seismic Shifts *Bridging the gap and enabling the seismic shifts in ICT.*

Application-level Benchmarking *Meeting the workload demands of the future.*

Machine Learning & Artificial Intelligence
- -Hyperdimensional Computing models
- -Transformer Networks — GPT-3 and beyond
- -Recommendation Systems
- -Perception and Autonomy

Associative Memories
- -Key Value Storage
- -RF Intelligence
- -Bioinformatics

Physics-based Computing

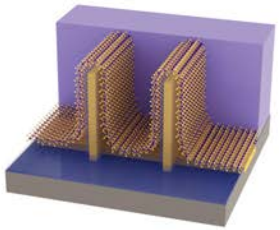
Augmented Memory Hierarchy

Impacts of Interconnects

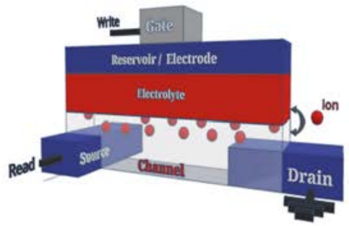
Secure Processing
- -Trusted execution environments
- -Homomorphic encryption

Devices & Interconnects *Accelerating innovations in Analog, Digital, Memory, Storage Devices, & Interconnects*

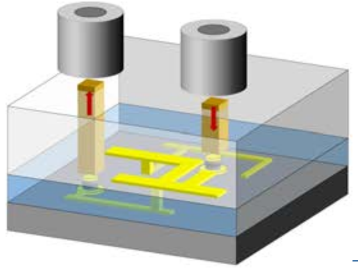
① **Analog & Digital**



② **Memory & Applications**



③ **Interconnects & Metrology**



④ **Materials Discovery & Processing:** *Taming new materials and new physics.*

Semiconductor
Research
Corporation

SUPeRior Energy-efficient Materials and dEvices

Grace Huili Xing (Cornell), Center Director

Tomás Palacios (MIT), Co-Director

Chris Hinkle (ND), co-Lead on High-Throughput

Elton Graugnard (BSU), Thrust Lead on Advanced Processing

Thomas Dienel (Cornell) Managing Director, Jenna LaMendola (Cornell) Administrative Assistant

Cornell University MIT TEXAS Rensselaer CU Yale ND Georgia Tech UCSB Stanford University BOISE STATE UNIVERSITY Northwestern University NC State

SUPREME
SUPeRior Energy-efficient Materials and dEvices

Highlights – Year 1.3

1. Growth of Center during year 1.3

- Students and Postdocs joined: **185**
- Sponsor Liaisons at SUPREME projects: **107**
- **11** FT hires, **15** interns at sponsors

2. Annual Review August 2-3, 2023

- **165** attendees at Cornell University

3. Annual Review June 11-12, 2024

- To be hosted at **MIT, Building 45**
- Planning for **150** on-site participants

4. Liaison Meetings weekly—exception apply

- Rotating through Thrusts/Topics of SUPREME
- Held **36** meetings, presentation materials on Pillar Science (TOC in Notes)
- At alternating times to balance time zones and availability

5. Broadening Participation

- Two BP Champions guide SUPREME's efforts
- Two awards established since 2023Q2/Q3
  - SUPREME Undergraduate Microelectronics Fellows (**7 awarded**)
  - SUPREME Undergraduate Travel Grant (**4 awarded**)
- Total number of undergrads working on SUPREME projects: **24**

2023 August – annual review

Sponsor interactions outside Liaison Meetings (tallied till Dec 2023)

6. **Publications (on Pillar Science)**: 130+

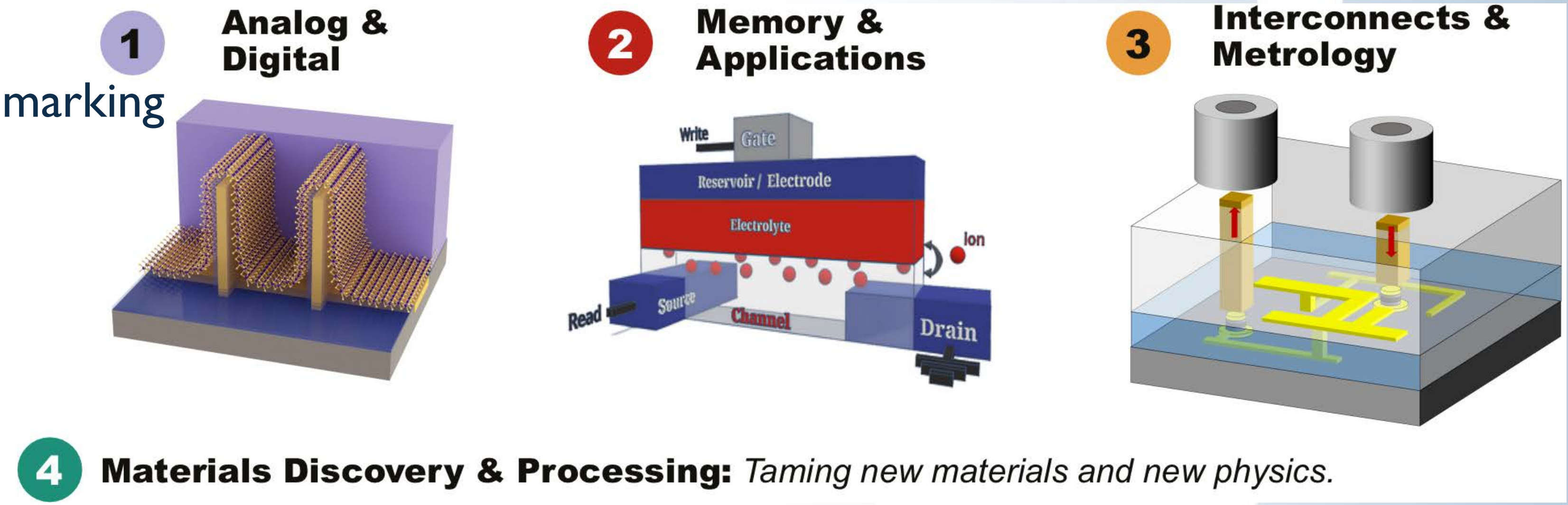
7. **Keynotes**: 70+

8. **Awards**: 25+

Additional slides

Topics in SUPREME

1. 2D materials & devices
2. **Nitride materials & devices**
3. Oxide materials & devices
4. Ferroelectric memories & benchmarking
5. Spintronic materials & devices
6. Ionic materials & devices
7. Electrical interconnects
8. Optical interconnects
9. Metrology
10. High-throughput materials discovery
11. Advanced processing
12. High-k dielectrics & ferroelectrics

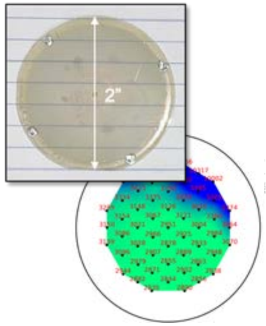


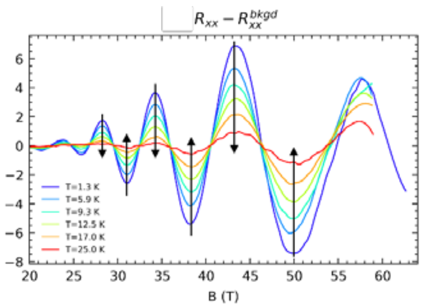
Topic: GaN materials and Devices

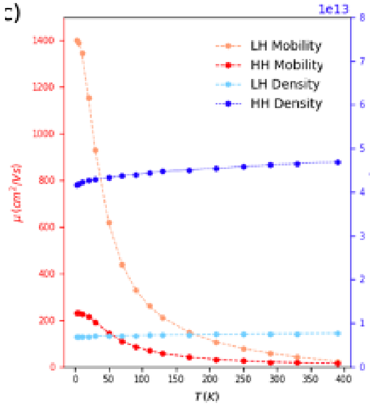
1. **PIs:** Debdeep Jena, Grace Xing, Tomas Palacios, James Hwang, Feliciano Giustino
2. **Tasks**: **3137.03/04/05/06/07**
3. **Application:** Analog, Power and Mixed Signal
4. **Objectives:**
    - a. To develop high-mobility *p*-type GaN channels
    - b. To explore sub-THz high-efficiency materials and devices
    - c. To develop dual-gate and nano-sheet-based GaN transistors to improve V_T control and operating frequency.
    - d. To explore design space for GaN-on-Si HEMTs to have better performance than GaN-on-SiC
5. **SOTA:**
    - a. p-type RT hole mobility 20-30 cm^2/Vs
    - b. Multi-channel Finfet-like GaN transistors have shown record power densities and efficiencies at W-band (link)
    - c. Sub-THz transceivers are large ($>\lambda^2/4$) with high noise (>5dB), insufficient power (~0.1W), and low efficiency (~10%)
6. **Approaches with feedback loops:**
    - a. Rational strain engineering via predictive *ab initio* calculations
    - b. Strain engineering in practical nanofin devices
    - c. AlScN barriers and levering of ferroelectric properties
    - d. Design-Technology-Co-Optimization (DTCO) of GaN transistors, assisted by calibrated device-physics s
    - e. Development of 8” GaN-on-Si process flow
    - f. Silicon substrate removal and wafer bonding for new processing flexibility
    - g. 3D heterogeneous integration of GaN chiplets on SiC interposer

Topic (achievements): GaN materials and Devices

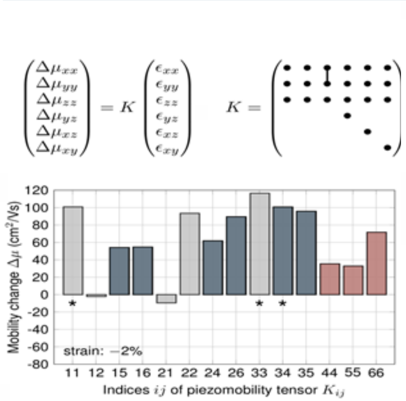
GROWTH (quantum oscillation observed in p-GaN for the 1st time, new III-N's…)

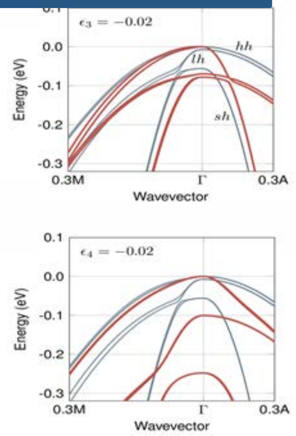




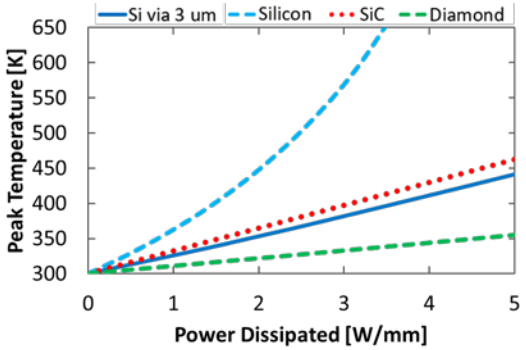


THEORY



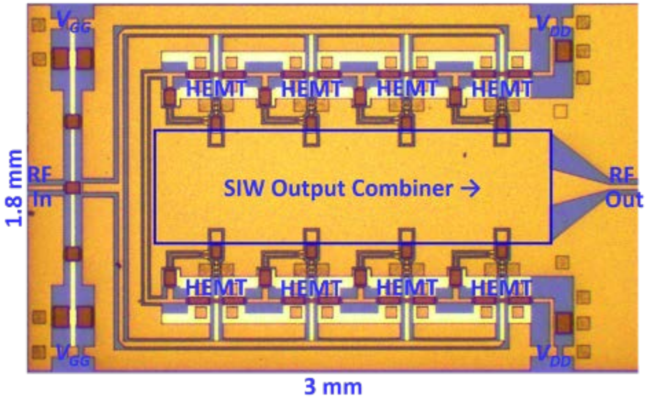


SIMULATIONS AND MODELING

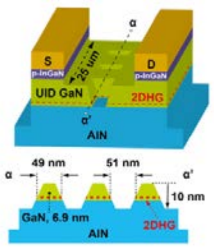


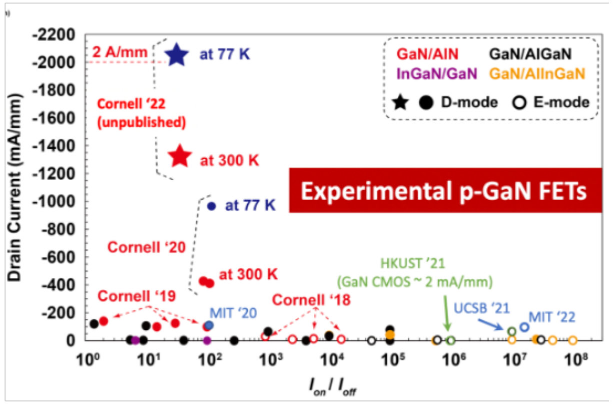
TECHNOLOGY (8", wafer bonding, ALD…)

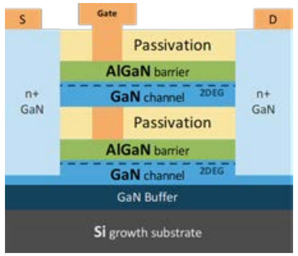
CIRCUITS

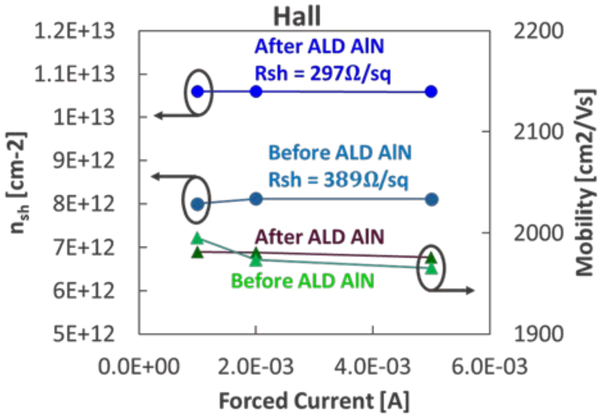


DEVICES (V_T, I_{on}/I_{off} control…)









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SUPeRior Energy-efficient Materials and dEvices

Topics in SUPREME

1. 2D materials & devices
2. Nitride materials & devices
3. Oxide materials & devices
4. **Ferroelectric memories & benchmarking**
5. **Spintronic materials & devices**
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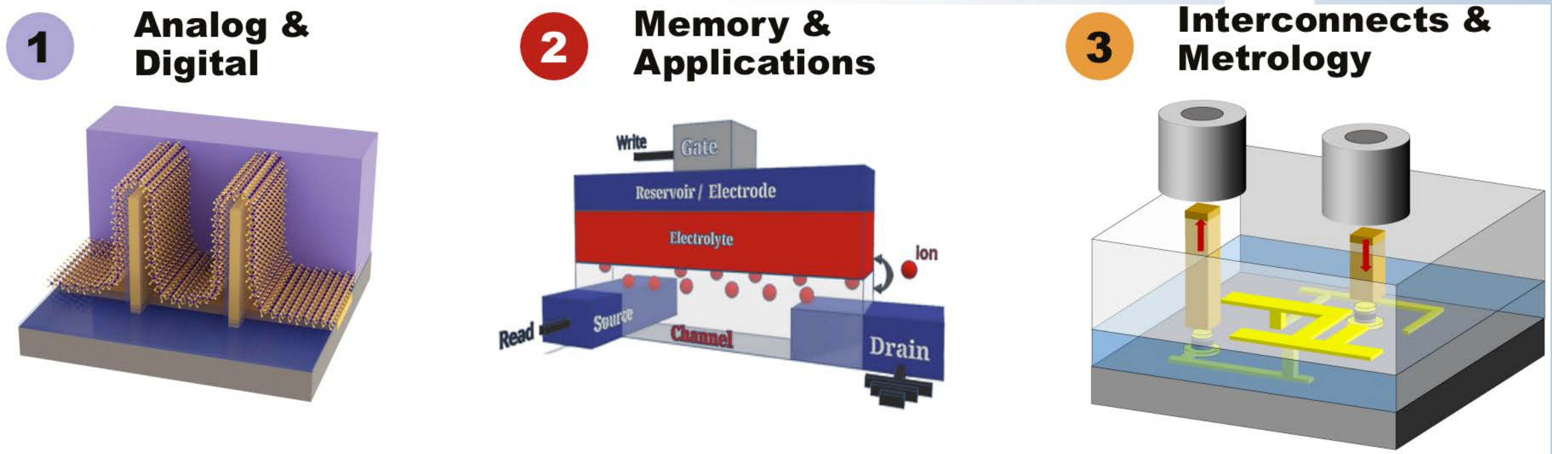


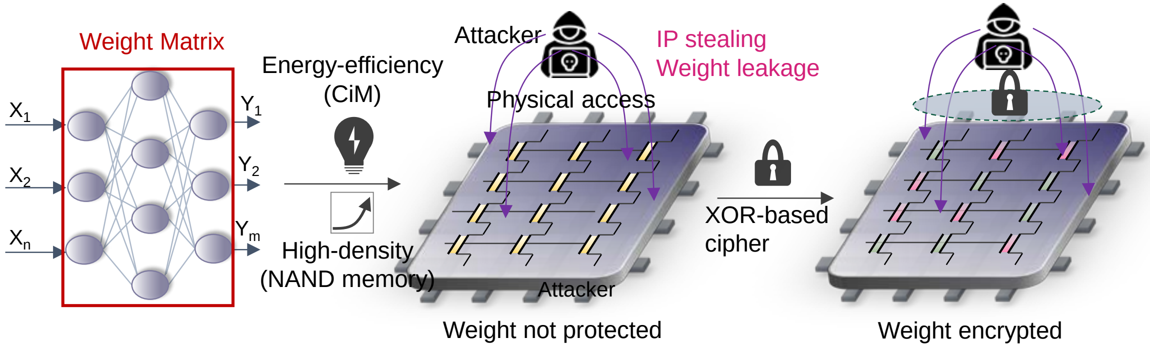
4 **Materials Discovery & Processing:** *Taming new materials and new physics.*

Topic: Ferroelectric memories

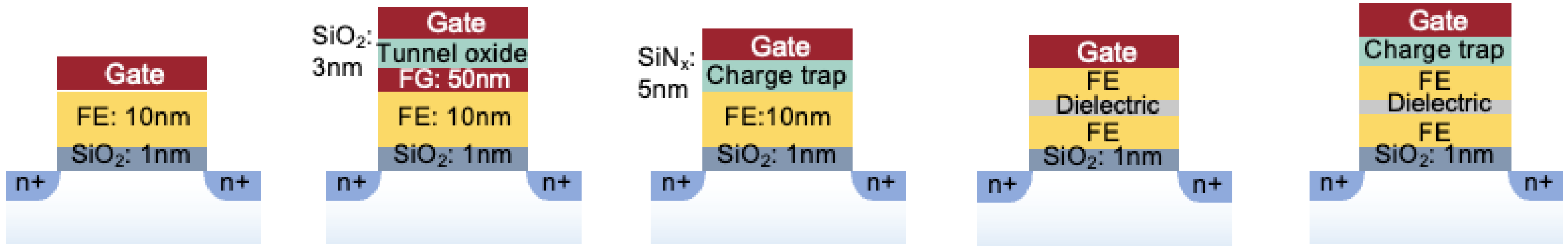
1. **PIs:** Asif Khan, Kai Ni, Michael Niemier
2. **Tasks:** 3137.022, 3137.012, 3137.013, 3137.018
3. **Application:** High-density memory
4. **Objectives:**
    a. To realize ultra-low voltage and high-speed operation of embedded applications
    b. To enable performance augmentation of DRAM and flash technologies using ferroelectric memories
    c. To explore novel architectures and new applications leveraging unique features of ferroelectrics
5. **SOTA:**
    a. Dual Layer 3-D stacked FRAM, 32 Gb capacity, 450 Mb/mm^2 density, near DRAM performance (Ramaswamy et al. Micron, IEDM 2023).
6. **Approaches with feedback loops:**
    a. Connecting ferroelectric TEM microstructure with scalability, reliability and variation.
    b. Engineering electrodes and interfacial oxygen reservoirs to control imprint, retention, and endurance in capacitor and FET structures.
    c. ALD approaches to low-voltage perovskite-structure oxides
    d. Benchmarking of different compute architectures and workloads with ferroelectric memories

Topic (achievements): Ferroelectric memory and storage

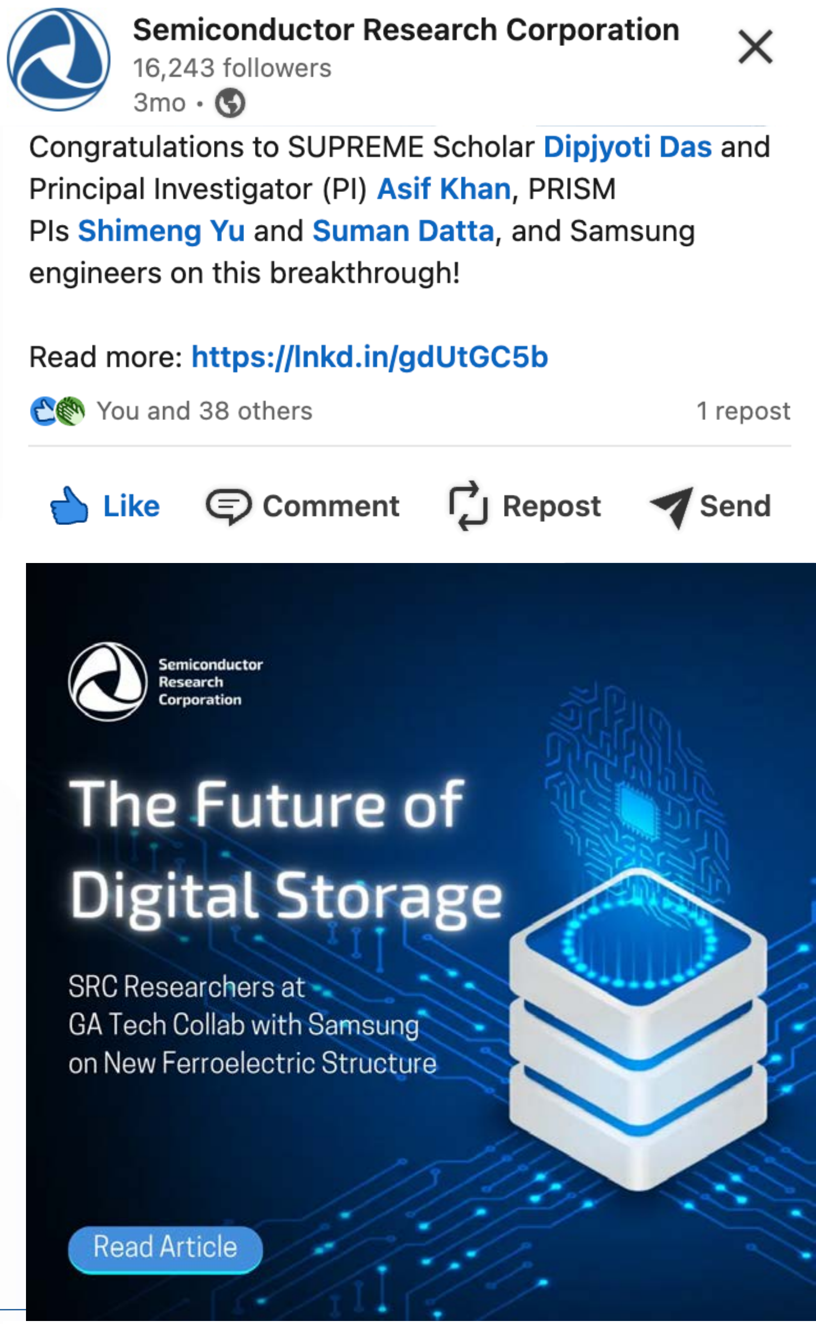
In-Situ Encrypted FeFET Array for Secure Storage and Compute-in-Memory
-Zhao, Ni, et al. IEDM 2023.



Interface design to massively enhance memory window for storage applications.
-Das, Yu, Datta, Khan, et al. IEDM 2023 – Selected as IEDM highlight for memory.
-Collaboration between SUPREME and PRISM PIs and Samsung.



SRC | SUPREME
SUPeRior Energy-efficient Materials and dEvices



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Congratulations to SUPREME Scholar **Dipjyoti Das** and Principal Investigator (PI) **Asif Khan**, PRISM PIs **Shimeng Yu** and **Suman Datta**, and Samsung engineers on this breakthrough!

Read more: **https://lnkd.in/gdUtGC5b**

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Topic: Ionic-Electronic Designer Memories

1. **PI(s)**: Bilge Yildiz (MIT), Farnaz Niroui (MIT)

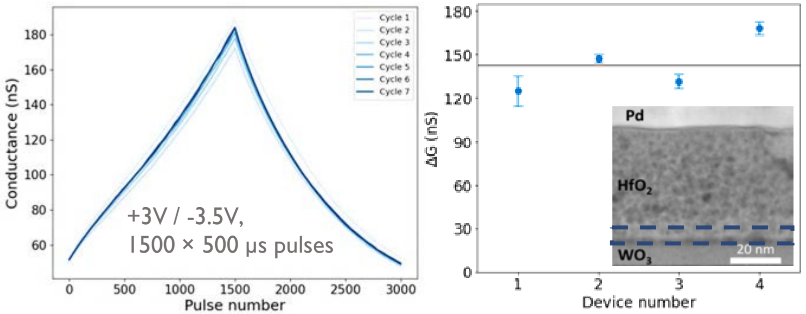
   Collaborating PIs: Jing Kong (MIT), Asif Khan (GaTech), Judy Cha (Cornell), Tomas Palacios (MIT), Kai Ni (Notre Dame), Michael Niemier (Notre Dame)
2. **Tasks:** 3137.008, 3137.017
3. **Application**: Neuromorphic and other unconventional memory and compute applications, AI hardware
4. **Objective**: Memories with programmable and deterministic conductance characteristics, and fast (ns), energy efficient (aJ) and low voltage (≤1V) modulation
5. **Approach**: 1) CMOS-compatible protonic ECRAMs, 2) Devices with transition metal redox-active complexes (TM)
6. **SOTA**: **<u>ECRAMs</u>** – Protonic ECRAMs show 5 ns multistate modulation but require 10 V; ECRAMs based on other ions show µs to ms operation. **<u>TM memories</u>** – Leading examples report multistate behavior and figures of merit competitive to emerging RRAM (<1 V, <30 ns, >10^{12} cycles endurance) but limited to µm-scale devices. Limited mechanistic understanding.

Recent Accomplishments: **<u>ECRAMs</u>** – 1) Demonstrated HfO_2 as a CMOS compatible electrolyte in ECRAM. High-k HfO_2 facilitates proton conduction in nano-porous state. 2) Using $WO_3|HfO_2$ as a model system, we started assessing device-to-device variability, and found it to be much lower than the state-of-the-art RRAMs. This indicates that ECRAM can be more reliable for AI accelerators. 3) Demonstrated MoS_2 and V_2O_5 as a CMOS compatible channel materials, with controllable sensitivity to hydrogen. **<u>TM memories</u>** –1) Designed and synthesized several redox molecules, confirming thermal stability >300°C. 2) Developed a wafer-scale compatible approach to fabricating nanoscale devices based on transition metal molecular complexes. 3) Demonstrated nanoscale devices with stable and repeatable switching behavior (< 1 V and < 200 ns) using a Ru-coordination complex. 4) Developed a correlated in-situ Raman spectroscopy and electrical characterization platform for studying the device working mechanism.

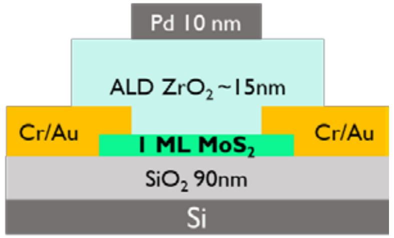
Topic (achievements): Ionic-Electronic Designer Memories

ECRAM with CMOS-compatible HfO_2 electrolyte and H-sensitive channels

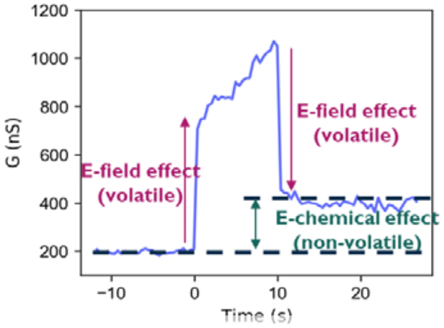
Symmetric and consistent conductance modulation of ECRAM with HfO_2 electrolyte



D-to-D variability (ongoing): +/-20%, much better than RRAM 2x-10x

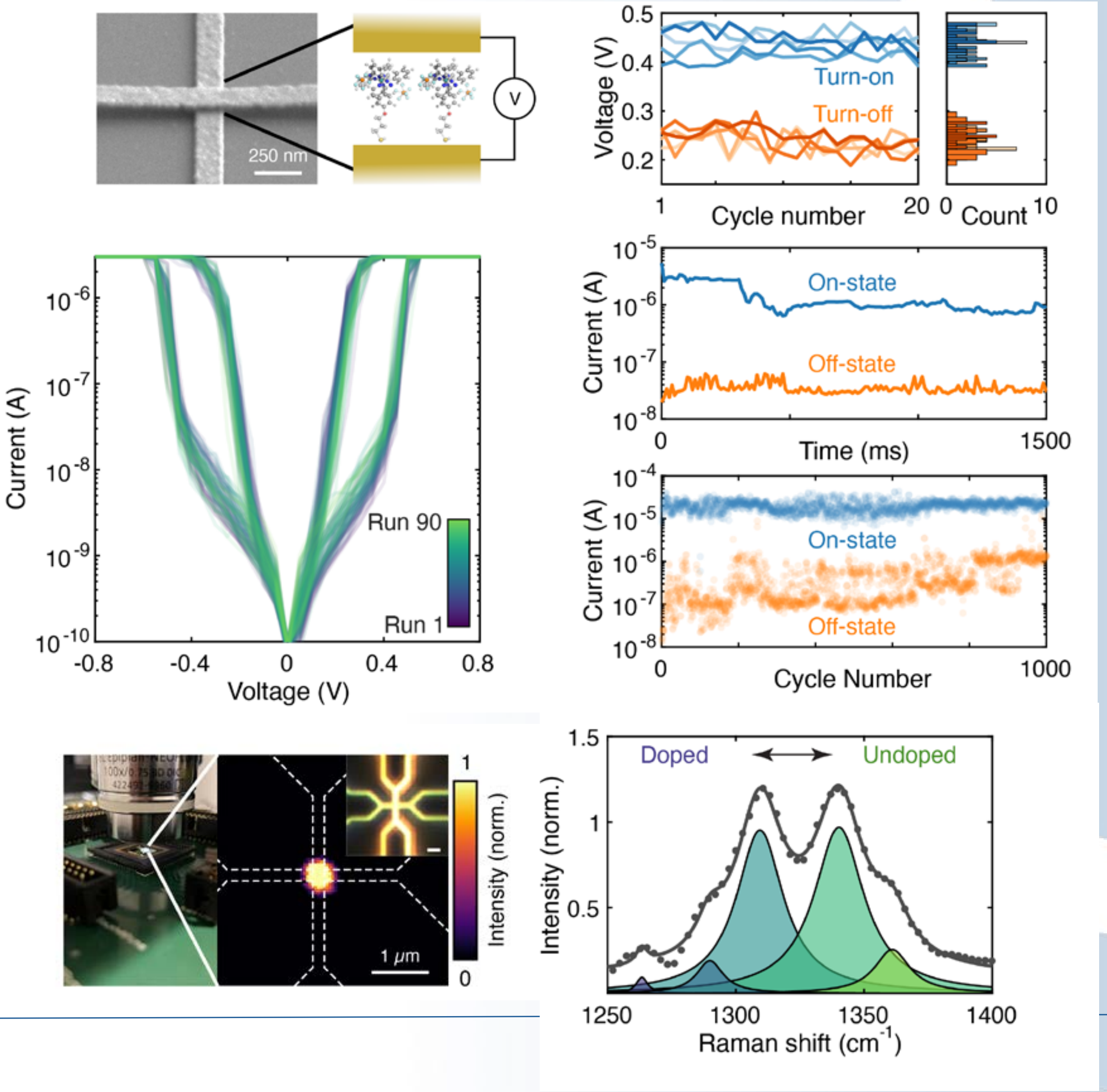


Conductance modulation of ECRAM with 2D ML MoS_2 channel



Volatile E-field effect + Nonvolatile E-chemical effect with no post-pulse transient.

TM devices show consistent switching when miniaturized to the nanoscale



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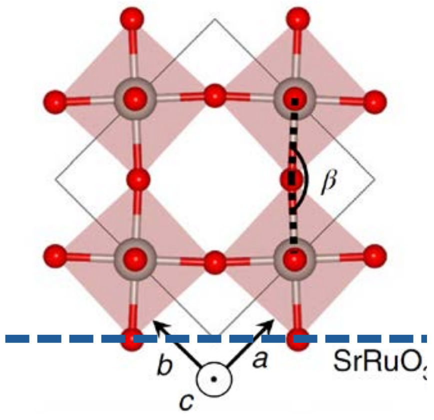
SUPeRior Energy-efficient Materials and dEvices

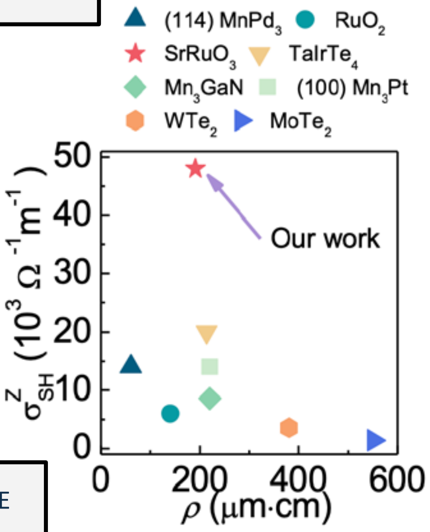
Topic: Spintronic materials and devices for logic and memory

1. **PIs:** Dan Ralph, Luqiao Liu, Farhan Rana, Darrell Schlom, Michael Niemier, James Rondinelli
2. **Tasks**: **3137.009, 3137.010, 3137.014, 3137.015, 3137.016, 3137.045**
3. **Application:** Spin-based logic and memory
4. **Objectives:**
    a. To lower down the writing currents of spintronic device to enable higher density
    b. To increase the read signals for higher memory window
    c. To reduce sensitivity of magnetic information storage element to external magnetic field
    d. To take advantage of unique dynamics of nanomagnets and new topological effects for new computing schemes
5. **SOTA:**
    a. Weak out-of-plane anti-damping spin-torque efficiency ($\xi_{DL,z}$ = 0.014 from WTe2)
    b. Low Inverse spin Hall Readout from metals for MESO device (Ta V/I = 1.7 Ω)
    c. Low TMR from MTJ based on antiferromagnet and topological semimetals (TMR ~ 0.1%)
    d. Simple magnetic free layers have coercive fields well below 0.1 Tesla
    e. High sensitivity of probabilistic device to environment, hard to pass true random number generation test.
6. **Approaches with feedback loops:**
    a. Low-symmetry conductors, magnets, and antiferromagnets as spin-source layers
    b. Anomalous Hall effect in topological insulator/magnet structures for high readout signal
    c. Explore antiferromagnetic topological material to achieve high spin polarization
    d. Combine SOT and STT to provide control over the probabilistic switching of nanomagnet
    e. Use intrinsic or synthetic antiferromagnet as the switching component in SOT-MRAM

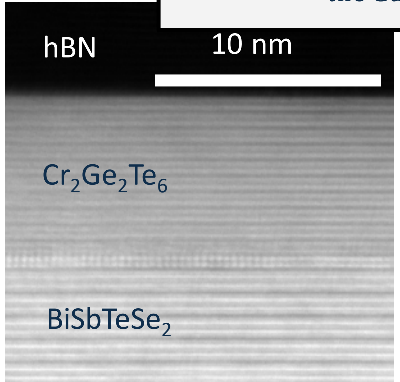
Topic (achievements): Spintronic materials and devices for logic and memory

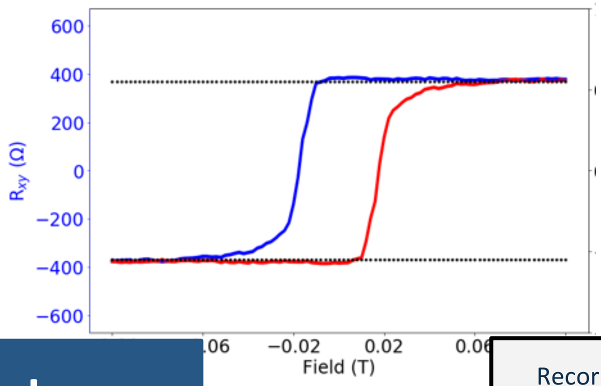
Record out-of-plane antidamping efficiency (0.092) from SrRuO3 (**Ralph**)

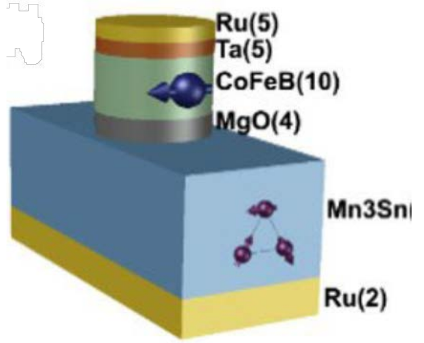




Record anomalous Hall signals in $BiSbTeSe_2/Cr_2Ge_2Te_6$ samples up to the Curie temperature of the magnets (**Ralph**)







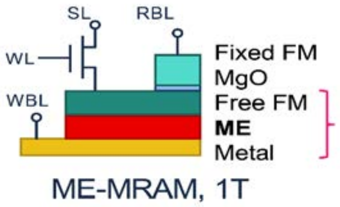
Novel Materials

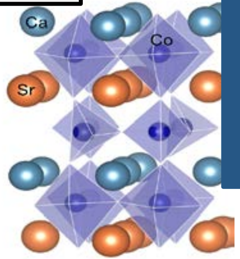
Record High TMR from Antiferromagnet MTJ (**Liu**)

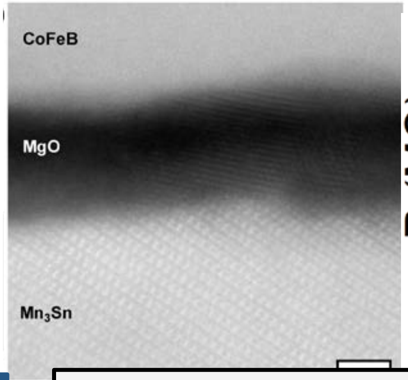
Theory and Calculation

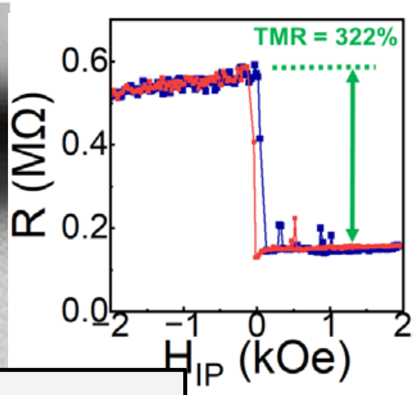
New Mechanism

Multiferroics Prediction with Large ME efficiency (**Rondinelli)**







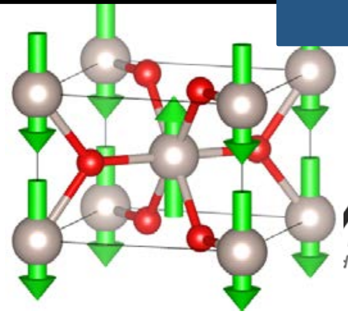


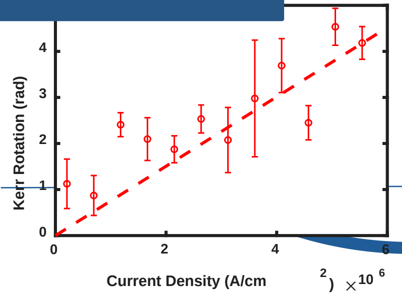
Fast characterization of spin Hall angle with optical Kerr effect method (**Rana**)

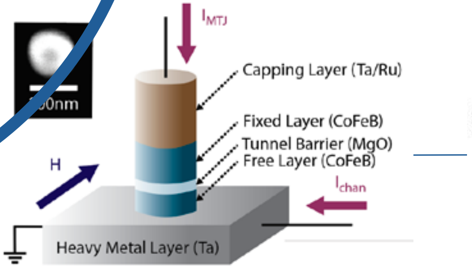
METROLOGY

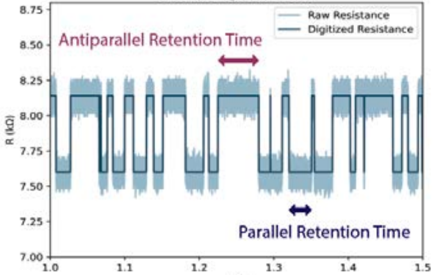
Devices

MTJ passing NIST random number test (**Liu**)









Topic: memory benchmarking

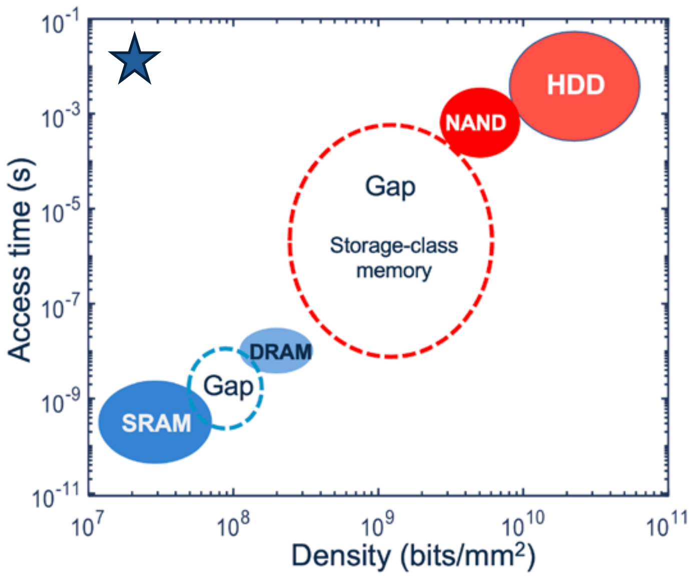
1. **PIs:** Niemier [Khan, Liu, Ni, Niroui, Ralph, Yildiz, SUPREME], [Gupta (CHIMES), Gupta (CoCoSYS), Martínez (ACE), Naeemi (CoCoSYS), Raghunathan (CoCoSYS)]
2. **Tasks:** 3137.{008, 009, 011, 010, 012, 013, 014, 015, 016, 017, 018, 027}
3. **Applications:** Device- and materials-driven, application-level benchmarking
4. **Objectives:**
   a. Identify value proposition (if any) when SUPREME memory technologies used as drop-in replacement for memory cell {SRAM, DRAM, Flash, ...} in existing memory hierarchy
   b. Identify value proposition (if any) for technology-enabled compute-in-memory architecture that exploits SUPREME memory technology in context of application-level workload (ideally identified by vertical JUMP 2.0 centers)
   c. Identify impact of necessary peripherals for options (1) and (2) + how (at scale) peripherals impact application-level FOM
   d. Identify {materials, device} design levers that maximize improvements to application-level FOM
5. **SOTA:**
   a. Established architectural solutions (e.g., GPU, TPU, HBM @ advanced technology node)
   b. In-memory prototypes from academic, industrial collaborators
6. **Approaches with feedback loops:**
   a. Highly-scaled memory devices as drop-in replacement for traditional memory hierarchy (possibly multi-bit storage)
   b. Highly-scaled memory devices used in in-memory computing architecture (with nominal compute functionality); key compute kernels workloads informed by vertical center research
   c. Layout-based analysis at advanced technology nodes to identify optimal paths at materials, device-levels to derive application-level benefits

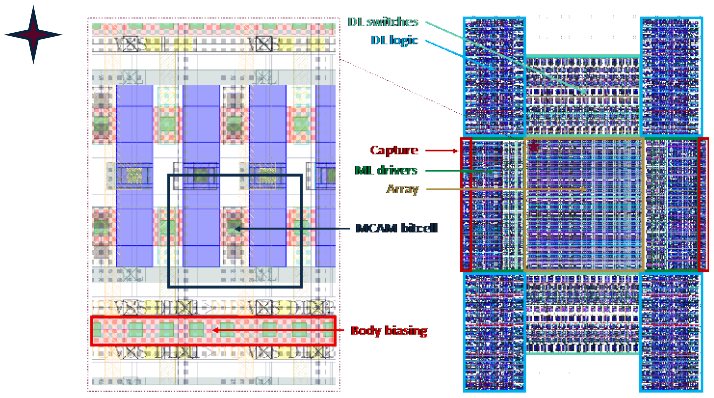
Topic (achievements): End-to-end benchmarking

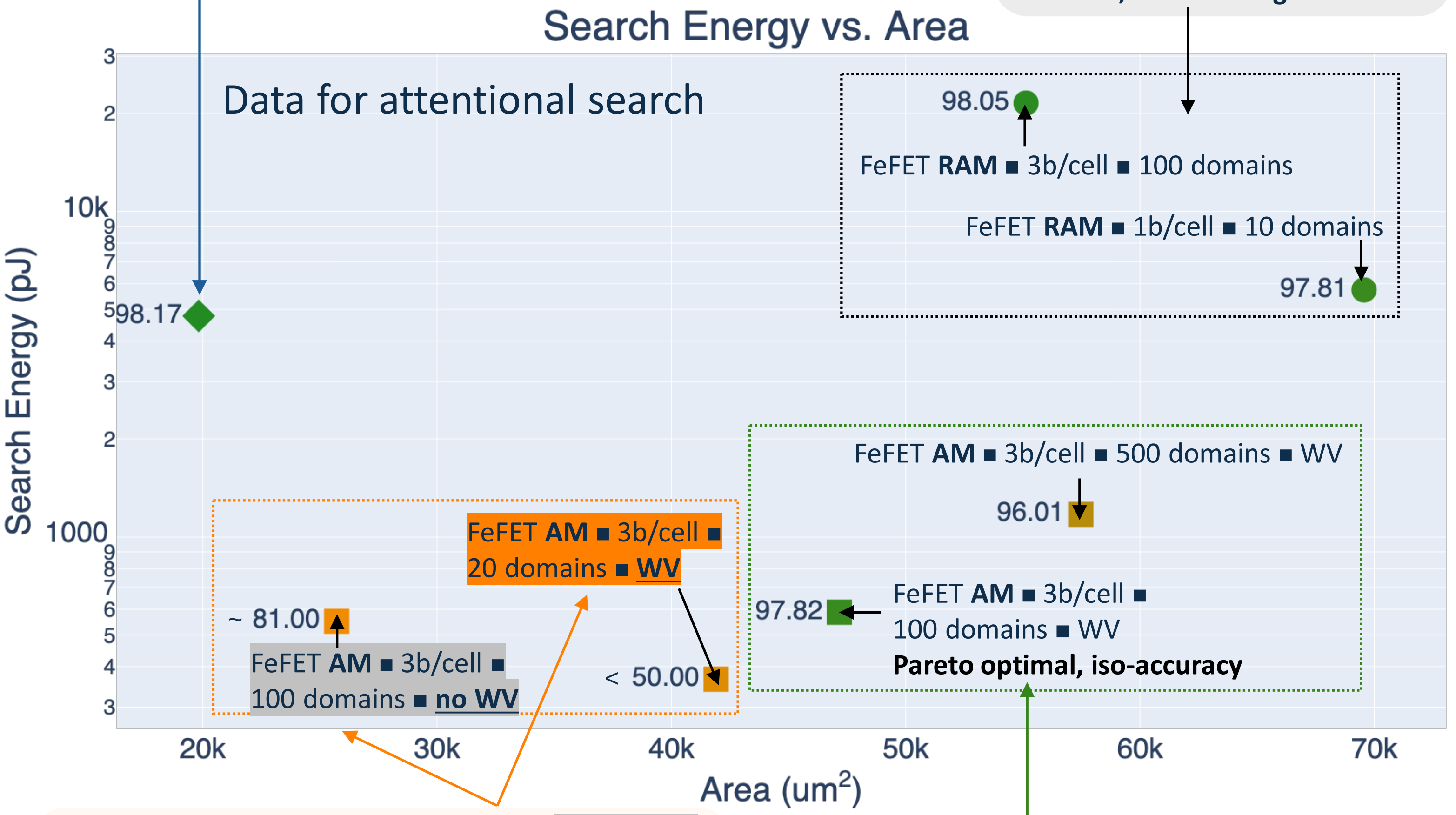
① Establish baseline with SOA CMOS memory hierarchy with trends from ★ (e.g., @ 5 nm node) for given workload

② Check advantage if use device as drop-in replacement *after* accounting for necessary peripheral overhead ✦

Here, no advantage





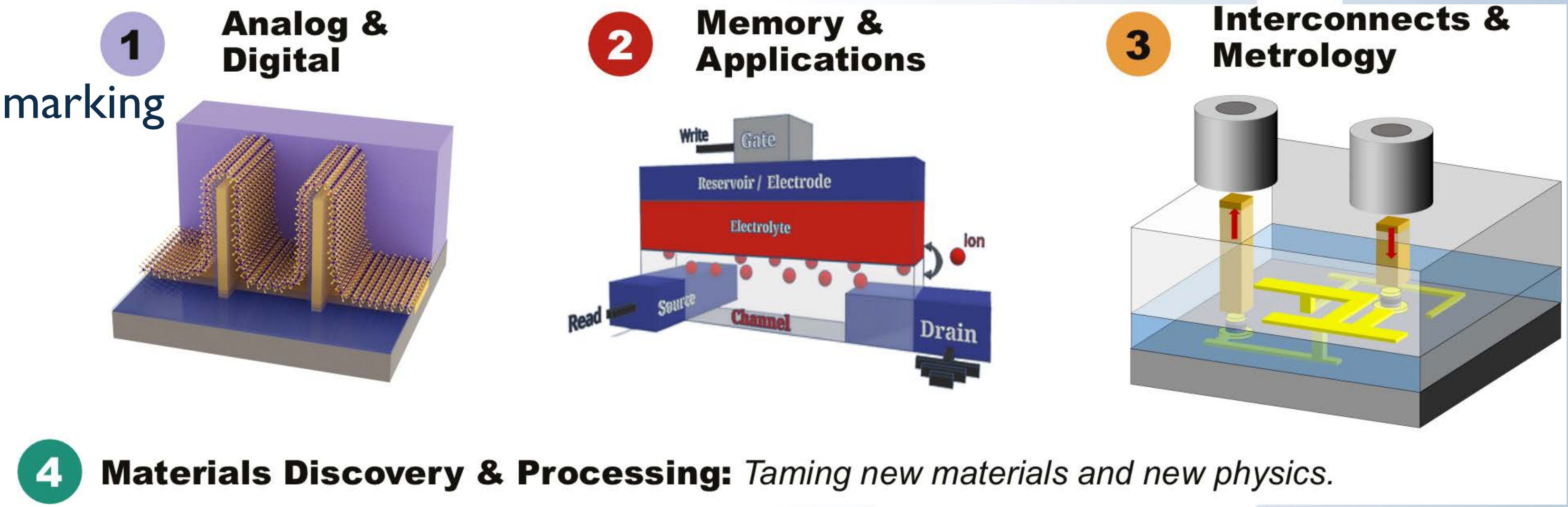


④ **[Feedback]** mitigating stochasticity to avoid write-verify has >> impact on area than device scaling with write-verify owing to reduced peripheral overhead ■ without mitigation, accuracy drops

③ Using inherent compute capability provides Pareto optimal solutions ■ device stochasticity requires write-verify for iso-accuracy solution

Topics in SUPREME

1. 2D materials & devices
2. Nitride materials & devices
3. Oxide materials & devices
4. Ferroelectric memories & benchmarking
5. Spintronic materials & devices
6. Ionic materials & devices
7. **Electrical interconnects**
8. **Optical interconnects**
9. Metrology
10. High-throughput materials discovery
11. Advanced processing
12. High-k dielectrics & ferroelectrics



Materials Discovery & Processing: *Taming new materials and new physics.*

Topic: Materials for high-conductivity interconnects

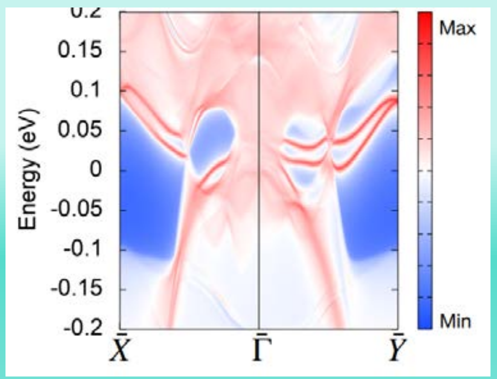
1. **PIs:** Daniel Gall, Judy Cha, Christopher Hinkle, Hong Tang, James Rondinelli
2. **Tasks**: **3137.019, 3137.020, 3137.021, 3137.026, 3137.038, 3137.046**
3. **Application:** High-conductivity narrow interconnects
4. **Objectives:**
   a. To identify materials with high conductivity at small < 10 nm dimension
   b. To develop thin film synthesis methods including control of composition and crystalline direction
   c. To develop nanowire fabrication processes
   d. To demonstrate high-conductivity narrow wires with < 400 Ω/µm for 8 nm line width
5. **SOTA:**
   a. Cu with Ta/TaN or Co liner: 4,000 Ω/µm (extrapolated to 8 nm line)
   b. Co with Ti(N/C) liner: 2,000 (extrapolated to 8 nm line)
   c. Ru: 800 Ω/µm (imec 2024, 9 nm line)

6. Approaches with feedback loops:
   a. First-principles computational search for new topological conductors (Rondinelli)
   b. High-throughput thin film materials synthesis (Hinkle)
   c. In-situ transport on epitaxial layers for resistivity benchmark (Gall)
   d. Direct high-throughput wire synthesis through nanomolding (Cha)
   e. Top-down lithography for <10-nm-line fabrication and transport measurements (Hong)

Topic (achievements): Material down-selection for interconnects

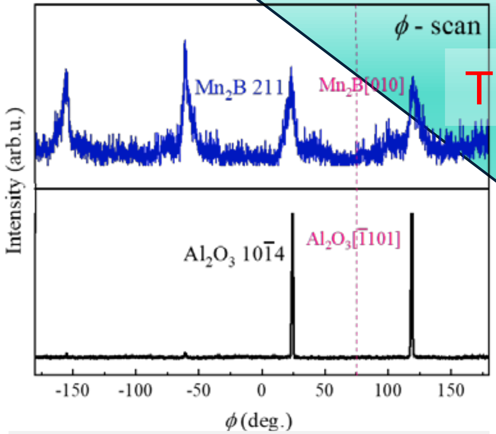
Start: 10^6 possible compounds

Computational Materials Search



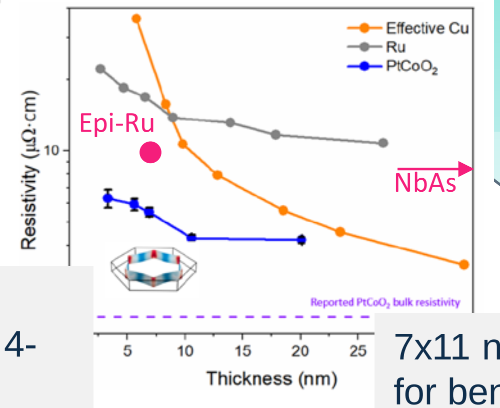
Fermi-arcs indicate promise as inversion-broken Weyl semimetal for new metal-rich nitrides (Rondinelli)

Thin Film Synthesis



Epitaxial growth of $Mn_2B(100)$ on R-plane sapphire (Gall)

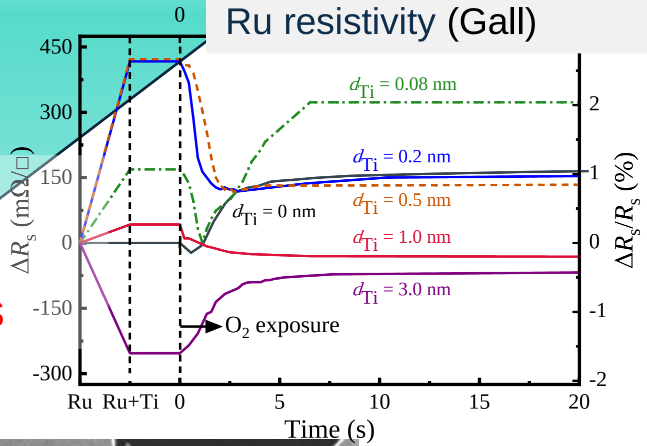
Transport on blanket layers



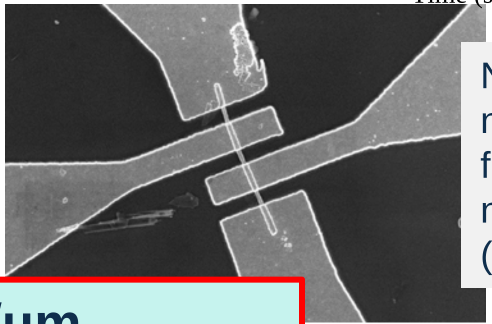
Thin film resistivity of $PtCoO_2 < 7$ μΩ-cm for 4-nm-thickness

Metal-liner interface

Ti liner thickness affects Ru resistivity (Gall)

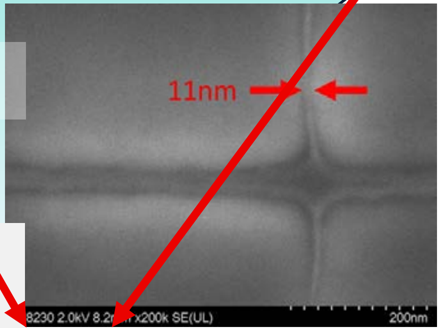


Direct Nanowire Synthesis



NbAs nanowire fabricated by nanomolding (Cha)

Line fabrication

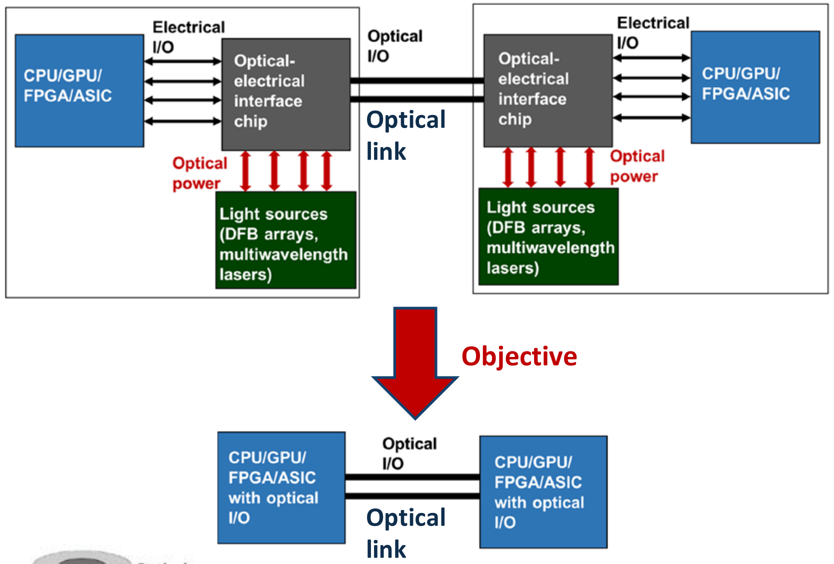


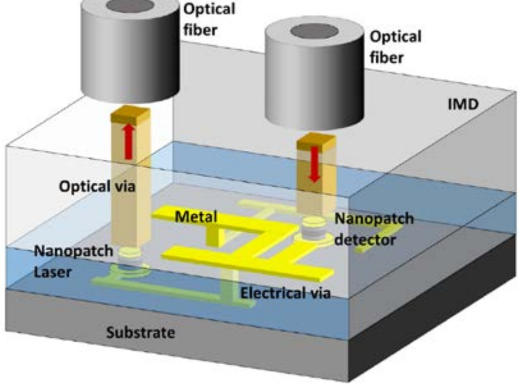
7x11 nm epitaxial Ru line for benchmarking (Hong)

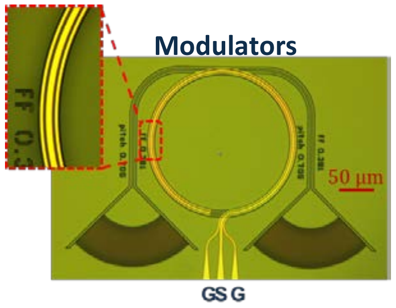
Goal: Demonstration of one 8-nm-line with 400 Ω/μm

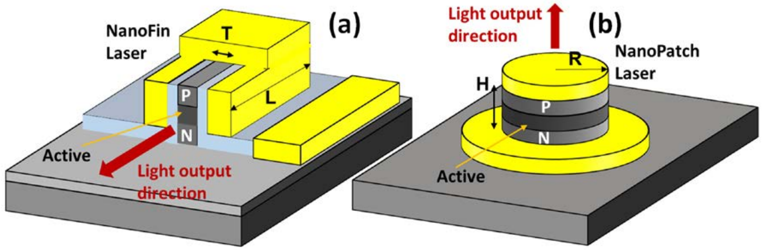
Topic: Materials and Devices for Chip-to-Chip Optical Interconnects

1. **PIs:** Hong Tang, Chris G. Van de Walle, Debdeep Jena, Farhan Rana
2. **Tasks**: **3137.023, 3137.022, 3137.034**
3. **Application:** Power and size efficient chip to chip optical interconnects
4. **Objectives:**
    a. Development of new materials and devices for optical interconnects
    b. Reduce the size and power consumption of optical components for interconnects
    c. Develop compact broadband optical modulators for BEOL placement
    d. Develop nanoscale directly-modulated optical light sources for BEOL placement
5. **SOTA:**
    a. Light sources and modulators are placed off-chip increasing system size and complexity
    b. Compact modulators are not broadband and require exacting temperature stabilization (<0.5^{o}K variation tolerable)
    c. Light sources have large footprints and power consumptions, and slow direct modulatio speeds (typically <40 GHz)
    d. Most optical materials are not BEOL compatible
6. **Approaches with feedback loops:**
    a. Development of new highly nonlinear materials (>5X of LBO) for optical modulators
    b. Development of nanoscale, high-modulation bandwidth (>150 GHz), light sources
    c. Explore BEOL compatible materials
    d. Discover new materials and device structures via computational studies, metrology, and characterization

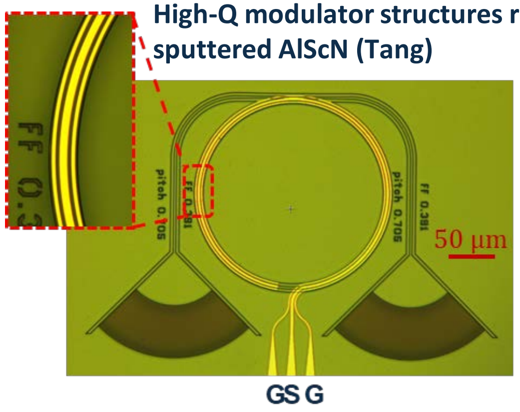




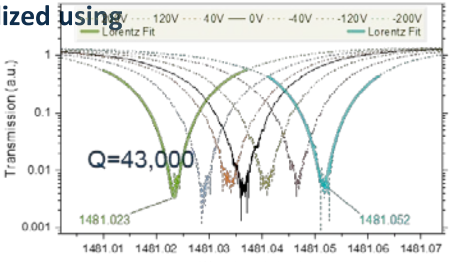


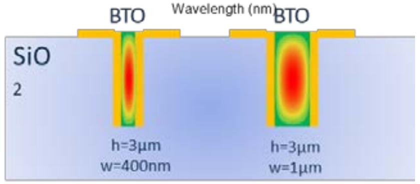


Topic (Achievements): Materials for Chip-to-Chip Optical Interconnects

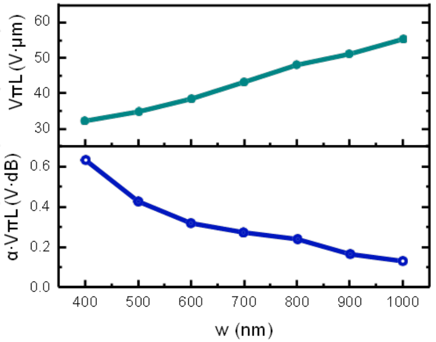


High-Q modulator structures realized using sputtered AlScN (Tang)





Compact (<10 micron) BTO modulators designed (Tang)



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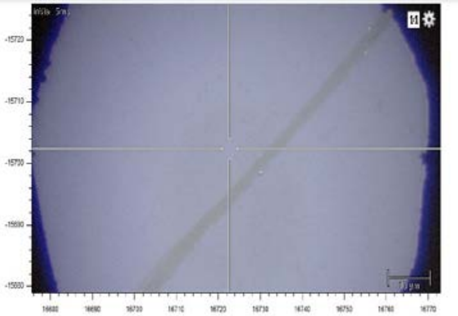
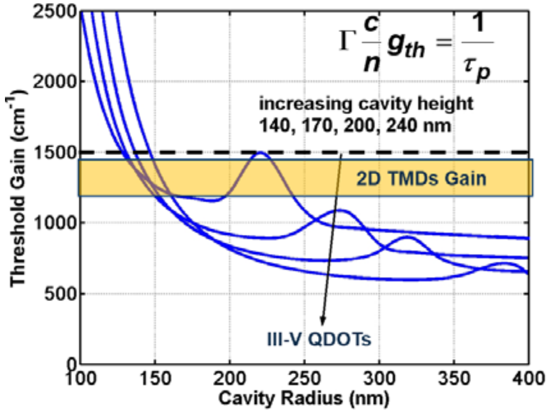
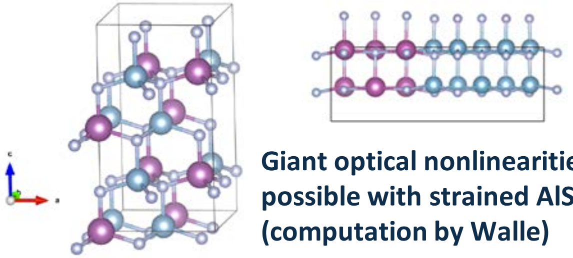


CVD grown MoS2 for laser gain materials (Kong)

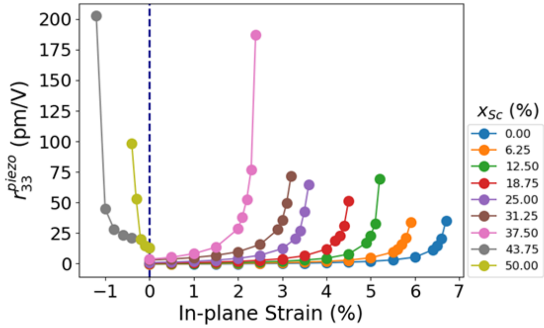


Laser designs using BEOL compatible 2D laser gain materials (Rana)

AlScN/AlBN and related digital alloys as nonlinear optical materials



Giant optical nonlinearities (>5X LBO) possible with strained AlScN (computation by Walle)

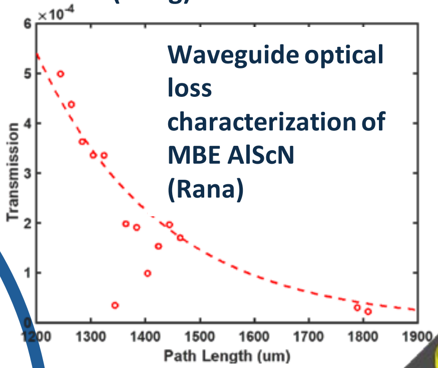


Novel Materials

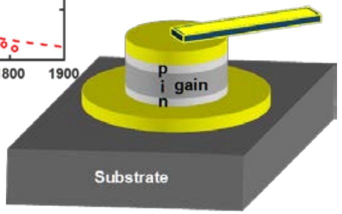
Metrology

New Material Discovery

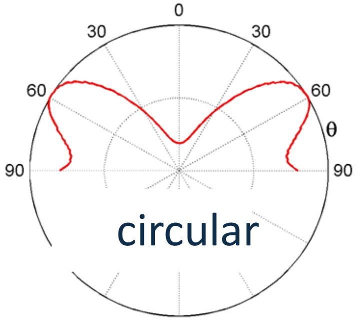
New Devices



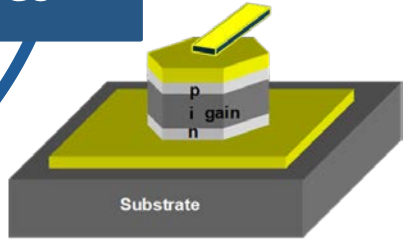
Waveguide optical loss characterization of MBE AlScN (Rana)



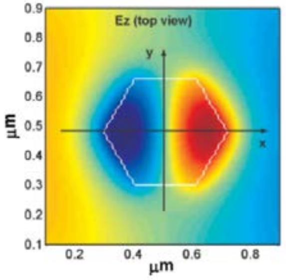
Beam pattern disruption with a top electrical contact

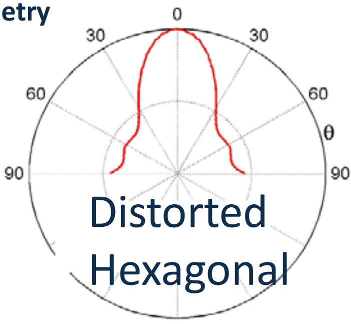


Problem solved with reduced symmetry hexagonal laser structures (Rana)



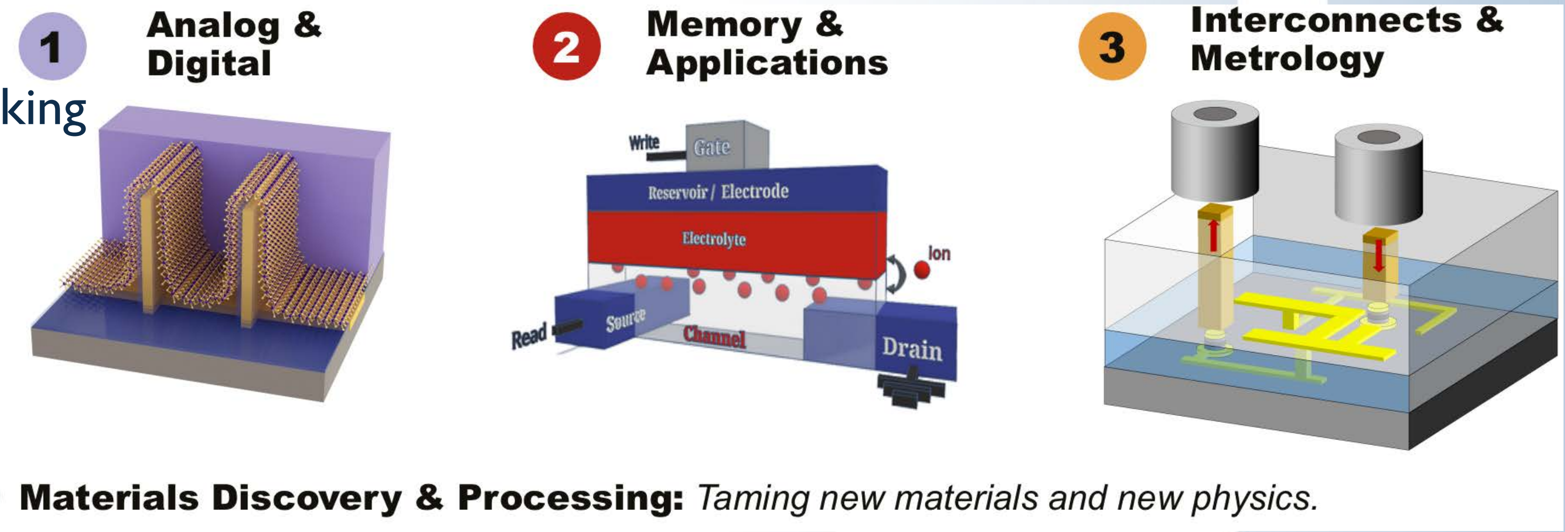
Hexagonal nanopatch laser





Topics in SUPREME

1. 2D materials & devices
2. Nitride materials & devices
3. Oxide materials & devices
4. Ferroelectric memories & benchmarking
5. Spintronic materials & devices
6. Ionic materials & devices
7. Electrical interconnects
8. Optical interconnects
9. **Metrology**
10. High-throughput materials discovery
11. Advanced processing
12. **High-k dielectrics & ferroelectrics**



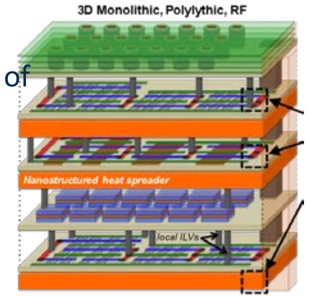
Materials Discovery & Processing: *Taming new materials and new physics.*

SRC | SUPREME
SUPeRior Energy-efficient Materials and dEvices

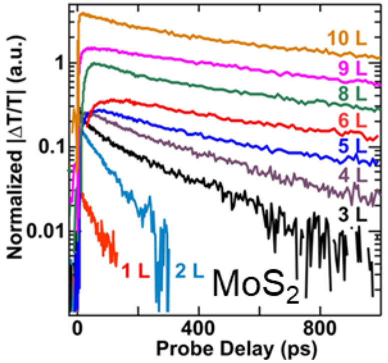
Topic: High-Throughput Metrology of Materials and Devices

1. **PIs:** Hong Tang, Daniel Gall, Eric Pop, Chris Hinkle, Elton Graugnard, Judy Cha, Farhan Rana
2. **Tasks**: **3137.026, 3137.044, 3137.025, 3137.024**
3. **Applications:** Develop rapid techniques for material and device characterization
4. **Objectives:**
   a. Measure and characterize the properties of materials being developed in the center
   b. Develop techniques for the high-throughput characterization of materials and devices and provide feedback to material synthesis and computational modeling teams in the center
   c. Develop characterization techniques for rapid material discovery via machine learning
5. **SOTA:**
   a. Most material characterization techniques require full device fabrication to access material properties and are not suitable for rapid material characterization
6. **Approaches with feedback loops:**
   a. Use optical, IR, and Terahertz techniques for material characterization
   b. Use chip-scale electron spin resonance technique for the detection and identification of defects in thin films and at material interfaces
   c. Use in-situ TEM techniques to characterize materials and devices
   d. Use Raman, SThM, and electrical techniques for studying material thermal properties
   e. Develop automated schemes for the electrical characterization of nanoscale electrical interconnect materials

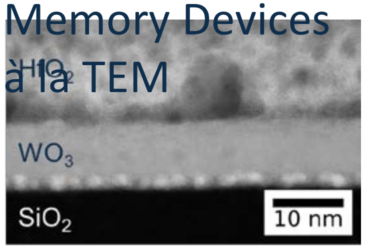
Thermal characterization of 3D stacks

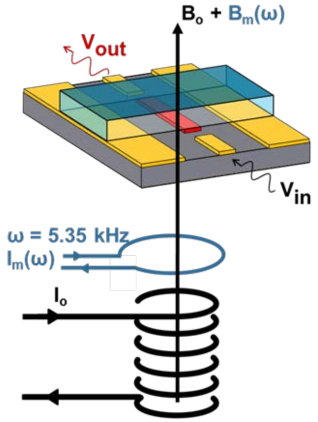


Ultrafast optical pump-probe studies

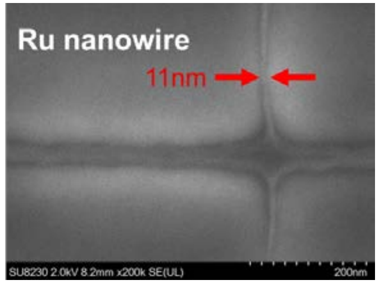


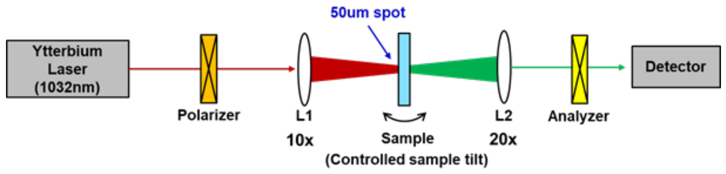
Interfaces in non-volatile Memory Devices à la TEM



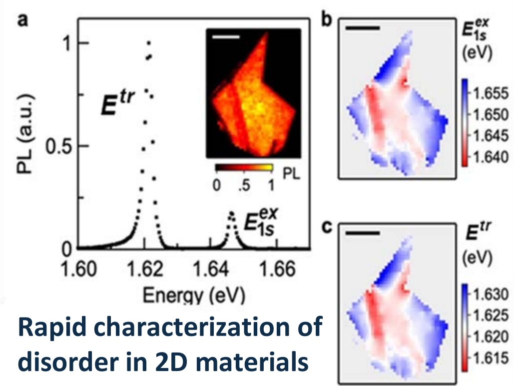


Chip-scale ESR

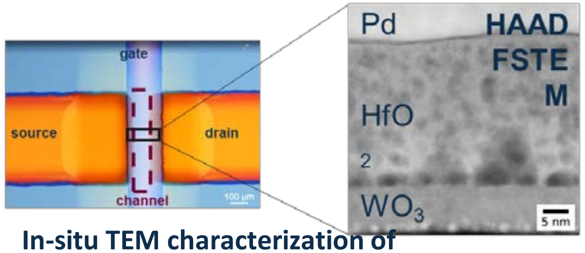




Topic (Achievements): High-Throughput Metrology of Materials and Devices

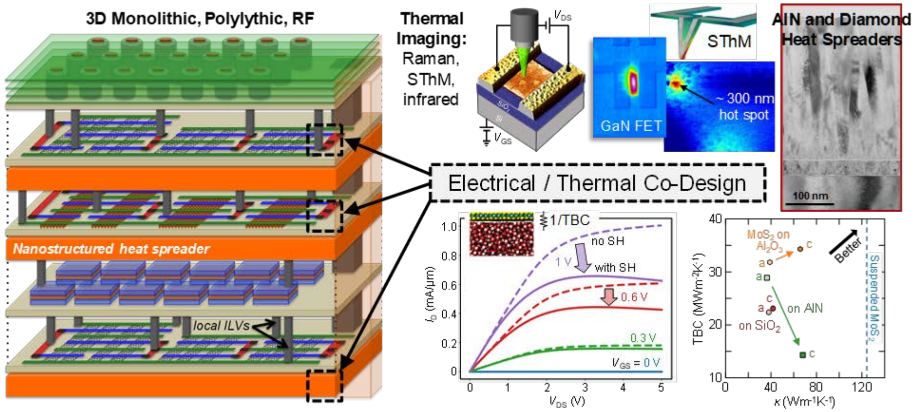


Rapid characterization of disorder in 2D materials via PL and Reflectance (Rana)

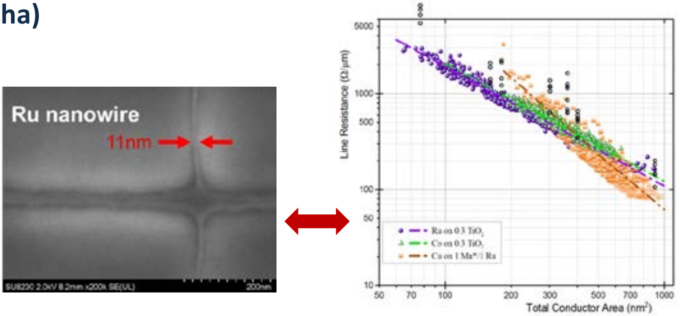


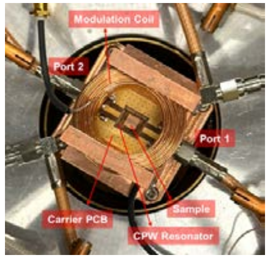
In-situ TEM characterization of proton conduction pathways in materials and interfaces for memory devices (Cha)

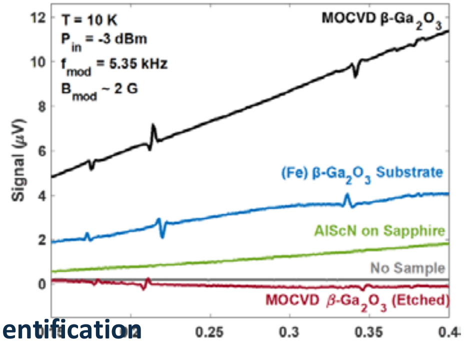
Thermal simulation of 3D memory-on-logic system & of various transistor geometries. Thermal measurements of ITO FETs and MRAM materials (Pop)



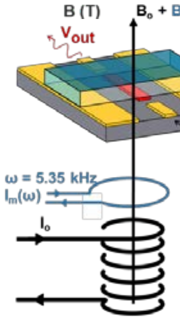
Full cycle benchmarking of Ru nanowires as small as 11x7nm (Tang)



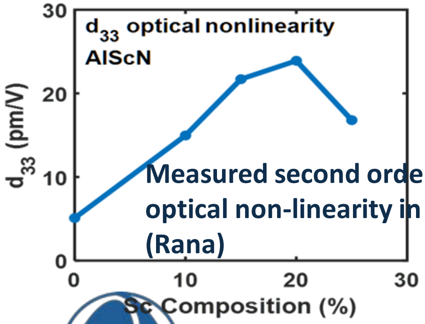




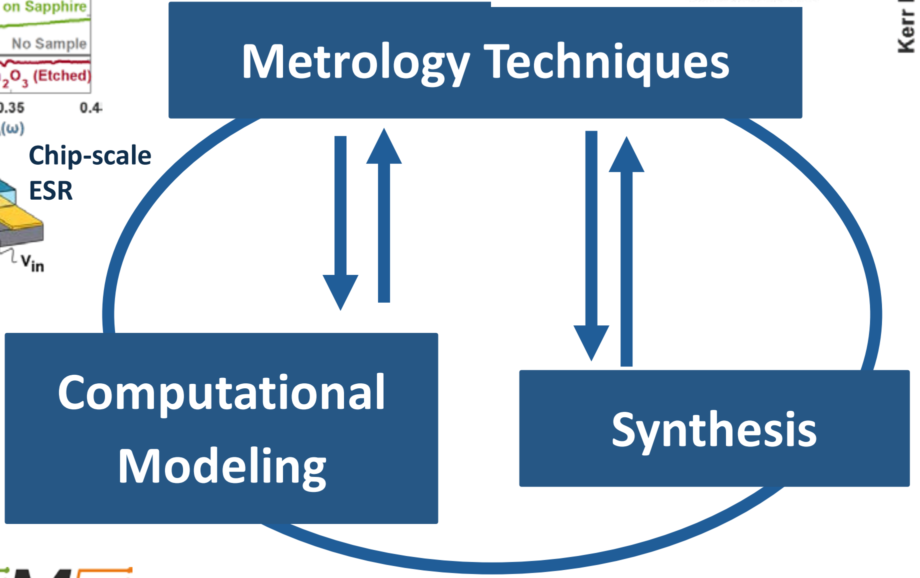
Rapid detection and identification of defects in materials using chip-scale ESR (Rana)



Chip-scale ESR



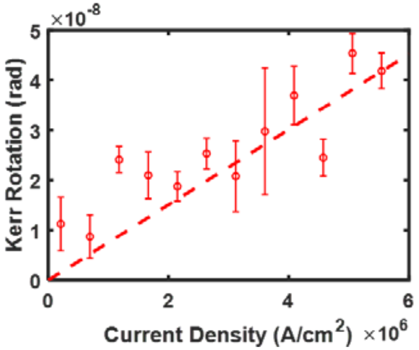
Measured second order optical non-linearity in AlScN (Rana)

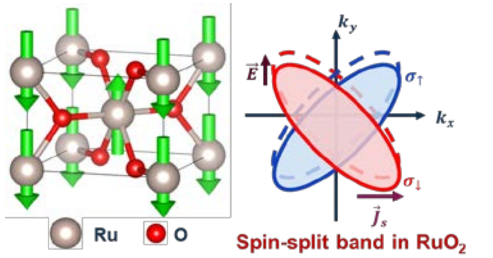


Metrology Techniques

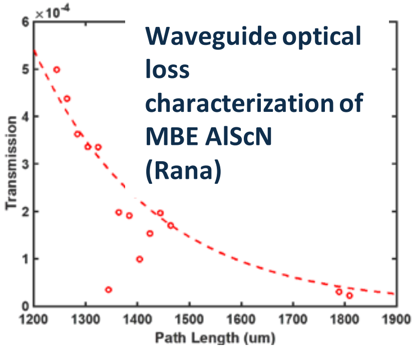
Computational Modeling

Synthesis

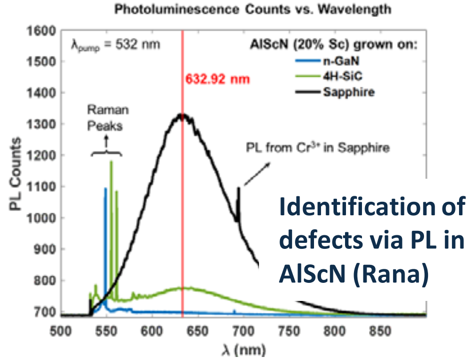




Rapid characterization of spin injection potential of materials using optical Kerr microscopy (Rana)



Waveguide optical loss characterization of MBE AlScN (Rana)

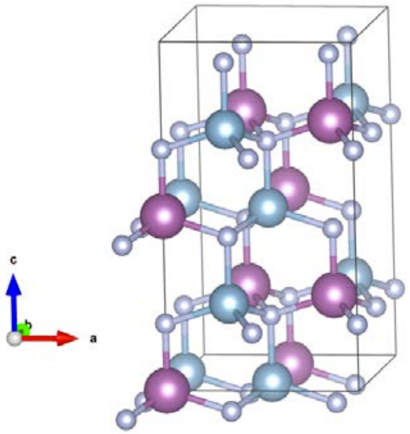


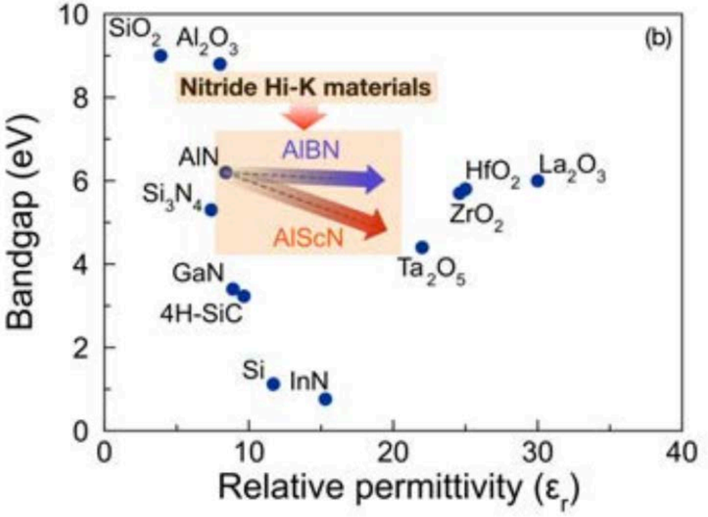
Identification of defects via PL in AlScN (Rana)

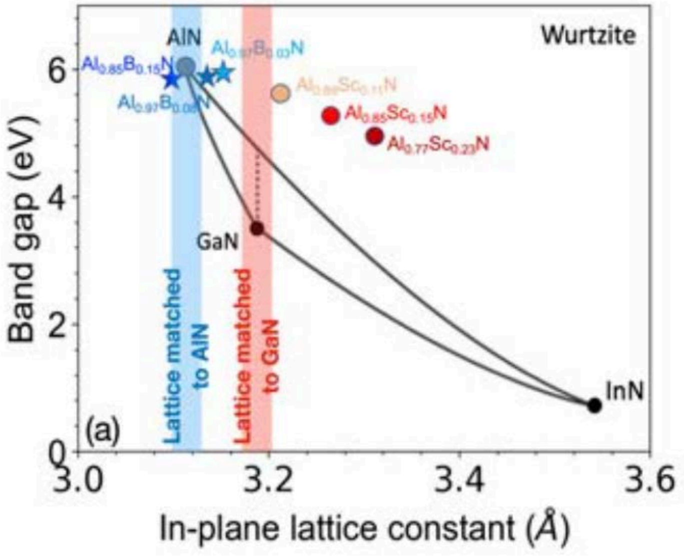
SRC | SUPREME
SUPeRior Energy-efficient Materials and dEvices

Topic: Next-generation ferroelectrics and high-K dielectrics

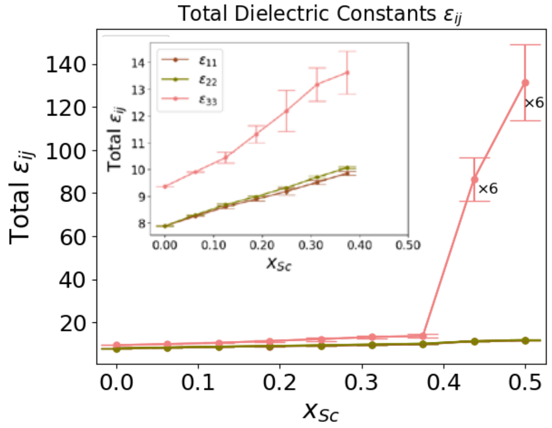
1. **PIs**: Depdeep Jena, Farhan Rana, Hong Tang, Asif Khan, H. Grace Xing, Elton Graugnard, Chris G. Van de Walle
2. **Tasks:** 3137.004, 3137.034, 3137.035
3. **Application**: Wide-bandgap transistors for high-efficiency gate drivers, RF and logic/memory hybrids
4. **Objectives**: Discovery of new high-K dielectric and ferroelectric barriers for wide-bandgap CMOS devices and circuits
5. **SOTA**: AlScN/GaN FerroHEMTs with f_{max}=150 GHz and 2 A/mm on currents, 1 V memory window
6. **Approaches with feedback loops**:
   1. First-principles calculations of AlScN, identification of microscopic structures responsible for enhancements/switching
   2. Experimental synthesis (epitaxy) and characterization; correlation with calculations
   3. Fabrication and characterization of nitride high-K/ferroelectric gated GaN HEMTs grown on full wafers
   4. Computational and experimental exploration of the AlScN barrier material space
   5. Build on insights to explore and find opportunities for other novel systems: AlBN, AlYN, AlLaN

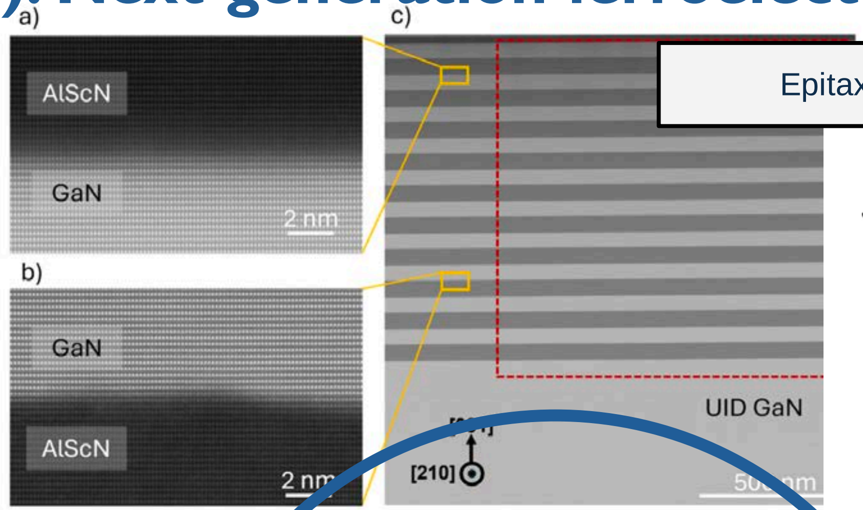






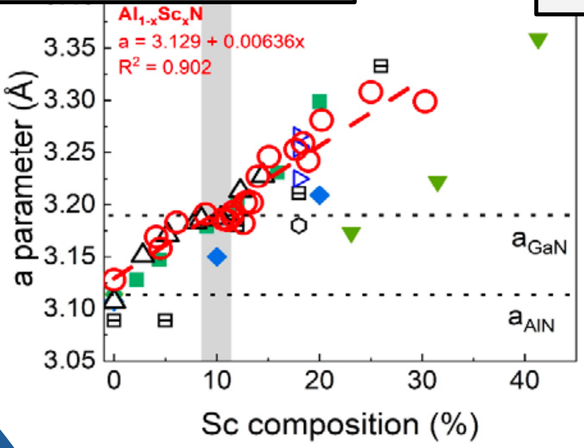
Topic (achievements): Next-generation ferroelectrics and high-K dielectrics

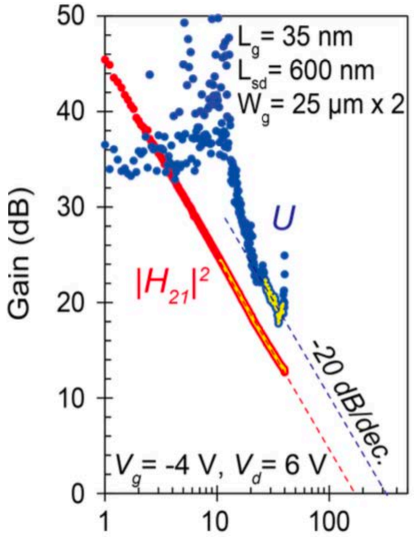




Epitaxy of AlScN/GaN

Discovery of lattice-matching conditions of AlScN

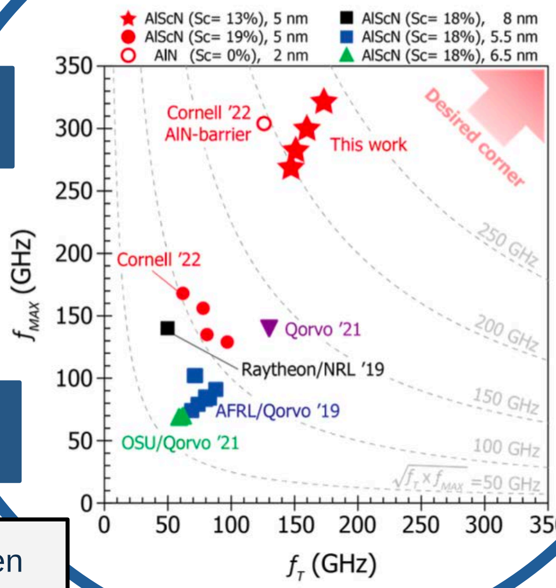




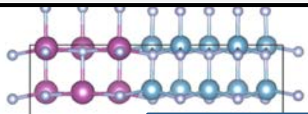
Identified atomic configurations that enhance dielectric properties

SYNTHESIS

CHARACTERIZATION

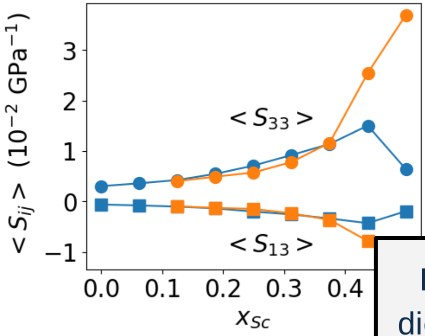


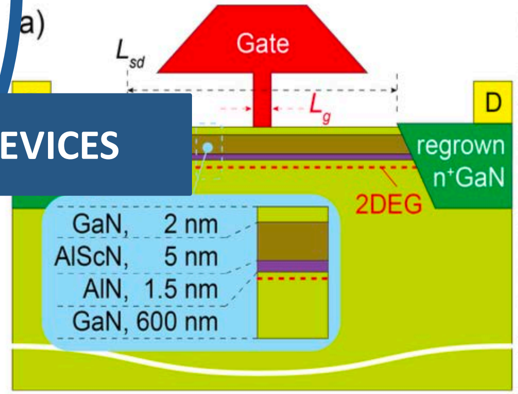
First-principles calculations of heterostructural alloys

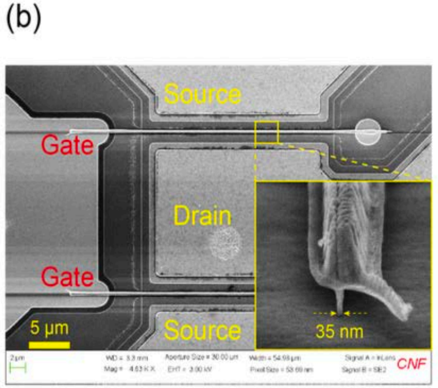


THEORY

DEVICES







Established relationship between dielectric and mechanical properties

Fastest AlScN/GaN HEMTs

Example collaborations

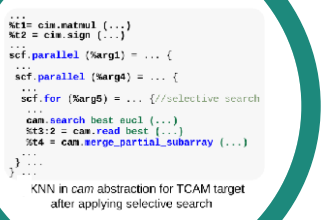
Seed projects under evaluation:

- SUPREME – PRISM
- SUPREME – CHIMES
- SUPREME – CUBiC
- SUPREME - CoCoSys

Intra-, Inter-center + industrial collaborations (memory benchmarking)

Compiler support

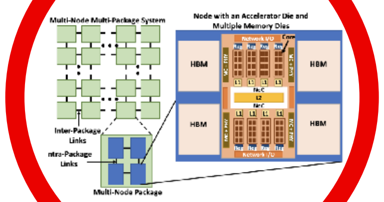
Physical layouts ⟹ more nuanced view of FOM from technology enabled architectures; compiler support impacts how often hardware employed



```
...
%t1= cim.matmul (...)
%t2 = cim.sign (...)
...
scf.parallel (%arg1) = ... {
 ...
 scf.parallel (%arg4) = ... {
  ...
  scf.for (%arg5) = ... {//selective search
   ...
   cam.search best eucl (...)
   %t3:2 = cam.read best (...)
   %t4 = cam.merge_partial_subarray (...)
  ...
 } ...
} ...
```

KNN in *cam* abstraction for TCAM target after applying selective search

With collaborators at TU Dresden studying solutions for storing FP floating point data ■ FE FP case study (error tolerance?) ■ …



Benchmarking versus HI solutions

Will logic, memory, interconnect, OR heterogenous integration have most beneficial impact on application-level FOM? (**X-Center collaborations**)

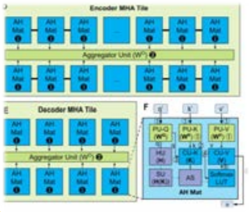
CHIMES

Joint paper at Design Automation and Test in Europe 2024

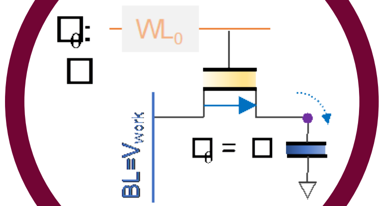
Transformers, RecSys, APs, …

Create mappings between (SUPREME) technology CIM primitives and algorithmic cores; **X-Center collaborations**

CoCoSys ACE CENTER FOR EVOLVABLE COMPUTING



Speaks to 2023 feedback: “[compare] novel device/architecture options to an existing product … for most popular applications to quantify power-performance-area benefits of novel options.



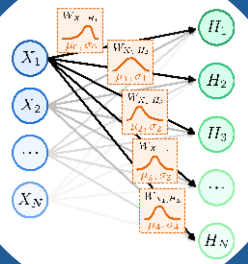
Enhanced IMC solutions

MLC functionality and/or TCAM functionality appealing ..but >> stochasticity, limits scalability? Explore 1FeFET-1C solutions with SUPREME PI Kai Ni; develop TCAM functionality

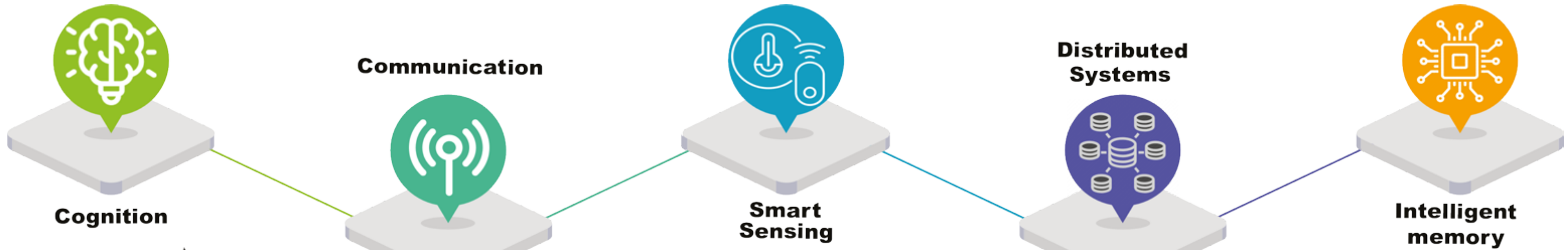
Application mapping under study: Explainable AI models ■ Database apps ■ Transformer, RecSys mappings

Explainable AI models

Leverage NVM to store distribution data associated with BNNs; amenable to MLC structures, other SUPREME memory technologies

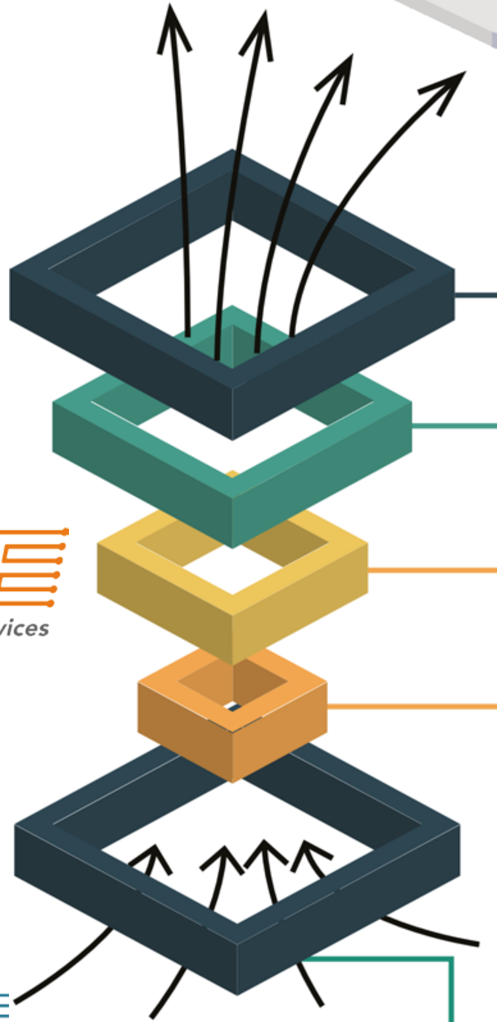


Ongoing discussions with Raytheon + other JUMP 2.0 center personnel



Center Vision

SUPREME
SUPeRior Energy-efficient Materials and dEvices



Seismic Shifts *Bridging the gap and enabling the seismic shifts in ICT.*

Application-level Benchmarking *Meeting the workload demands of the future.*

Machine Learning & Artificial Intelligence
- Hyperdimensional Computing models
- Transformer Networks — GPT-3 and beyond
- Recommendation Systems
- Perception and Autonomy

Associative Memories
- Key Value Storage
- RF Intelligence
- Bioinformatics

Physics-based Computing

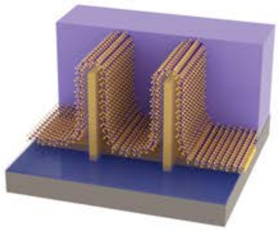
Augmented Memory Hierarchy

Impacts of Interconnects

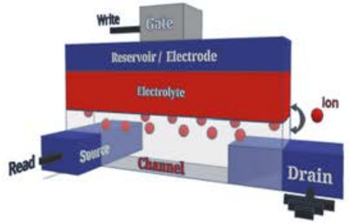
Secure Processing
- Trusted execution environments
- Homomorphic encryption

Devices & Interconnects *Accelerating innovations in Analog, Digital, Memory, Storage Devices, & Interconnects*

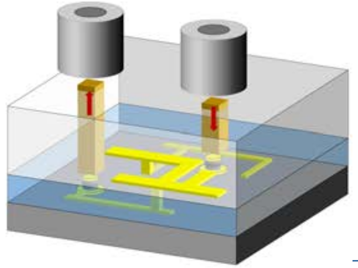
① **Analog & Digital**



② **Memory & Applications**



③ **Interconnects & Metrology**



④ **Materials Discovery & Processing:** *Taming new materials and new physics.*

Semiconductor
Research
Corporation

SUPeRior Energy-efficient Materials and dEvices

Grace Huili Xing (Cornell), Center Director

Tomás Palacios (MIT), Co-Director

Chris Hinkle (ND), co-Lead on High-Throughput

Elton Graugnard (BSU), Thrust Lead on Advanced Processing

Thomas Dienel (Cornell) Managing Director, Jenna LaMendola (Cornell) Administrative Assistant

Cornell University MIT TEXAS The University of Texas at Austin Rensselaer CU Yale ND Georgia Tech UCSB Stanford University BOISE STATE UNIVERSITY Northwestern University NCS

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