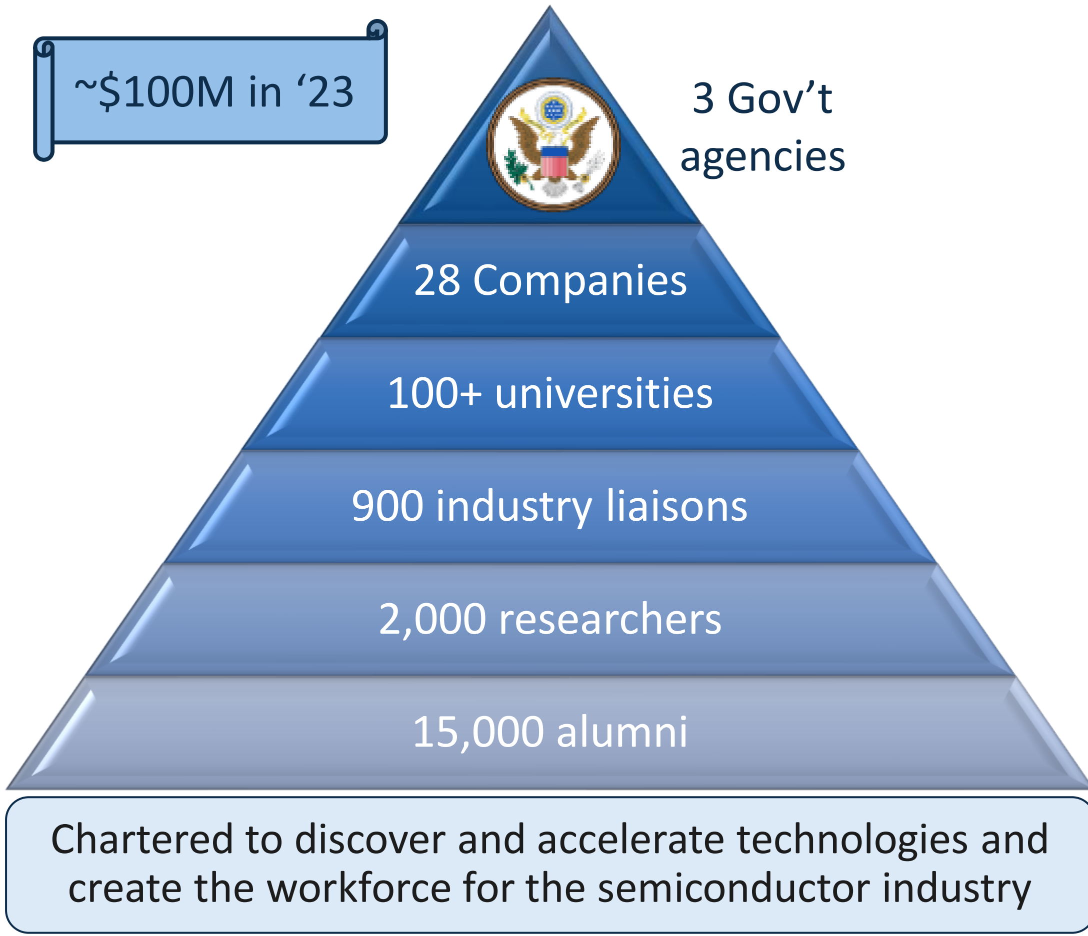
Collaboration towards MAPT Roadmap goals: Advanced Packaging Technologies

John Oakley
Science Director for Hardware Security, AI Hardware, Semiconductor Packaging, and Supply Chain AI Realized Future
www.src.org
John.Oakley@src.org

February 28, 2024

Who We Are: Premier Global Microelectronics Consortium

~$100M in '23



3 Gov't agencies

Chartered to discover and accelerate technologies and create the workforce for the semiconductor industry

Members include larger companies across the supply chain

What We Do: Manage Collaborative R&D Programs

SRC manages research programs on behalf of members;

- Recruit members
- Run solicitations
- Manage performance
- Ensures tech transfer to members

In-house Contracting, Legal, Event Production, Billing, MarCom, web portal, etc.

Members

Company 1

Company 2

Company…*n*

Government Program Office

Pool members' guidance and funds

SRC

Return tech, IP rights, students for hire

Researchers

Professor 1

Professor 2

Professor 3

Professor 4

Center 1

Professor 5

Professor 6

Professor *x*

Center 2

Professor 7

Professor 8

Professor *y*

Professor *z*

SRC members jointly define research needs, fund selected projects, and reap the rewards

PI will directly engage with experts and conduct research relevant to industry applications

SRC's Plan for the Decade

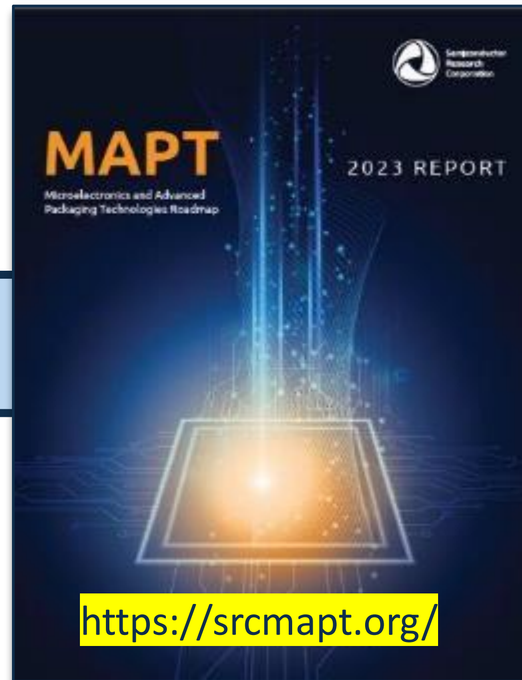
The What

https://www.src.org/about/decadal-plan/

January 2021
2030 Decadal Plan for Semiconductors

181 participants
81 organizations

The How

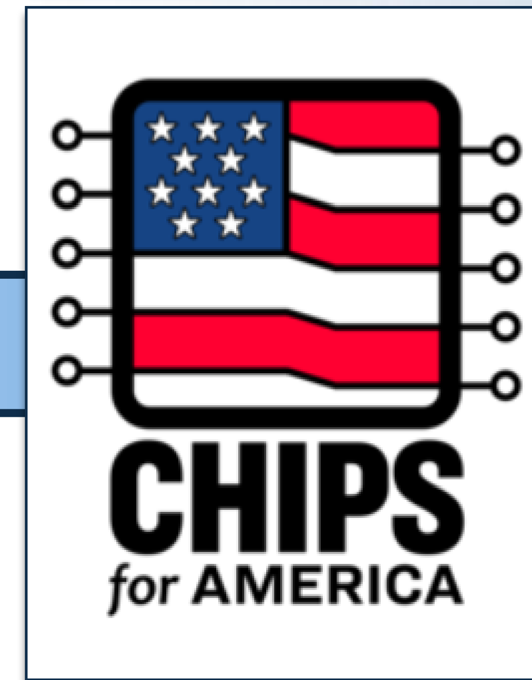


https://srcmapt.org/

October 2023
Microelectronics & Advanced Packaging Technologies (MAPT) Roadmap

300 participants
112 organizations

The Implementation



2023+
CHIPS and SCIENCE Act – 9902 Incentives and 9906 R&D Investments

www.nist.gov/chips

SRC

Let's Talk about The MAPT Roadmap

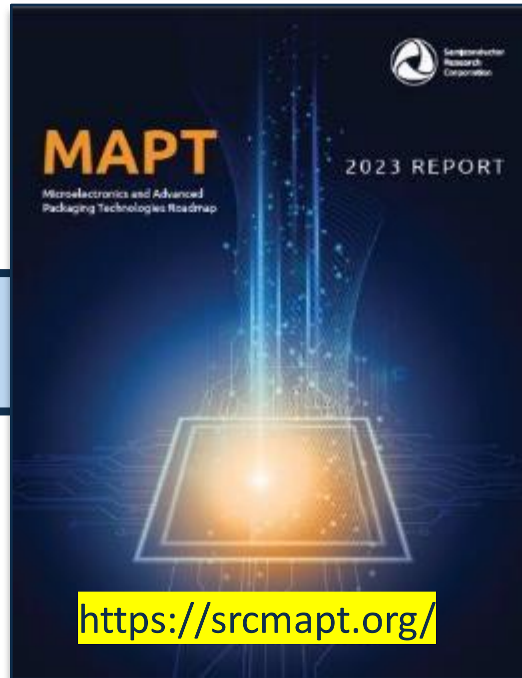
The What

https://www.src.org/about/decadal-plan/

January 2021
2030 Decadal Plan for Semiconductors

181 participants
81 organizations

The How

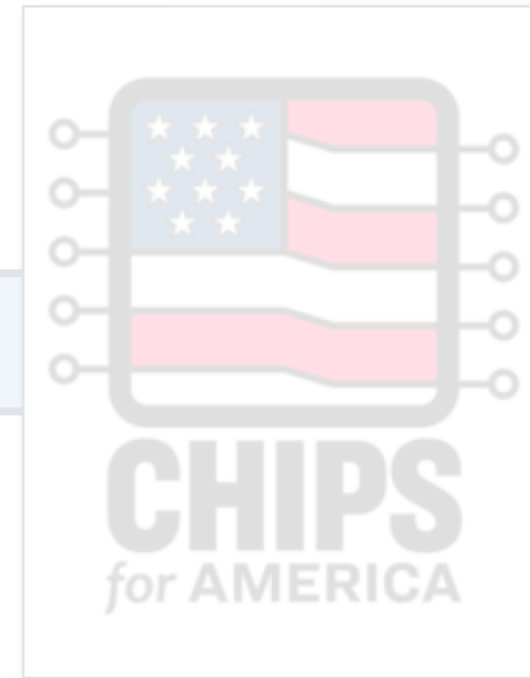


https://srcmapt.org/

October 2023
Microelectronics & Advanced Packaging Technologies (MAPT) Roadmap

300 participants
112 organizations

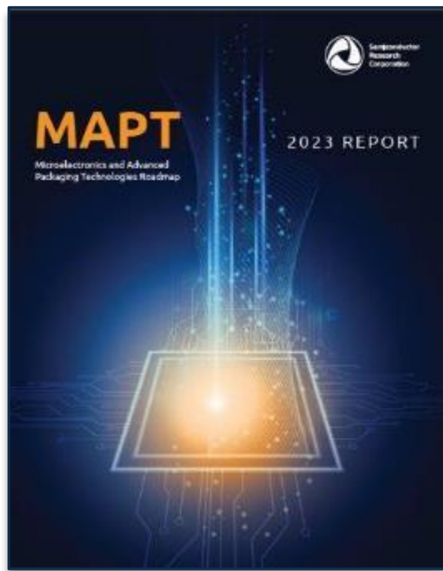
The Implementation

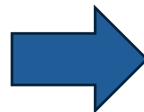


2023+
CHIPS and SCIENCE Act – 9902 Incentives and 9906 R&D Investments

www.nist.gov/chips

Critical Advanced Packaging Needs Identified in Ch. 7





Chapter 7

Advanced Packaging and Heterogeneous Integration

7.1. Introduction

Information and Communication Technologies (ICTs) are the source of exponential increase in data that must be moved, stored, computed, communicated, and secured. Traditional semiconductor technologies that rely on feature-size reduction (dimensional scaling) are reaching their physical limits.[1] Significant challenges remain in scaling up system performance as the industry moves to double transistor energy efficiency along with transistor scaling. Progress to new technology nodes has slowed to more than the two-year technology cadence. Increasingly, the need is becoming critical for "More than Moore" Heterogeneous Integration (HI) alongside "More Moore" traditional transistor scaling to achieve cost-effective Systems in Package (SiPs). HI will be fundamental to cost- and power-efficient implementations of next-generation computing and communication systems. Advanced packaging through heterogeneous integration will be critical as it "...provides an alternative avenue for innovation in density and size of products"[2]. Moreover, "just as Moore's law led the advancement of the global semiconductor industry over the past 55 years, heterogeneous integration is and will be the key technology direction going forward."[3]

Advancements in HI technologies are necessary to meet the anticipated *seismic shifts*[1] in ICT, including:

- Analog hardware required to generate smarter world-machine interfaces
- Radically new memory and storage solutions
- Hardware to address emerging security challenges in highly interconnected systems
- Artificial intelligence (AI)
- Exponential growth in energy consumption by general purpose computing

The energy consumption is doubling every three years and outpacing the efficiency improvements achieved by dimensional scaling, requiring new computing paradigms. Thus, the broad goals addressed by this chapter are:

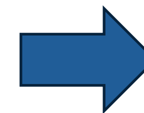
Grand Goal

To discover computing paradigms/architectures with a radically new computing trajectory, demonstrating > 1,000,000x improvement in energy efficiency.

Chapter Goal

Develop technologies for integrating analog and digital systems, including neuromorphic and quantum computing, sensing, photonics, and wireless communication.

Challenge Promising Technology Key Finding Trend Need for Foundational Capabilities 140



The scope of this chapter on Advanced Packaging and Heterogeneous Integration includes (but is not limited to):

- Chip-package architectures and codesign
- Next-generation Interconnects
- Power delivery and thermal management
- Materials
- Substrates
- Assembly and test
- Performance and process modeling and model validation
- Reliability

Cross-cutting activities under advanced packaging include:

- Energy efficiency and sustainability
- Supply chain: materials, chemicals, substrates
- Manufacturing process and performance metrology
- Security and privacy
- Design modeling test and standards

SRC

Elite Contributors

The world's experts identified the challenges and needs for advanced packaging and heterogeneous integration

Contributors

Griselda Bonilla (IBM) – *Chair*

Henning Braunisch (Intel) – *Vice Chair*

Ganesh Subbarayan (Purdue University) – *Vice Chair*

Amit Agrawal (NIST)

Bilal Akin (UT- Dallas)

David Bergman (IPC)

Kirk Bresniker (Hewlett Packard Enterprise)

Yu (Kevin) Cao (Arizona State University)

Abjhit Chatterjee (Georgia Tech)

Aiping Chen (LANL)

Gary Chen (TSMC)

Promod Chowdhury (IBM)

Bob Conner (3D Glass Solutions)

Josh Conway (America's Frontier Fund)

Mike Delaus (Analog Devices)

Patrice Ducharme (IBM)

Jeb Flemming (3D Glass Solutions)

John T. Heron (University of Michigan)

Tengfei Jiang (University of Central Florida)

Dan Jiao (Purdue University)

Dae Young Jung (SUNY Binghamton)

Pikyu Kang (Samsung)

Zia Karim (Yield Engineering Systems)

Jason Kawasaki (UW-Madison)

Matt Kelly (IPC)

Jong-Hoon Kim (SK hynix)

Walter Kocon (GlobalFoundries)

Michel Koopmans (Micron)

Deepak Kulkarni (AMD)

Gilles Lamant (Cadence)

David Landsman (Western Digital)

Thomas LeBrun (NIST)

Timothy Lee (Boeing)

Heejin Lee (SK hynix)

Sung-Kyu Lim (Georgia Tech)

Ravi Mahajan (Intel)

Babu Mandava (3D Glass Solutions)

Varughese Mathew (NXP)

Andrew Mawer (NXP)

Rajiv Mongia (Intel)

Benoit Montreuil (Georgia Tech)

Kwangjin Moon (Samsung)

John Oakley (SRC)

Valérie Oberson (IBM)

Kunal R. Parekh (Micron)

John Park (Cadence)

Mark Poliks (SUNY Binghamton)

Kaladhar Radhakrishnan (Intel)

Gnyaneshwar Ramakrishna (Cisco)

Urmi Ray (iNEMI)

Sathya Raghavan (IBM)

Sadasivan Shankar (SLAC Nat'l Lab)

Ravi Shenoy (Qualcomm)

Akshay Singh (Micron)

Suresh Sitaraman (Georgia Tech)

Spyridon Skordas (IBM)

Ilseok Son (TEL)

Eric Tervo (UW-Madison)

Sharad Vidyarthy (Analog Devices)

Chip White (Georgia Tech)

Glen Wilk (ASM)

Brett Wilkerson (AMD)

Jaimal Williamson (Texas Instruments)

Charles G. Woychik (Skywater Technologies)

Jinkyoung Yoo (LANL)

SeHo You (Samsung)

Katie C. Yu (NXP)

Ming Zhang (PDF Solutions)

SRC

MAPT Packaging Outline:

- As a ‘thank you’ to the MAPT Chapter 7 Packaging contributors you’re invited to review white papers to our MAPT Packaging program solicitation.
- If you’re interested in a project, you may sponsor it and get access to that project, and every other project selected by your co-authors potentially up to 16 projects, for the price of sponsoring your 1 project.

Dave will talk further about the opportunity

ACADEMIA • INDUSTRY • GOVERNMENT

MAPT Packaging Opportunity:

- The upcoming MAPT Packaging Webinar marks the initiation of SRC's commitment to disseminating Packaging research outlined in the MAPT Roadmap to the wider MAPT community.
- The Advanced Packaging and Heterogeneous Integration Chapter of the MAPT Roadmap received contributions from over 60 packaging experts, and we are privileged to host 3 of them who will delve into the benefits and the future landscape of collaborative packaging research.
- As the demand for chiplets continues to rise, driven by the pursuit of higher yield, node optimization, IP reuse, modularity, heterogeneity, and the development of cost- and power-efficient systems, the need for innovative research is more pressing than ever.
- SRC recognizes this urgency and is set to launch a new solicitation in packaging this spring, aiming to propel the industry forward in alignment with the MAPT Roadmap.

Target Date & Time:

February 28th at 2:00-3:30pm ET

Agenda:

Time	Topic	Speaker
2:00 PM - 2:10 PM	Introduction	John Oakley SRC
2:10 PM - 2:20 PM	Benefits of jointly funded research in packaging	Katie Yu [confirmed] NXP
2:20 PM - 2:30 PM	Advantages of collaboration for academia	Ganesh Subbarayan [confirmed] Purdue
2:30 PM - 2:40 PM	Future needs of packaging research	Brett Wilkerson [confirmed] AMD
2:40 PM - 2:50 PM	Business opportunity	Dave Henshall SRC
2:50 PM - 3:30 PM	Open Q & A	

SRC event is on SRC.org and will have the presentations and recordings once available: https://www.src.org/calendar/e007890/

MAPT Packaging Program Timeline

Encourage your favorite academics to share concept papers!!

Work your preferred selected concepts to make proposals the most relevant to your company

Feb 28: Webinar
- Announce Program

Thru April 1: Agree to review concept papers
- Join risk-free

Initial Go/ no-go

April 1 – May 1: Open Solicitation
- Chapter 7 will be announced as the topics of interest
- Collect 100s of concept papers

Thru June 1: Review and Select Concept Papers
- Members select which will be invited for full proposals

Final Go/ no-go

June 5 - July 5: Develop Full Proposals
- Members will select which proposal(s) they want to sponsor

August 5: Review and Select Projects to Fund
- Projects will be contracted by SRC before project starts

Jan 1, 2025: Research Begins
- Able to join as liaisons/ subject matter experts to all selected projects
- Able to work with PIs and students at launch of project

Feb 1, 2025: Payment due to SRC
- Y1 payment due

Risk-free:
- Can cancel after seeing concept papers with no obligation
- If continuing, no payment due until Feb 2025
- Initial Go/ no-go: 12 or more participants agree to sponsor at least 1 project each
- Final Go/ no-go: Commitments of at least 10 projects are needed to proceed

SRC's Thought Leadership That Positions Our Industry

2D Wafer Scaling

1st research roadmap across industry

1984
SRC 10y goals

1990
Microtech 2000

1992
SIA/SRC NTRS

National Technology Roadmap for Semiconductors

1998
ITRS

2019
SIA Blueprint

2021

2023

SRC's Decadal Plan

1987
SEMATECH

1999
SRC-MARCO

Massive DARPA-MTO investments in semiconductors

2005
SRC-NRI

Massive NSF and NIST investments in semiconductors

2017
DARPA-ERI

JUMP
nCORE

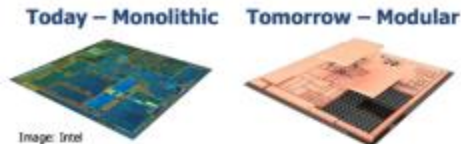
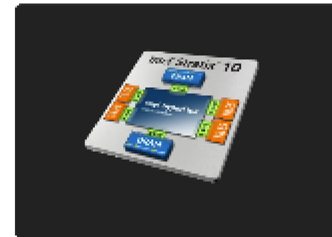
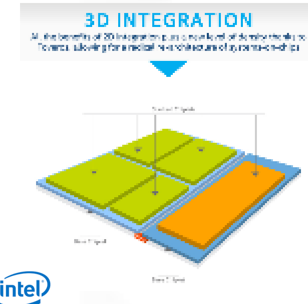
3x increase of federal investments in semiconductors

3D Heterogeneous Integration

Advanced Packaging Technology Transfer Success Story

STARnet

MTO

SRC	CHIPS	1st DARPA ERI Summit San Francisco, CA		
				
www.src.org (2016)	DARPA CHIPS Program Dan Green (Aug-17)	Intel ERI/CHIPs Update – CTO Mike Mayberry (Jul-18)	An Intel Breakthrough Rethinks How Chips Are Made (Dec-18) Intel's Interconnected Future: Combining Chiplets, EMIB, and Foveros (Apr-19)	Lakefield SoC in Galaxy Book S is first using 3D stacking and hybrid computing architecture (May-20)
Composable Customization for Assembly-Time Customization *SRC Liaison = Dan Green, DARPA MTO*	***CHIPS will develop design tools, integration standards, and IP blocks required to demonstrate modular electronic systems***	***Intel taking a leadership role to support the industry shift to heterogeneous integration***	***Lakefield is symbolic of the strategic shift in Intel's design and engineering model that underpins the company's future product roadmaps***	***Samsung Galaxy Book S is the first laptop with Intel's fascinating Lakefield chip***

MAPT Roadmap in the context of related roadmaps & road mapping activities

2018 BioElectronic Medicine Roadmap

UCLA/SEMI Roadmap

HETEROGENEOUS INTEGRATION ROADMAP

EES2 Roadmap

IMEC Roadmap

iNEMI Roadmap

2018 Semiconductor Synthetic Biology Roadmap

SRI Quantum Roadmap