Executive Summary

Second Nanotransistor Workshop:
Technology, Physics, and Simulation

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Organizing Committee

Dimitri Antoniadis	MIT
David Blackburn	NIST
George Bourianoff	Intel / SRC
James Hutchby	MARCO / SRC
Mark Lundstrom	Purdue

The Second Nanotransistor Workshop brought together a over 60 leading device researchers to examine the scaling limits of MOSFETs for applications in digital systems. It was designed to discuss critical research issues for nanoscale transistors and to identify strategies to address those issues. This Second Workshop focused on transistors at the 10nm scale and was a follow-up to the first workshop held at NIST in February 1999 that focussed on issues at 100nm dimensions. The specific objectives of the workshop were:

1) To discuss critical circuit, device, and process issues for scaling transistors to 10 nm dimensions and to identify promising new device structures.

2) To identify improvements needed in simulation tools so that simulation can contribute to scaling devices to their limits.

3) To discuss strategies so that circuit, system, process, and device researchers can collaborate in addressing the challenges of transistors at the 10 nm scale.

1. Summary of Presentations

The workshop brought together a heterogeneous group of experimentalists and computationalists and device physicists from academia, government and industry. The meeting opened with a session of presentations designed to identify issues for 10nm scale transistors from a variety of perspectives. It was followed by an afternoon session in which various approaches were examined. The remaining one-half day of the workshop was devoted to discussion and debate. To encourage open discussion and debate and the presentation of preliminary results and speculations, the proceedings of this workshop will not be published. However, a CD will be prepared and distributed to the Workshop participants. The purpose of this Executive Summary is to convey the spirit and overall conclusions of the meeting to the broader device community.

The Workshop formal presentations together with the participants' energetic discussions conveyed a guarded optimism that major challenges will be overcome and that scaling of CMOS may reach the 22-nm node for which the effective channel length would be 9 – 10-nm. This is a very significant change in perspective from the First Nano-Transistor Workshop held in February, 1999. The most important challenges include:

1. Power Management to limit total power dissipation
2. Judicious and very limited use of very leaky, high-performance transistors to limit their contribution to total chip power dissipation.
3. Control of the variability of the transistor's physical characteristics to control σV_{th}

Addressing these challenges will require an increasingly close cooperation between process and device engineers on the one hand and circuits and systems designers on the other. To establish a context for the conclusions of the discussion groups, a very brief summary of the formal presentation follows.

Session 1: "Issues for 10nm Si Technology," consisted of six presentations from diverse perspectives. Borivoje Nikolic (UCB) began by presenting a view from circuit and system designers identifying device variations and the need for multiple V_T's as critical issues along with the requirement that new device approaches minimize changes to the circuit and system design process. At the 10nm scale, chips will contain a relatively small logic core with large, on-chip cache, and systems on a chip a chip (SOC) will require analog and RF devices as well as digital switches. M. Alam (Agere) continued by examining the challenges of gate oxide scaling noting that the limit will be determined by leakage, reliability, and mobility degradation. NMOS is likely to scale indefinitely without reliability problems, but PMOS reliability may become an issue. Given the constraints and what is now known, an oxide scaling limit of ~1.1nm (physical) is projected. High-K replacements are still problematical because of reliability and mobility concerns. Carl Osburn (NCSU) examined issues from a process perspective using the 2016 node of the ITRS as a framework for discussion. He summarized the key problems as contact resistivity, compatible integration with thermally unstable gate stacks, and the need for selective deposition of junctions and contacts. The next speaker, Dimitri Antoniadis (MIT), examined the device issue of maintaining adequate on current at acceptable DIBL. He noted that series resistance is a critical issue and that mobility continues to be important, even at nanoscale dimensions. Antoniadis also observed that devices continue to operate well below the ballistic limit and will likely continue to do so – even at the 10nm scale. Konstantin Likharev (SUNY) proceeded to the ballistic limit and examined the issues for ballistic MOSFETs. He presented calculations showing that ballistic MOSFETs continue to have the gain necessary for logic all the way to 4nm, but that power scaling becomes a serious issue (with power actually increasing as V_{DD} is decreased due to exponential increases in leakage). Session 1 concluded with Bob Dutton's (Stanford) overview of the modeling and simulation approaches available to examine device issues at the 10nm scale. He discussed the existing semiclassical (particle based) approaches and the complementary quantum (wave-based) approaches and how they support each other in providing the device researcher with the tools needed for device design at the nanoscale. Several examples illustrated the significance of quantum effects in nanoscale MOSFETs.

Session 2, which examined various device approaches, opened with a presentation by Dave Frank (IBM). Frank reviewed the device issues for scaling, then noted that a super high performance, L < 10nm MOSFET can be realized, but that its leakage and therefore its power

dissipation will limit its use to perhaps 1% of a future system. For future digital systems, and certainly for systems on a chip, a variety of devices will be necessary -- each one with its own scaling limit. Brian Doyle (Intel) presented the case for bulk CMOS to the end of the road. Reviewing the recent history of technology development along with Intel's and others' recent reports of 20nm research devices, leads to the conclusion that 20nm bulk devices will be manufacturable. The message was that alternative device geometries should continue to be explored, but that the limits of bulk CMOS have not yet been identified and that industry will certainly push bulk CMOS all the way to its limit – wherever that may be. Gerry Neudeck (Purdue) followed by discussing double gate MOSFETs, showing how self-aligned DG MOSFETs can be achieved by selective epitaxy. Jack Hergenrother (Agere) then discussed the vertical replacement gate (VRG) approach. The VRG approach produces devices with one channel length and without halos, but channel length control can be very tight. The vertical approach makes a cylindrical geometry, which is best from an electrostatic perspective, possible, and using thin Si and self-limiting oxidation, VRG technology could make an attractive platform for fully depleted devices. Jeff Bokor (Berkeley) followed with a discussion of the FINFET. The device offers compatibility with existing design tools, with the caveat that transistor "width" is scalable in fixed increments. Techniques for producing sub-lithographic dimensions were also described. Current research issues include series resistance, mobility, and V_T control. The Schottky barrier FET was then discussed by Jakub Kerdzierski (IBM). This device seeks to address the series resistance issue and the main challenge is identifying low-barrier, complementary, silicides, particularly for NMOS, that are process compatible. Sub-30 nm devices have been achieved, and double gate implementations could provide additional improvements. Session 2 concluded with Judy Hoyt's discussion of the role of new materials, specifically strained Si and SiGe. Biaxial tensile strain produces large (~1.6X) improvements in Si electron mobility and smaller improvements in hole mobility which translate into on-current improvements that should persist even to 10nm dimensions. Very high Ge content, even pure Ge, could be attractive from a channel transport perspective because of enhanced hole mobility.

2. Break-out Discussions

The purpose of the workshop was discussion and debate, much of which took place during the presentations on the first day. During the morning of the second day, the participants were divided into four groups with directions to:

1) Identify three top scaling challenges.
2) Identify three opportunities to address those challenges.
3) Clarify the challenges for modeling and simulation.
4) Identify other issues that should be highlighted.

There was some discussion as to whether these questions were too narrow. The concern was that SOC issues were much broader than simply scaling digital devices to the limit. Some groups chose to address these broader issues and reported them under item 4). Appendix 1 contains a summary of each break-out group's report.

Question 3), Modeling and Simulation, was the focus of the first workshop. The conclusions from that workshop are listed in Appendix 2. The break-out groups were not asked to re-examine those broad conclusions, which have guided the SRC's modeling and simulation research program, but they were asked to identify specific challenges for modeling and simulation at the 10 nm scale.

3. Overall Conclusions

The reports of the four independent breakout groups indicate that there is a broad consensus on the challenges and opportunities for silicon transistors at the 10-nm scale. This broad consensus, which will provide a framework for the plans and activities of the Semiconductor Research Corporation and the MARCO FOCUS Center on Materials, Devices, and Structures is briefly summarized here.

With regard to the challenges at the 10nm scale, a number of issues surfaced with each group. Among these are the need to provide a variety of devices on a single chip – even for solely digital applications. Providing these devices in the face of increasing device-to-device variations will be a key challenge. The limits of oxide scaling are very near, and promising high-K replacement have still not been identified. If gate oxide scaling stops, new device structures may be needed to continue scaling. Series resistance is an increasingly difficult challenge as device resistances scale towards zero. Metrology for nanoscale devices was identified as a key challenge. TEMs are common but expensive and time-consuming and do not address critical doping profiles. Fundamental questions arise as to what oxide thickness or junction grading means at these dimensions (along with the question of how they can be measured).

Along with these serious challenges, the participants identified promising opportunities. In the first category are new opportunities such as self-assembly and self-limited processes, continuously tunable V_T's, and subthreshold swings less that 60 mV/decade. Original thinking along these lines could provide the electronics community with fresh research directions. In a second category is recently reported work that holds special promise. Enhanced mobility materials (strained Si and SiGe) are one example. Alternatives to the bulk CMOS transistors are opportunities that should continue to be explored but the continuing vigorous scaling of the bulk MOSFET sharpens the questions for alternative devices. The advantages of new device structures for ultimate scaling should be established, but broader device metrics should also be examined (e.g. device flexibility, device manufacturabilty, and sensitivity to variations). Research to explore the possibilities of increasing the functionality of a single device should be explored. (The use of a four-layer device to achieve a one-transistor SRAM cell is one example of what has already been achieved.) Finally, there was a consensus that problems at the 10nm scale will increasing involve device, circuit, and system trade-offs and that meaningful collaborations between device technologists and systems designers may provide new opportunities.

Modeling and simulation has an important role to plan in addressing the challenges at the end of the roadmap, and a number of simulation issues were identified. The distinction between materials, process, and device modeling is blurring as device simulations seek to deal with atomic scale structure. To address issues at the scaling limits, simulations will have to span the scale from atoms to systems. The challenges of dealing with the different scales involved (atomic scale materials modeling to the system scale for ECAD) will have to be bridged. The digital core will be a shrinking part of future SOCs, so a broader class of devices and issues will have to be addressed (e.g. digital, analog, RF, sensors, carrier transport, heat transport, noise, and high frequency). Opportunities to couple modeling with metrology will be essential to close the loop in modeling but may also improve metrology itself. In the process of developing tools and addressing problems at the 10 nm scale, a number of challenging problems remain (e.g.

understanding inversion layer mobility and ohmic contacts at the atomic scale and boundary conditions for nanoscale contacts).

4. Follow-up

The organizers thank the workshop participants who provided generously their time and expertise, which made the workshop a success. The Semiconductor Research Corporation and the MARCO Focus Center for Materials, Structures, and Devices both intend to use the conclusion of this meeting as input to their own planning processes. In addition one very specific follow-up action has already been initiated. Because of the success of the "well-tempered" 25 nm MOSFET (a device designed by Dimitri Antoniadis' group in response to the first workshop), there were similar requests after this workshop for "well-tempered" 10 nm designs. The intent is to use these designs to compare device approaches and simulation tools and to engage the design community in exploring new device approaches. Dimitri Antoniadis and Mark Lundstrom have initiated work to develop such designs and to make them available to the device community.

Appendix 1: Summary of the Breakout Group Reports

Group 1: Bob Dutton Reporting

1 and 2) Challenges and Opportunities:

- New devices and materials to address SOC issues.
  For example, high-speed and low power, analog, RF, noise, memory, need for redundancy in digital systems.

- Large numbers of transistor
  An opportunity for SOC, but a challenge for power and fluctuations. Device variations lead to a need for redundancy and drive some major issues in metrology and simulation.

- Self-assembly and self-limited processes
  An opportunity at nanoscale dimensions.

- Metrology
  Microscopic and atomic scale effects are becoming more important, but tools to characterize devices at this scale are lacking. Fundamental methods are needed for understanding, but "just enough" methods are needed for manufacturing. A new effort in physical experiments and characterization is needed to re-evaluate the experimental databases for the nanoscale. Metrology is needed for closing the loop with simulation and to provide constraints on models.

3) Modeling and Simulation

- Modeling tells us what is worth doing, but the devil is in the details.

- Modeling and simulation must deal with several philosophical divides. For example, the split between circuits (ECAD) and devices (TCAD), between deep physical models by those who seek to understand and experimentalists who march to a different drummer seeking direction in fast-paced technology development. These communities need to better understand each other in order to get full synergy.

- Modeling should be driven by new, innovative experiments.

- Computational materials at the atomic scale offers an opportunity to explore limits and alternative device directions.

4) Other Issues that should be highlighted

This group highlighted systems applications as the key issue driving device development. Systems and SOCs are supported by a manufacturing base, which provides inputs to ECAD tools. The manufacturing base is supported by a TCAD modeling and simulation and experimental base that provides a capability for

technology development. Another view of these levels was presented as a "science – engineering – manufacturing" triangle. Science provides the physical understanding and the metrology that gives closure to simulation. Engineering provides device design and TCAD tools to predict device, material, and process performance and robustness. Manufacturing uses these inputs in ECAD tools to design systems, establish manufacturability, and identify show-stoppers. The "hooks" between different levels have to be there so that system "care abouts" can be traced back to the manufacturing and physical levels.

Group 2: Krishna Saraswat Reporting

1) Challenges:

The group examined a long list of challenges and identified the three top challenges as:

- The need for a variety of transistors (with different V_T's, oxide thicknesses) and the challenge of providing them given the increasing importance of device-to-device variations.

- Oxide scaling, the serious challenges of high-K replacements (reliability, mobility, and leakage) and the need for alternative device structures if (when) oxide scaling ceases.

- Series resistance, which will be increasingly difficult to handle as device resistances scale towards zero.

- Metrology at the nanoscale.

  Among the other issues discussed were: off-current, gate leakage, on-current, power, maintaining compatibility with design automation tools, inversion layer mobility – especially with high-K, statistical metrology, and the metal-semiconductor interface.

2) Opportunities

- Alternative MOS device structures (double-gate, Schottky S/D, etc.)
  This group called for realistic comparisons of conventional, bulk CMOS to new device structures the purpose being to understand in a broad context what alternative devices may offer not only in providing an extra generation (or two?) of scaling, but also in terms of other device and system metrics such as device variability and manufacturability.

- High mobility materials (strained Si all the way to pure Ge)

- Better connection to circuit designers (because technology development will increasingly be driven by system design and trade-off issues).

3) Modeling and Simulation

- Device performance modeling should be tightly linked with computational materials science so that alternative materials and structures can be explored. The basic physical understanding of inversion layer mobility and its relation to the nanostucture of the interface and the physics of ultra-thin oxides could also be between explored by coupling these two disciplines.

- The metal-semiconductor interface poses a number of challenges. Multi-dimensional tunneling simulations that treat the interface rigorously are needed to design ohmic contacts and devices (e.g. Schottky S/D FETs).

- Simple compact models would be useful so that technologists and circuit designers can communicate and explore circuit and system issues at an early stage of technology development.

Group 3: Mark Law Reporting

1) Challenges:

After discussing issues and questions, this group identified the three top challenges as:

- Lithography

- Manufacturing variations

- Power management

2) Opportunities

- Alternative device structures (double-gate, ultra-thin-body, Schottky barrier, but process integration issues need to be addressed as well.
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- Mobility-enhanced materials (strained Si all the way to pure Ge)

- Higher levels of functionality (for example, replacing the 6T SRAM with a 1T SRAM)

- Working with the design community to exploit new device functionality.

3) Modeling and Simulation

- Device and process modeling should better address the alternative devices that SOC's will need (analog, RF, memory, etc.)

- Temperature distributions need to be coupled to device simulations (phonons and electrons need to be coupled).

- Boundary conditions especially contact to small devices) need to be carefully examined (an issue raised by Paul Solomon during the first day's discussion).

- Noise margins and noise modeling will be increasingly important.

- Process modeling and the need to calibrate process models will be increasingly challenging at the nanoscale.

4) Other Issues that should be highlighted

As a background for the discussion that resulted in the conclusions listed above, this group first discussed the following general issues and challenges:

a) What applications currently (will) drive device development?
(high-performance, memory, RF, analog (and the need for bipolar and BiCMOS, low-power logic, sensors, etc.)

b) How can the design community be engaged in the technology development effort?

c) Should device development focus on those devices with the greatest degree of freedom (in terms of V_T, L_G, etc.)

d) Which device type has the least sensitivity to process variations?

e) Scaling drivers is a known path, but what will drive device functionality in the future? What will be the market drivers?

Finally, this group identified the continuing scalability of bulk CMOS and the optimism of those doing it as the surprise of the workshop. It appears that "brick walls" should be taken with a grain of salt.

Group 4: Judy Hoyt Reporting

1) Challenges:

- Power

- Device variability

- Performance in terms of Ion/Ioff

- The increasing need for a wide variety of devices on a chip

2) Opportunities

These were divided into new opportunities (i.e., we have no idea how to accomplish these)

- Self-limiting processes.
- Tunable gate workfunction technology and electrically variable V_T.
- Beyond 60 mV/decade. Devising a new device that beats the thermal injection limit for sub-threshold swing.
- Working with the design community to exploit new device functionality.

And work underway that is showing good promise:

- Alternative device structures.
- Mobility enhancement (e.g. via new materials, strained materials, but, perhaps in other ways too).

3) Modeling and Simulation

- The challenges of modeling statistical variations in 3D.
- There is a need to model stress and its effect on electrical performance.
- ab initio materials models can be useful in exploring new materials.
- The possibility of using modeling to enhance metrology should be explored.
- Advanced simulation tools need to be easy to use.
- Thermal modeling is becoming essential.
- Noise modeling will become increasingly important.

4) Other Issues that should be highlighted

The device community needs to begin addressing a number of issues that have not been high priority:

- Does high performance continue to drive device technology?
- How can the device variety that SOCs will demand be provided?

- How do we get circuit and device people to communicate?
- What does device design have to say about yield?

Appendix 2: Modeling and Simulation Conclusions from the Feb. 1999 Workshop

1) **Future device simulation must address a broader range of problems.**
   Future device simulations should deal directly with atomic scale structure, fluctuations, and discrete charge effects. Efforts to treat reliability by simulation should also be explored. Tunneling through oxides and from band-to-band is increasingly important, and contacts are becoming an integral part of the device and should be dealt with directly. Other effects can be catalogued; the real issue is identifying the critical problems and addressing them by simulation promptly, so that the results can guide technology development.

2) **Computational electronics should emphasize problem-solving and invention.**
   Building simulation tools and matching measured data should not be the sole emphasis. Identifying and solving important problems, inventing devices, proposing experiments, etc. should receive more emphasis. The product of such research will be a solution to a problem, a deeper understanding of an issue, a proof-of-concept for a new idea, or a proposal for new experiments, rather than solely the development of a software tool. New software tools and numerical algorithms continue to be needed, but broader metrics for success are needed.

3) **Computational electronics must work more closely with experimentalists.**
   Working more closely with experimentalists will help focus work on important problems and provide the data needed to test models. Development of a significant new tool or numerical method is often the by-product of solving an important problem. This issue is more difficult for universities to address than for industry, but it is an important one.

4) **Simulations should capture quantum and atomic scale effects.**
   "Well-tempered MOSFETs" should continue to operate in an essentially classical (i.e. non-quantum) manner for some time, but to comprehend atomic scale effects, fluctuations, reliability, etc., full quantum simulation tools are essential. They are needed to understand the detrimental effects of atomic scale fluctuations and to interface to atomic scale process models. More importantly, answers to the critical long-term issues may lie in learning to engineer electronic devices on an atomic scale, and simulations may help us understand how to. This work is still at the frontier; no roadmap is possible; many approaches and issues need to be explored and understood.

5) **Current tools must evolve and new tools may be necessary.**
   Since problems are addressed by the simplest technique that captures the relevant physics, a range of tools will continue to be necessary. Existing tools should continue to be developed and extended as should efforts to understand each tool's role and limitations. New tools may be needed, but beyond the NTRS, it is not clear what the right tools are or what new tools are needed. Investments should be made so that there are options to choose from. Ways to bridge the gap between the capabilities of the latest research codes, often developed at universities, and those available from vendors should be explored. Detailed tools should act as a "laboratory" for the development of new phenomenological models, including new compact models based on sound physics for nanotransistors.

6) **Techniques for speeding new code development should be broadly applied.**
   The development of new simulation tools is a slow process requiring many person-years of effort, but the pace of technology development is quickening. The use of problem-solving

environments, off-the-shelf components, scripting approaches, and modern programming methodologies should be accelerated. Codes can be shared better and existing codes may be adapted to new problems. Universities can still address significant computational problems, but it is unrealistic to expect the resulting codes to have industrial-strength in terms of user interfaces, visualization, robustness, etc. The problem solved or understood, the device invented, or the approach or algorithm demonstrated should be regarded as the primary research product and the software tool as a proof-of-concept demonstration.