

SRC Post-RTL Design CAD Research Needs - A 2002 Update

Short History of SRC “Top PD Problems”

- **ISPD 1997: “Top 10 PD Problems”** presented by Naveed Sherwani
 - Developed by group of professors and industry leaders
 - **1999: SRC drafted a “Research needs for physical design CAD” document.**
 - **1999: SRC PD task force identified SRC “Top 10 PD” problems.**
 - Problems where research is behind industry needs.
 - Presented at ISPD '99 and DAC '99
 - **ICCAD 1999: EDA firms asked to provide their top ten list**
 - **April 2000: SRC invited EDA, academia, and industry to provide their *bottom ten list* of problems.**
 - **Spring 2002: SRC task force updates PD CAD Needs document**
 - Updated document completed by task force in April 2002
 - Not yet officially released.
 - To be published in August
 - **Guides researchers to critical needs in physical design CAD.**
 - **For researchers seeking SRC funds: Updated view of research needs.**
 - **For rest of us: Assessment of PD CAD issues the industry faces.**
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Design CAD Needs - Drivers

Physical design CAD needs driven by constant goals (cost, value) and change factors:

Drivers	Goals/Issues	Change Factors
Manufacturing Cost	Minimize die area, obtain highest yield, reduce test cost.	Subwavelength lithography (OPC/PSM).
Integration	Integrate more transistors and diverse logic types on chip	Embedded DRAM, mixed-signal, system-on-chip (SoC) design.
Performance	Attain best chip and system performance.	Interconnect dominates global DSM delays, SOI, advanced clocking.
Power Dissipation	Minimize static and dynamic power.	Multi-threshold (Vt) processes, SOI, dynamic chip power management.
Quality	Improve system quality and reliability.	Rising test costs vs. overall chip fab cost , process variations, BIST.
Design Cycle-time and effort	Reduce TTM and design cost for new IC designs and incremental redesigns.	Tighter integration of physical design and synthesis.

The Underlying change driver ... Moore's Law

On to 90 nm and below!

Design CAD Research Needs

SRC Top Needs in Physical Design CAD Research

Scope

- **Physical Design CAD: Algorithms for silicon implementation**
 - Place and route, design planning, etc.
- **Covers (parts of) synthesis, timing analysis and verification**
- *What new research is required to address these needs?*

Focus

- **Timeframe: CAD Research for next 4 - 7 years**
- **New list extends beyond traditional digital design**
 - Many references to mixed signal and analog designs.
 - SOC more prominent
- **Tries not to specify solutions or narrow scope**

Top Needs - Categories

Placement and Routing:

- Placement and routing solutions that consider different circuit families and broader design goals

Key issues:

- Size/capacity: Place and route solution for thousands of large blocks and millions of small blocks in a reasonable time
- Optimize for reliability, performance, signal integrity, & power density
- Handle analog circuits, SoCs, multiple circuit family interactions, etc.
- OPC and PSM constraints

Synthesis and Layout Integration:

- Synthesis/P&R flows that converge to a solution efficiently.

Key issues:

- Optimize for routability at the logic synthesis level.
- Synthesis/P&R operations that preserve locality of changes.
- Account for presence of manufacturing variations.
- Parameterized libraries and tools that can use them.
 - synthesis that automates custom design (e.g. transistor-level synthesis).

Prashant Saxena Intel Corporation

**High Level Planning and Integration
Power Distribution Design and Analysis
Timing Analysis and Verification
Research Directions in CBC**

Top Needs - Categories

High Level Planning and Estimation:

- **Front-end algorithms that analyze features of a design and concurrently optimize (area/delay/SI/power/hot spots).**

Key issues:

- Wire planning, latency planning.
- Predict physical and performance metrics of a block before implementing a synthesis and layout step.
- Integrated data models and consistent metrics across the design/verification flow. Fidelity.
- Behavioral parsing

Power Distribution Design and Analysis:

- **Power grid solutions that satisfy power delivery and dissipation requirements while ensuring reliability.**

Key issues:

- Optimize power network for noise, power, and quality/reliability.
- Co-opt with signal distribution (clock nets, critical global nets),
- Grid modeling aware of package design, manufacturing variability, inductance.
- Early design analysis of power grid impact on system performance.
 - Better block power consumption models
- Isolation and decoupling technologies.

Top Needs -Categories

Timing Analysis and Verification:

- **Accurate timing analysis in the presence of process and statistical variations (power grid variations, temperature, noise).**

Key issues:

- **SOI, emerging circuits, transparency, false paths, MIS**
- **Analog design**
- **Combined synchronous/asynchronous clocking schemes.**
- **Timing analysis/verification during and after layout phases.**
 - **Better wire delay models**
 - **Silicon correlation**

Research Directions in Correct by Construction Design

- **Circuit, synthesis and layout solutions to enable predictable correct-by-construction design that avoids iterations.**
 - **Motivation: Optimization-verification iterations are expensive in terms of design time. Break loops by designing to specs rather optimality.**
 - **Analogy: Can we have a DSM simplified flow like traditional ASIC flow?**

Roberto Suaya Mentor Graphics

**Clocking Design and Analysis above 15GHz
Interconnect Synthesis and Analysis**

Top Needs - Categories

Clocking Design and Analysis above 15GHz:

- Synthesis of a clock tree based on prescribed skews at latches

Key issues:

- Enabling techniques: cycle stealing; power reduction; ECO.
- Comprehend process and manufacturing variations.
- Alternatives to a globally synchronous methodology.

Interconnect Synthesis and Analysis:

- Intra-chip communication synthesis

Key issues:

- Algorithms that understand simultaneous: wire sizing, routing, signal isolation/shielding, gate sizing, repeater insertion, cell placement.
- Exploration of bus structure characteristics and topologies.
- Simultaneous synthesis of multiple interconnects (vs. net ordering).
- Incorporate impact of wire design on noise and timing with variable accuracy, on-the-fly RLC extraction and analysis.

Dale Edwards AMD/SRC

Design and Verification of mixed signal designs

What are the needs for MS?

High level planning and estimation for MS SoCs

Synthesis of analog blocks with consideration for

- Symmetry/parameter variability
- Design tradeoffs such as power/performance
- Efficient interface to other SoC blocks
- Passive components
- Design scalability

Placement and Routing to handle

- Creation of analog IP blocks
- Incorporating analog IP blocks in SoCs
- Noise concerns of analog
- Power and thermal concerns of analog
- Analog BIST

What are the needs for MS? (cont'd)

Verification tools comprehending analog design constraints

- **Accurate parasitic extraction for mixed-signal and RF**
- **Noise**
- **manufacturing variabilities**
- **isolation**
- **thermal, etc.**

Technology issues

- **Tools that take into account analog circuitry needs such as effects of post tape out metal fills**
- **Tools that handle BiCMOS and possibly other technologies**

Top Needs -Categories

Design and Verification of mixed signal designs

- Physical design solutions for mixed signal designs

Key Issues:

- Verification of mixed signal design
- Interactions and requirements of digital and analog interfaces
- Incorporate analog design constraints - noise awareness, substrate coupling, parasitics, etc.

Patrick McGuinness Motorola

**Design for embedded SOC
Optimization and Analysis for Power**

Top Needs -Categories

Design for embedded System On Chip

- **Solutions that address physical design needs of complex SoCs.**

Key Issues:

- **Floorplanning and chip integration algorithms for SoC mixed-block designs. Timing analysis supporting mixed types of circuits.**
- **Algorithms and techniques to support IP reuse, characterization and verification for SoCs**
- **Data management and frameworks to support large and complex SoC chip design and integration.**

Top Needs -Categories

Optimization and Analysis for Power

Motivation: Power is becoming a dominant factor in many designs.

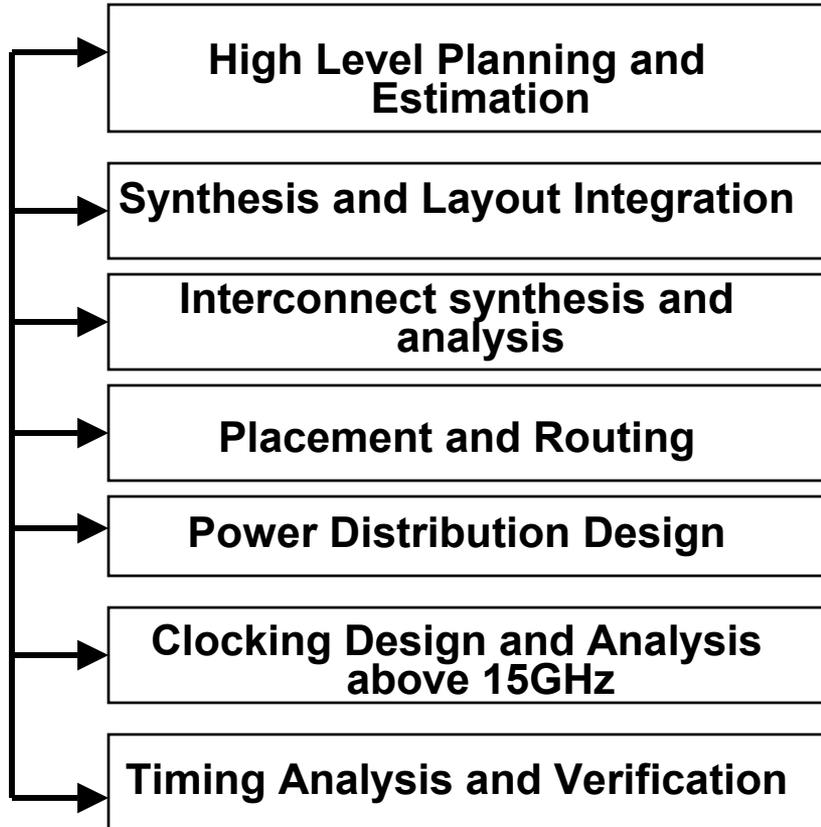
Sacrifices to timing or area may be needed to meet power requirements.

Key Issues:

- **Make power a primary optimization target**
 - Power reduction part of objective function.
 - Sometimes timing and area are secondary objective functions behind power.
- **Power characterization and modeling for power for IP cores**
- **Power characteristics of analog design**
- **Early power estimation that considers physical design effects**
- **Support low-power design and circuit techniques in PD algorithms:**
 - Gated and/or skewed clocks
 - Asynchronous design
 - Multiple-Vt, and multiple or variable VDD implementations.
- **Consider power density and thermal effects**
- **Leakage**

Top Design CAD Research Needs - Summary

Aspects of Design Flow



Not a Linear Flow !!!

New Methodologies

- Correct by Construction Design

Design Types/Styles

- Design and verification of mixed signal designs
- Design for embedded System On Chip

Design Optimization Targets

- Optimization and Analysis for Power

Cross-cutting issues:

- Process variations
- SoC/mixed-signal
- manufacturability/quality
- OPC/PSM, SOI

Design Driver

- SOC: “Not just digital”

Conclusion

Big Picture :

- **Moore's Law Lives! ... getting to "nano-scale"**
- **Physical Design Is Electrical Behavior Design**
 - **Effects we could ignore earlier now are important**
Example: "Routing" -> "Interconnect Planning & synthesis"
- **IC Value Added Is The System We Can Build With It**

Need to push PD CAD envelope to create Systems of the Future!