SRC-NSF Mixed-Signal Workshop
May 16-17, 2002

Executive Summary

Mixed-signal technology is a rapidly expanding field that is struggling with important technical issues crossing the traditional discipline boundaries of CAD Tools, Design, Devices and Packaging. Top researchers in mixed-signal design and technology from industry and academia outlined critical cross-disciplinary needs at the first annual SRC-NSF Mixed-Signal Workshop held May 16-17, 2002, in Orlando, Florida, in conjunction with the Custom Integrated Circuits Conference. The purpose of this Workshop was to explore and identify major technical needs and issues related to development of mixed-signal products, with a particular focus on issues spanning the traditional disciplinary boundaries. The major questions addressed at the workshop included:

- Are there critical needs that are not being funded?
- How can mixed-signal research efforts reach across traditional tool-system-circuit-device-packaging boundaries?
- What continuing unmet mixed-signal research needs spanning these disciplines should be highlighted?

The workshop attendees developed an extensive list of issues. The most critical issues were as follows:

- Leakage in scaled CMOS, a critical issue for all analog and digital technologies
- Bifurcation of technology requirements for digital and analog/RF devices with scaling
- CAD tools and modeling for advanced technologies and design methodologies

Over the next two months, the SRC staff who participated in the workshop, along with representative workshop attendees, will meet to discuss and prioritize needs identified in the workshop. We will also reconstitute the Mixed-Signal Task Force who generated the 2001 Research Needs Document for Mixed-Signal, and publish a revised 2002 edition. We will then formulate a plan to put research in place to address these needs.

Summary of Issues Discussed

Increased leakage currents that are currently anticipated for future CMOS were a major concern. A great number of mixed-signal designs rely on charged-based circuits, which rely on storage of a charge for a period of time. Leakage currents force increased power dissipation in such circuits in order to maintain accuracy. Such circuits perform poorly or not at all in the presence of leakage, and leakage is expected to be severe in future CMOS; gate leakage is arguably the greatest threat, as there are no known solutions. Subthreshold leakage and junction leakage are additional problems for analog charge-based circuits. These leakages are a problem for digital circuits as well, as chip power is expected to increase to unmanageable levels. Some other effects that are expected for analog as we scale CMOS are lower gains, poorer settling times, limited dynamic range (due to kT/C and lower V_{dd}), and increased noise. Voltage scaling increases power dissipation for high-speed high resolution circuits at a given technology node.

Traditionally, designers have "designed around" many of the process issues. For example, as L_{eff} scales, analog designers have used longer drawn channel lengths to control device mismatch due to variability. As V_{dd} decreases, analog designers have invented folded cascode amplifiers to handle the situation. Digital designers have used multi-threshold devices to trade off performance with power or adding repeaters to improve signal speeds. As the technologies shrink allowing

many more transistors, designers can no longer cope with making these "design arounds" by hand. Future designs will require new CAD tools to handle these tasks. EMI is a big issue with SoCs – we need better, more efficient, more robust CAD tools in this area including EMI driven Place and Route.

Future scaled processes present new problems for RF circuits in addition to those discussed above. Tank circuits will exhibit nonlinearities due to low breakdown voltages of devices. Good varactors will be more difficult to design due to leakages. Noise in NMOS devices will increase, as will resistor noise due to more resistive interconnects contacts and devices. Digital noise coupling into RF will continue to be a problem. We must invent improved materials to build better integrated passive components. Porous Silicon may offer better performance for passives (lower loss). Are passives more effective in Systems in Package (SIP)? Although passive capabilities on wafer are improving, excellent substrate passive components are already available for SIP. SIPs may be a better solution for Power Amplifiers, as power added efficiency is an issue when fully integrated. RF circuits need better isolation, and even SOI technologies may not provide enough isolation.

Better modeling will be required in all areas , includingbetter modeling for ESD, especially for RF circuits. Better RLC model extraction including transmission lines is required. For SiGe, noise and linearity and the effects of the profiles, processing limits, and trap quantization must be studied and modeled. Will popcorn noise return? (don't need it again!). Good substrate noise modeling is required. Will models ever capture a good analog designer's "gut feel"? Transmission line models must become real elements in circuit simulators and model libraries. Better tools are needed to automatically generate models rapidly. We will need ways to better model and simulate signal integrity, jitter, and clock skews.

We must continue to study better design techniques for high performance processing, *e.g.*. 16 bit Analog to Digital Converters. We must think about systems first – what are the system tradeoffs between analog and digital? A good rule of thumb is "do it in digital if possible".

Manufacturing issues abound. Given the very high cost of reticles for advanced processes, how can we design for first pass success (not usually possible with Mixed Signal)? Special metal coverage rules (especially post tape-out fill) must be modeled in order for analog to work properly. Which is the most cost-effective solution – SoC or SIP? How can we design analog/RF circuits that will allow Intellectual Property blocks to scale to the next node; is it even possible? Will integrated passives scale? Will new materials in processing have a negative impact on circuit performance? How can we achieve rapid yield ramp? How are we going to design for test? How can we accelerate testing to guarantee acceptable Bit Error Rate? Is hierarchical Built-in Self Test a viable approach for Mixed Signal? How can we lower the test cost by testing components prior to SIP assembly? We will need new efficient bus signaling schemes to handle high pin counts: pseudo differential, incremental signaling, etc.

Summary of Key Issues and Areas of Concern for Mixed Signal

1. Leakage: Gate leakage, junction leakage, and subthreshold leakage
2. V_{dd} scaling
3. Isolation
4. Variability
5. Noise

6. Capacitive resistors
7. Model accuracy
8. CAD tools
9. Mixed Signal Test
10. Low intrinsic gain – (g_m x r_o)
11. Costs: Mask and wafer cost (especially since analog usually requires a second pass), System integration costs, Test costs
12. Mixed Signal IP scaling

Ten Specific Recommendations

1. Sponsor device research projects to address high gate leakage, low gain, subthreshhold leakage and other technology problems mentioned at the workshop. Sponsor circuit design and modeling research to perform physical measurements, develop models, and implement prototype circuits using new devices and technologies.
2. Develop compact models to capture the results learned from the measurements of the devices. Develop forward-looking compact models for designers to do predictive work and do design tradeoffs for MS.
3. Explore revolutionary approaches to improve performance without increasing power
4. Increase research in the package and SIP area for Mixed Signal and RF, including chip-package co-design, thermal management, ESD protection and better overall modeling.
5. Continue system (application) driven circuit design projects. These projects will develop new circuit techniques which have broad application. Mixed-signal design problems are difficult, and will require very talented engineers. Create research programs to attract the very best and brightest students. Make known what we want students to learn (curriculum).
6. Sponsor circuit design projects that require use of the most advanced technology, to uncover new problems and develop innovative solutions.
7. In all Mixed Signal research, emphasize cost effective solutions – both development and manufacturing cost.
8. Develop programs which permit academia to work closer with industry on key mixed signal issues, permitting researchers access to leading edge technologies and libraries at low cost. Increase internships and liaison programs. Figure out how to lower the cost to use MOSIS.
9. Have follow-on workshops within the coming year to focus on other key issues (in conjunction with DARPA, NSF, and MARCO).
10. Put more focus on Mixed Signal Technologies in the coming ITRS.

Background Information

In the spring of 2001, the National Science Foundation and the Semiconductor Research Corporation announced a $6 million joint initiative for innovative university research in mixed signal electronic design and technology, leading to the integration of analog and digital components into a systems on chip and on package with orders of magnitude improvement in performance, time-to-product, reduced power consumption and cost reduction. Proposals received spanned the anticipated range of areas, including system architecture, circuit design, CAD and test, advanced devices and technologies, packaging, interconnect, and passives. Sixteen proposals in these areas were selected for three-year joint funding by SRC and NSF. In

addition to these new tasks, SRC currently funds 63 other tasks at a level of approximately $10M over three years.

Now we ask ourselves these questions: Are there critical needs that are not being funded? How can mixed-signal research efforts reach across traditional tool-system-circuit-device-packaging boundaries? What continuing unmet mixed-signal research needs spanning these disciplines should be highlighted?

To help address these questions, we held a day and a half workshop in conjunction with the Custom Integrated Circuits Conference where mixed-signal experts from industry and university could discuss the issues. We targeted 60 participants and ended up with 65: 20 from 11 different industrial companies and 35 from 24 different universities along with 10 from SRC.

The focus of this first workshop was on interactions between design and device technologies, especially CMOS, since many millions of research dollars are currently directed towards advancing CMOS at a rapid rate. Will advanced CMOS nodes continue to be suitable to building mixed-signal circuits for anticipated applications? Since no one wants to entirely neglect the important needs in other areas, we set aside the last half-day to discuss the topics of CAD, test, packaging, and any other issues with the idea that follow-on workshops will focus on one or more of these important areas.

Both days were organized into focused sessions, consisting of talks by experts followed by panel discussions. The first day's talks were:

Analog and charge-based circuit design by Prof. Charles Sodini, MIT
High performance digital design by Shekar Borkar, Intel
RF design by Prof. Ken O, Univ of FL
SiGe HBT by Prof. John Cressler, Auburn
Substrate Coupling by Daniel Friedman, IBM
Advanced CMOS for MS by Prof. Bruce Wooley, Stanford
Optimizing CMOS for RF & Analog/Digital by Derchang Kau, Intel

On the second day:

Mixed Signal SOC/SIP Design and CAD Issues by Prof. Rob Rutenbar, CMU
Mixed Signal SOC/SIP Industry View of SOC/SIP Process/Manufacturing Issues by Paul Kempf, Jazz Semiconductor
Mixed Signal SOC/SIP Test Issues by Prof. Jacob Abraham, UT Austin

All presentations may be found on the SRC web siteat:

http://www.src.org/member/event/E002032_Results.asp