Request for Proposals for the Nanoelectronics Research Initiative (NERC RFP # S201006)

A. Background

The Nano Electronics Research Corporation (NERC) is soliciting proposals from US Institutions qualified to do research in areas of interest to the Nanoelectronics Research Initiative (NRI). NERC, a not-for-profit research management organization, makes this solicitation on behalf of NRI's collaboration with the National Institute for Standards and Technology (NIST). NERC is a wholly owned but separately managed subsidiary of the Semiconductor Research Corporation (SRC). SRC is a research management consortium that was established in 1982 and sponsors semiconductor research for its members.

As the ultimate limits to the scaling of CMOS (Complementary Metal Oxide Semiconductor) technology are getting closer, new approaches in emerging areas in electronics at the nanoscale need to be explored. NRI wants to focus the research and resources on specific beyond-CMOS device concepts that will extend the "emerging technologies" of the International Technology Roadmap for Semiconductors (ITRS) and to encourage the exploration of novel technology opportunities in order to help sustain the historical growth of the electronics industry. The on-going NRI collaboration with NIST is expected to stimulate research that will address long-range semiconductor research needs and identify new device technologies.

The NRI mission is to discover and demonstrate novel computing devices capable of replacing the CMOS FET as a logic switch in the 2020 timeframe.

- These devices should show significant advantage over ultimate FETs in power, performance, density, and/or cost to enable the semiconductor industry to extend the historical cost and performance trends for information technology.
- To meet these goals, NRI is focused primarily on research directed toward devices utilizing new computational state variables beyond electronic charge. In addition, NRI is interested in new interconnect technologies and novel circuits and architectures, including non-equilibrium systems, for exploiting these devices, as well as improved nanoscale thermal management and novel materials and fabrication methods for these structures and circuits.
- Finally, it is desirable that these technologies be capable of integrating with CMOS, to allow exploitation of their potentially complementary functionality in heterogeneous systems and to enable a smooth transition to a new scaling path.

A 1 - Research Areas of Interest

NRI is seeking to encourage research on topics with the potential for maintaining the historical scaling of both computational power and the cost of information processing. To define a well-directed program for new device research, SRC and NSF jointly organized a set of industry-academia-government workshops in 2003 and 2005. The workshops defined 13 research vectors that were felt to be essential to make progress in the search for the next switch beyond

ultimately-scaled CMOS. The first five of these vectors currently form the heart of the NRI research program:

- Computational state variables other than electronic charge
- Non-equilibrium systems
- Novel data transfer mechanisms
- Nanoscale phonon / thermal management
- Directed self assembly of new device structures

The next two research vectors in the list are so intricately linked with all five vectors, they have been interwoven directly into the research programs at all of the NRI centers and are expected to continue to play a key role:

- Modeling/Simulation
- Metrology/Characterization

In the nano-metrology area, proposers are encouraged to consider how collaboration with NIST could be beneficial for enabling characterization of materials and devices, particularly if it requires the discovery and development of potentially revolutionary measurement techniques and tools.

Phase 1.0 of NRI made strong progress in looking at many of these vectors and demonstrated the potential of several areas through experimental and simulation data. In Phase 1.5, NRI will focus on just the 8-10 most promising device areas by establishing teams for each device to look at every aspect from materials growth to fabrication and characterization, and from basic physics and simulation to device design and circuit implementation. Specifically, each center is expected to focus on 2-3 device technologies, with multi-PI and multi-university teams to cover all key areas of research as listed below to implement computation with that device.

- Novel materials development, growth, and characterization
- Specific work on self-assembly or other novel fabrication techniques, if necessary for device development
- Physics theory and experimental verification of key phenomena, including work on phonon / heat flow for novel cooling and/or non-equilibrium behavior
- Device modeling, design, fabrication and characterization
- Novel circuit & architecture work to take advantage of the unique device properties (e.g. non-volatility / built-in memory) for low-energy or energy-recovery during operation

Ideally, all proposals will have at least one PI working in each of these areas for each device technology being proposed. Of course in some cases, it may be more efficient to have a single PI working in one of these areas as part of more than one device team, either within a center or across centers, where his/her work can be used more broadly (e.g. a PI developing graphene growth or characterization processes may support several different graphene device efforts). Particular focus should be given to the planned circuit/architecture implementation for the device, i.e. how will this device actually perform computation and what will be the total speed, energy, and area of the base computational unit being proposed. While the focus should remain on finding a new logic device, consideration should also be given to the system as a whole, including integrated memory devices, interconnects, and communication.

Ideally the devices and circuits should be targeted to compete favorably with high performance CMOS for general purpose computation, but devices that perform well for specific application areas or on important algorithms or at ultra-low power will also be considered. Proposers are encouraged to consider the novel behavior of their devices and to look for circuits and application areas that exploit this behavior for maximum benefit. And for whatever application space is chosen, the focus should not only be on showing how the device/circuit can outperform CMOS at the end of its scaling roadmap, but also how the new device/technology can be expected to scale further. Here, scaling should be considered more broadly than simply continuing to double the number of physical devices on a chip each generation, but rather how to "double" the amount of computational performance on a chip in each generation, with particular concern given to how power will continue to scale as needed.

The primary outcome of these projects should be to produce sufficient data and understanding of each device area to enable conclusions on whether it could pose a viable option for extending scaling beyond the limits of CMOS. Ideal outcomes would be functional proof of concept demonstrations of computational technologies with significantly improved computation per unit power per unit area. Barring a full demonstration, a plan to have a strong set of data through experiment and simulation to support a device technology's ultimate capability is also important. The goal is to have the results of Phase 1.5 be sufficient for determining which one or two devices show the most promise for significantly larger investments in the future. Note that it is also expected that many of these devices may warrant further research – either in NRI or FCRP or other programs – due to their capabilities in related areas (e.g. memory), even if they do not look promising as pure logic device replacements. The Phase 1.5 results will also be used for making those decisions.

Proposers are encouraged to reference the NRI website (http://www.src.org) for additional information on the current NRI research centers and projects.

A 2 - Proposal Process

Based on this solicitation, approximately 4 centers are expected to be funded. The proposals will be reviewed by the NRI Technical Program Group, which comprises of senior researchers from the participating companies (AMD, GLOBALFOUNDRIES, IBM, Intel, Micron and TI) and NIST. In addition to financial support appropriate to pursuing mutual interests of the investigators and the NRI, there will be an opportunity to collaborate with industrial researchers from NRI participating companies and from NIST. The research results should be widely disseminated, and publication in technical journals and presentations at conferences will be encouraged. Participation by funded researchers in the NRI reviews and potentially at industry/government sponsored workshops and meetings is required. There is an annual review of the overall NRI program, as well as annual on-site reviews of each center and semi-annual reports submitted to NERC from each center. All publications, reports and review materials are to be posted on the NRI website.

Investigators should ensure that their proposals address the following essential attributes:

- A research plan which contains a compelling and well-articulated vision on how the center's work will result in key learning about specific device and/or circuit technologies that complement or support the NRI's research agenda described in Sec. A1. The proposer is expected to identify how the proposed research relates, if at all, to other on-going research in nanoelectronics.

- A list of clear milestones that will result in sufficient learning about the proposed technology to prove out its future potential as a logic switch or system that can scale beyond the expected limits of CMOS technology.
- A reasonable scope of research which can be realistically executable with available resources and in accordance with sound cost management.
- A description of the host institute's policy and history of successful industrial collaboration regarding the exchange of staff, recruiting of students, intellectual property agreements and previous successful collaborations with industrial partners.
- A statement addressing the availability of facilities and resources needed to help make the proposed project successful. This should include any plans for collaboration with NIST or other labs / institutes / NRI member companies for doing joint work, if appropriate.
- A statement addressing the plans for matching funds from university, state or federal sources to leverage the funds from NRI.

All NRI research will be funded through the NRI interdisciplinary, multi-university centers, and hence all proposers should contact the existing NRI centers to discuss their proposals: The Western Institute of Nanoelectronics (WIN) headquartered at UCLA in California; The Institute for Nanoelectronics Discovery and Exploration (INDEX) headquartered at SUNY-Albany in New York; The South West Academy for Nanoelectronics (SWAN) headquartered at UT – Austin in Texas; and The Midwest Institute for Nanoelectronics Discovery (MIND). As part of this RFP process, these centers are expected to put together new programs which focus on specific device areas and include the best set of projects, PIs, and universities possible. Proposers may contact the centers directly, or contact the NRI Director, Jeff Welser (jeff.welser@src.org) to facilitate this.

Evaluation and technical review of the proposals will be done by the NRI Technical Program Group, and the final decision on the awards will be made by the NRI Governing Council.

A 3 - Program Scope and Planned Funding Level

Project proposals are expected to be for a two year time period, with funding allocated on a yearly basis. All funding after the first year will be contingent upon successful performance, as evaluated by the NRI-NIST collaboration, and availability of funds. Several multi-university center awards could be made in the areas identified, with the average award expected to be from $750,000 - $1,250,000 per year per center. Following proposal selection, research agreements will be negotiated with awardees as appropriate, with the research expected to start in the first quarter of 2011. Any potential for additional funds from university, state or federal sources to match the NRI funds should be included in the proposal and will be considered in the review process. Not all areas of interest may necessarily be funded, and the titles of the broad areas of interest are not synonymous with the names of the current or planned research agendas, nor are there any implications that an area of interest cannot accommodate more than one research effort.

B. Proposals guidelines and schedules

B.1 Purpose, Format, Content and Length of Solicited Proposals

Solicitation Purpose and Process

In order to permit selection of the proposals most likely to advance the NRI research goals; proposals are being solicited from investigators to address the NRI agenda in Sec. A1.

The proposals are due electronically by 5:00 p.m. Eastern Standard Time at the Nano Electronics Research Corporation (NERC) on October 16, 2010. The process and address for submitting these proposals is described below.

Proposal Format, Content and Length

The proposal format is:

1. A cover sheet to include:
    a) NERC RFP number;
    b) Proposal title and center name;
    c) Investigator(s) name, address and contact information.
    d) Proposed institution(s) name, address and reference number (if any);
    e) Names and contact information of any industrial or governmental collaborators
    f) Proposed institute(s) administrative point of contact to include: salutation, last name, first name, street address, city, state, zip code, telephone, fax and electronic mail;
2. Table of Contents keyed to the page numbers of the proposal sections.
3. An Executive Summary, a one to two page description of the proposal and key features.
4. A Center Research Overview, a description of the center research objectives, themes, project portfolio, and structure, not to exceed 6 pages. This section should show the total planned center portfolio, structured around the specific 2-3 device concepts the center will pursue.
5. Statement of Work, to include a one page table of projects/PIs organized by device theme, followed by one-page description of each project including a description of the research, goals, fit to NRI objectives and to a specific device theme, and a timeline of key milestones.
6. High-level Budget broken down by theme and university for the funding period requested, including the matching funds from university, state, or federal sources. Note that if a proposal is selected for funding, a full detailed budget will be needed prior to contracting.
7. The availability of the resources necessary should be described in 500 words or less, including plans for receiving matching funds from university, state, or federal sources to leverage NRI funding.
8. The institute's plans for collaboration with industry and NIST should be described in 300 words or less.
9. Relevant publication record and references.

B.2 Proposal Submission Process and Related Information

Submission Process

Electronic submission of all proposals is required. Please submit PDF (preferred) files using Arial, Courier, Times Roman, or Helvetica fonts of 11-point size or larger. Send the PDF files as email attachments to the NRI Director, Jeff Welser (jeff.welser@src.org), and cc Allison Hilbert (allison.hilbert@src.org). Please address all questions to Jeff Welser by email.

Disclosure of Proprietary Information

All proprietary portions of proposals must be clearly marked. Restrictive notices notwithstanding, proposals may be handled and read for purposes of evaluation by NERC, NRI Participants, NIST officials and selected external reviewers.

Intellectual Property

NERC expects proposals to comply with the policies and procedures of NRI concerning Intellectual Property (IP). In return for sponsoring research, NERC receives a royalty-free, nonexclusive, worldwide license to intellectual property (including software, copyrights, patents, mask registrations). Universities own and are free to license this intellectual property to companies outside the NERC community. Certain IP rights will also have to be provided to NIST. NERC may be available as a resource, to assist awardees strategically and financially, as appropriate, to develop IP rights developed under their awards.

Blocking Background Intellectual Property

Blocking Background Intellectual Property (BIP) is defined as patents, patent applications, or computer software of any party that is required to practice the anticipated results of the research. NERC funds University research on the condition that NERC Member companies will have the freedom to practice the results of the research. The existence of Blocking BIP of any party can seriously impair or even block the ability of NERC Members to exercise this freedom to practice. Therefore it is important that NERC be informed as early as possible of the extent, if any, that the proposed research requires the use of Blocking BIP.

B.3 Evaluation Criteria and Selection and Award Process

Evaluation Criteria

The selection criteria used in the technical review of the proposals, in order of relative importance and priority, are:

1. Overall scientific and technical merit, including:
    a. Impact of the proposed work on the NRI research agenda
    b. Plan for producing data necessary to prove-out a new logic device technology
    c. Ultimate potential of the device areas being pursued
2. Ingenuity, novelty, and feasibility of the proposal.
3. Investigator(s) capabilities and related relevant experience.
4. Access to the needed personnel, resources, facilities, equipment, and data to perform the work.
5. The potential for leveraging NRI funds with university, state, and federal funds.
6. Quality of the industrial and/or NIST collaboration plan.
7. Intellectual property issues and policies which may preclude timely execution of the contract.

Selection and Award Process

Proposals will be evaluated by a Proposal Evaluation and Selection Committee, comprised of a group of senior researchers from NRI participating companies and NIST. The proposer will be notified of selection or non-selection in a timely manner.

All non-selected proposals will be destroyed, except one copy which may be retained for file purposes, unless the applicant has requested that the proposal be made available for consideration of alternate funding by other NRI participating company funding instruments.

Not all proposals submitted in response to the invitation by NERC and selected in the *proposal review* will be funded. Decisions to fund proposals will be based on funds available, scientific and technical merit, and potential contribution and relevance to the NRI goals. All *proposals* selected for award will be funded through NERC and will be subject to oversight by NERC.

Any awards are tentative pending formal agreement of the fellow's host institute to accept and administer the funds in accordance with a research agreement with NERC. The investigator(s) will be expected to facilitate administrative matters if needed.

B.4 Solicitation Schedule

Proposal Timetable	
Event	**Deadline**
Publication of Request for Proposal	August 1, 2010
Deadline to Submit Proposals to NERC	October 16, 2010
Awards Announced	December, 2010
Award Start Date	First quarter, 2011