

Request for Proposals for the Nanoelectronics Research Initiative (NERC RFP # S201215)

A. Background

The Nano Electronics Research Corporation (NERC) is soliciting proposals from US Institutions qualified to do research in areas of interest to the Nanoelectronics Research Initiative (NRI). NERC makes this solicitation on behalf of NRI's participants and in connection with NRI's collaboration with the National Institute for Standards and Technology (NIST). NRI participants consist of five leading semiconductor device companies: GLOBALFOUNDRIES, IBM, Intel, Micron, and Texas Instruments.

NERC, a not-for-profit research management organization, operates under the direction of the NRI Governing Council and is a wholly-owned but separately-managed subsidiary of the Semiconductor Research Corporation (SRC). SRC is a research management consortium that was established in 1982 and sponsors semiconductor research for its members.

As the CMOS (Complementary Metal Oxide Semiconductor) technology approaches its ultimate limits, new nanoscale device concepts and architectures must be explored. For this reason, the time horizons and objectives of important industry-sponsored research programs – the Global Research Collaboration (GRC) and the Focus Center Research Program (FCRP) – are being extended to explore and develop the technological possibilities of a post-CMOS world. NRI will continue to be positioned as the most forward-looking of these programs.

NRI was established in 2005 to focus research and resources on specific beyond-CMOS device concepts that could extend the “emerging technologies” of the International Technology Roadmap for Semiconductors (ITRS), particularly those areas covered in the Emerging Research Devices and Materials working groups (<http://www.itrs.net/Links/2011ITRS/Home2011.htm>), with the goal of sustaining the historical growth trend of the digital electronics industry. The on-going NRI collaboration with NIST is expected to stimulate research that will address long-range semiconductor research needs and identify new device technologies.

The NRI was created with a mission to “Demonstrate novel computing devices capable of replacing the CMOS FET as a logic switch in the 2020 timeframe.” Research was primarily aimed at the exploration of devices for logic that could show significant advantage over ultimate FETs in power, performance, density, and/or cost to enable the semiconductor industry to extend the historical trends in cost and performance. While many new and exciting device concepts have been explored under the program, a clearly superior candidate for the “next switch” has not yet emerged. This increases the urgency of continuing the work, but also indicates the need to think more broadly about how to address the challenge.

Many of the new phenomena, materials, and devices discovered and developed in NRI are promising by a variety of metrics, but do not necessarily have all the attributes of a superior digital switch. Most are slower than CMOS, and consequently are not competitive in performance when inserted into established CMOS circuit architectures. However, many show

potential for operation with much reduced energy dissipation and many exhibit unique functionality, such as non-volatility and suitability for reconfigurable circuit architectures. To take better advantage of these properties, future NRI research will expand beyond its present focus on the logic device to include the circuit and architecture level. Device-focused proposals are still sought -- particularly proposals for novel devices that can enable digital switching with greatly reduced energy dissipation *and* improved switching speed compared to the FET. To beat the power problem, such devices must operate on principles conducive to greatly reducing the stored energy which distinguishes and preserves digital states, or on principles conducive to operation in energy-conserving circuits. Based on the lessons learned from the first phase of NRI, and the data collected on many new technologies, the research vectors have been refined for the next phase accordingly, while maintaining the core of NRI's primary mission.

A 1 - Research Areas of Interest

NRI Mission: Demonstrate non-conventional, low-energy technologies with potential to outperform CMOS approaches on critical applications in ten years and beyond.

- These computation-focused technologies should include both novel device and architecture approaches to achieve low-energy, high-functionality solutions, and can include logic, memory, analog and other components, with a particular emphasis on non-conventional devices whose properties may span these categories.
- The primary research vectors to be pursued are:
 - Devices utilizing alternative state vectors for representing information
Examples include but are not limited to devices based on spin or photonic state, or collective effects such as magnetism or ferroelectricity. Voltage-based devices are welcome, but must operate by novel physical principles which provide distinct advantages over the conventional FET.
 - Devices with higher computational density
Examples include but are not limited to devices which combine memory, logic, analog or other functions, devices which are conducive to high fan-out and/or high fan-in circuits, reconfigurable circuits, or any other approach to greater logic efficiency.
 - Novel interconnect approaches native to the information token
Examples include but are not limited to novel transduction devices (if the logic device is not externally voltage-based), advanced contacts to the active device, and novel circuit topologies.
 - Non-equilibrium systems for enhanced noise immunity, low energy dissipation, and high performance
Examples include but are not limited to phonon engineering, devices which exploit physical phenomena with timescales shorter than the thermal equilibration time, or devices conducive to use in energy recovering or energy conserving circuits.
 - Architectures to exploit non-conventional device behavior for manipulating information
Examples include but are not limited to non-Boolean, analog-like, and neuromorphic or other biologically-inspired architectures, and architectures which trade digital precision for reduced power consumption or which are conducive to cost-effective nanoscale regular/modular patterning and fabrication.

- To ensure the results are relevant and sufficient for proving out the new approach, simulation and experimental demonstration of all parts of the technology are included, from developing new materials and demonstrating new phenomena to fabricating, patterning, and characterizing devices and basic circuits.

NRI is seeking to encourage research on topics which have potential for maintaining the historical trends in increasing computational power and decreasing cost of information processing. Ideally the devices and circuits should be targeted to compete favorably with tomorrow's high-performance CMOS technology for general purpose computation, but devices and/or circuit architectures that perform well for specific and important applications or algorithms or at ultra-low power will be carefully considered. Proposers are encouraged to consider devices with novel function beyond that of a simple digital switch, and to look for circuits and application areas that exploit this behavior for maximum benefit. Whatever application space is chosen, the focus should not only be on showing how the device/circuit can outperform CMOS at the end of the CMOS scaling roadmap, but also how far the new device/technology can be extended beyond the end of the CMOS roadmap. Here, scaling means more than simply doubling the number of devices on a chip each technology generation. The focus should be on compounding increases in computational performance without being limited by physical and economic constraints on power dissipation.

Similar to the ongoing research at current NRI Centers, proposals for the next centers should be "device-centric." Exploration of novel materials is encouraged, but should be motivated by the desire to demonstrate and establish more promising and novel device concepts or circuit architectures. New centers should establish interdisciplinary teams to effectively address the key research problems engendered by each device and related circuit architecture, from materials growth to fabrication and characterization, and from basic physics and simulation to device design and circuit implementation. More specifically, each center is expected to focus on 2-3 device technologies, with multi-PI and multi-university teams to cover all key areas of research as listed below to implement computation with that device.

- Novel materials development, growth, and characterization
- Novel fabrication techniques, such as self-assembly, if appropriate for a particular device or circuit architecture
- Physics theory and experimental verification of key phenomena, including work on phonon transport / heat flow for novel cooling mechanisms and/or non-equilibrium behavior
- Device modeling, design, fabrication and characterization
- Novel circuit & architecture work to take advantage of the unique device properties (e.g. non-volatility / built-in memory) for low-energy or energy-recovery during operation

Ideally, all proposals will have at least one PI working in each of these areas for each device technology being proposed. Of course in some cases, it may be more efficient to have a single PI working in an area as part of more than one device team, either within a center or across centers, where his/her work can be used more broadly. (For example, a PI developing graphene growth or characterization processes may support several different graphene device efforts.) Particular focus should be given to the planned circuit/architecture implementation for the device, i.e. how will this device actually perform computation and what will be the total speed, energy, and area of the base computational unit being proposed. While the focus should remain on finding a new device for computation, consideration should also be given to the

system as a whole, including integrated memory devices, interconnections, and communication.

Proposing continued work on devices already being studied in NRI is acceptable, assuming the data collected to date shows promise for the future. However, promising *new* device or architectural proposals are strongly encouraged. NRI will continue to focus exclusively on “beyond CMOS” devices” and will exclude any FET type devices, including tunneling FET (TFET) devices where the materials are standard semiconductors (Si, SiGe, III-V, etc.) and the structures are largely FETs with tunneling injectors at the source. NRI does encourage research proposals on more novel devices based on tunneling, in particular, devices utilizing novel materials such as graphene or topological insulators, or which otherwise introduce novel physics for greatly improved device attributes. Similarly, NRI encourages proposals for devices based on spin or magnetism, in particular, proposals that leverage new device physics to go beyond the capabilities of known spin- or magnetism-based devices. NRI also strongly encourages proposals to explore novel technology concepts in line with the new research vectors on “non-conventional” and “high computational density” devices and architectures.

All proposals should include a strong characterization and nano-metrology component, to link between the experimental and simulation work. Proposers are encouraged to highlight areas where new breakthroughs in metrology are needed and to consider collaboration with NIST to enable characterization of materials and devices, particularly if it requires the discovery and development of potentially revolutionary measurement techniques and tools.

The primary outcome of all projects should be to produce sufficient data and understanding of each device area to enable conclusions on whether it could pose a viable option for extending scaling beyond the limits of CMOS. Ideal outcomes would be functional proof of concept demonstrations of computational technologies with significantly improved computation per unit power per unit area. Barring a full demonstration, a plan to have a strong set of data through experiment and simulation to evaluate a device technology’s ultimate capability is also important. That “ultimate capability” may turn out to be for a related function (e.g. memory) rather than as a pure logic device, in which case it might be considered for future research in other SRC programs (e.g. the Focus Center Research Program, FCRP).

Note that NRI does not intend to fund efforts overlapping with the new FCRP program. If applicable, proposers should explicitly state how the work in the NRI center is significantly differentiated from any similar work proposed in FCRP, particularly if there is any overlap in PIs.

Proposers are encouraged to reference the NRI website (www.src.org/program/nri) for additional information on the current NRI research centers and projects.

A 2 - Proposal Process

This solicitation is open to all U.S. universities and shall be conducted on a competitive basis. Universities should join together to achieve the depth and scope needed to address the technical content of this solicitation, as all NRI research will be funded through interdisciplinary, multi-university Centers. Proposed collaboration among PIs and universities in the form of Centers should identify a lead university and lead PI for purposes of an award and consummation of a sponsored research agreement with the Consortium. Cross-sharing between universities is strongly encouraged, but only U.S. institutions of higher education or their associated research institutions will be considered for funding.

Proposals are encouraged from both the existing NRI Centers as well as new Center teams. In responding to this solicitation, the existing NRI centers are expected to put together new programs which focus on the research areas described here, and which will likely include new PIs and universities. Note for all proposals, it is strongly encouraged that the number of PIs and universities involved be limited to a reasonable number for the total budget, to insure that each PI is getting a critical mass of funding. No formal minimum amount per PI per year is being stipulated, but in general each PI should have sufficient funds to fully support at least 1-2 students or post-docs.

Investigators should ensure that their proposals address the following essential attributes:

- A research plan which contains a compelling and well-articulated vision on how the center's work will result in key learning about specific device and/or circuit technologies that complement or support the NRI's research agenda described in Sec. A1.
- If applicable, a clear explanation of how the proposed research will be unique or how it will be distinguished from related university research in nanoelectronics. (Such an explanation may be helpful because NRI aims to support research which compliments but does not overlap that of other industry-sponsored university research programs.)
- A list of clear milestones that will result in sufficient learning about the proposed technology to prove out its future potential as a platform that can scale beyond the expected limits of CMOS technology for logic/computation.
- A reasonable scope of research which can be realistically executed with available resources and in accordance with sound cost management.
- A description of the host institute's policy and history of successful industrial collaboration regarding the exchange of staff, recruiting of students, intellectual property agreements and previous successful collaborations with industrial partners.
- A statement addressing the availability of facilities and resources needed to help make the proposed project successful. This should include any plans for collaboration with NIST or other labs / institutes / NRI member companies for doing joint work, if applicable.
- A statement addressing the plans for matching funds from university, state or federal sources to leverage the funds from NRI. There is no formal requirement for cost sharing, but proposals that include matching funds and infrastructure investments will be considered favorably in the review process.

Based on this solicitation, approximately 2-3 centers are expected to be funded. The proposals will be reviewed by the NRI Technical Program Group (TPG), which comprises senior researchers from the participating companies (GLOBALFOUNDRIES, IBM, Intel, Micron and TI) and NIST. In addition to financial support appropriate to pursuing mutual interests of the investigators and the NRI, there will be an opportunity to collaborate with industrial researchers from NRI participating companies and from NIST. The research results should be widely disseminated, and publication in technical journals and presentations at conferences is strongly encouraged. Participation by funded researchers in the NRI reviews, and potentially at industry/government sponsored workshops and meetings, is required. There is an annual review of the overall NRI program, as well as annual on-site reviews of each center and quarterly reports submitted to NERC from each center. All publications, reports and review materials are to be posted on the NRI website.

Evaluation, technical review and recommendations on the proposals will be done by the NRI TPG, and the final decision on the awards will be made by the NRI Governing Council.

A 3 - Program Scope and Planned Funding Level

Project proposals are expected to be for a five year time period, with funding allocated on a yearly basis. There will be a checkpoint at 2 years to allow for re-direction as needed within the Centers; this will not be a re-competition, but the NRI review committee is expected to give formal feedback on any re-direction needed, including changes in projects and PIs. All funding after the first year will be contingent upon successful performance, as evaluated by the NRI-NIST collaboration, and availability of funds. Several multi-university center awards could be made in the areas identified, with the average award expected to be from \$1,500,000 - \$2,000,000 per year per center from NRI, in addition to any matching funds being proposed. Following proposal selection, research agreements will be negotiated with awardees as appropriate, with the research expected to start in the first quarter of 2013. Any potential for additional funds from university, state or federal sources to match the NRI funds should be included in the proposal and will be considered in the review process. These are expected to be included in the final formal budget, and will be tracked just as the NRI funds are. Not all areas of interest may necessarily be funded, and the titles of the broad areas of interest are not synonymous with the names of the current or planned research agendas, nor are there any implications that an area of interest cannot accommodate more than one research effort.

B. Proposals guidelines and schedules

B.1 Purpose, Format, Content and Length of Solicited Proposals

Solicitation Purpose and Process

In order to permit selection of the proposals most likely to advance the NRI research goals; proposals are being solicited from investigators to address the NRI agenda in Sec. A1.

The proposals are due electronically by 5:00 p.m. Eastern Standard Time at the Nano Electronics Research Corporation (NERC) on November 14, 2012. The process and address for submitting these proposals is described below.

Proposal Format, Content and Length

Go to: <http://www.src.org/app/proposal/submit/> to download the **NRI Template Package** and read the **Guide to Online Proposal Submission**. In order to submit a proposal you will need to obtain a proposal number by e-mailing Allison.hilbert@src.org.

The proposal format is:

1. When you first enter the Submit a Proposal Submission page you will be prompted to complete the cover page. After completion, you will need to print the cover page you have just created and gather the necessary signatures.
2. A Center **Research Overview** (included in template download), consisting of:
 - a. Table of Contents keyed to the page numbers of the proposal sections.
 - b. An Executive Summary, a one to two page description of the proposal and key features.
 - c. Description of the center research objectives, themes, project portfolio, and structure, not to exceed 6 pages. This section should show the total planned center portfolio, structured around specific device concepts the center will pursue.
 - d. Statement of Work, to include a one page table of projects/PIs organized by device theme, followed by one-page description of each project including a description of the research, goals, fit to NRI objectives and to a specific device theme, and a timeline of key milestones.
 - e. The availability of the resources necessary should be described in 500 words or less, including plans for receiving matching funds from university, state, or federal sources to leverage NRI funding.
 - f. The Center's plans for collaboration with industry and NIST should be described in 300 words or less.
 - g. List of key personnel and relevant publication record and references.
3. **Catalog Page** (included in template download), lists tasks under theme.
4. High-level **Budget** (included in template download) broken down by theme and university for the funding period requested, including the matching funds from university, state, or federal sources. Note that if a proposal is selected for funding, a full detailed budget will be needed prior to contracting.

B.2 Proposal Submission Process and Related Information

Submission Process

Electronic submission of all proposals is required. Please contact Allison Hilbert (allison.hilbert@src.org) for a Proposal Number before attempting to upload your proposal. Please address all questions to Thomas Theis, NRI Director, by email (thomas.theis@src.org).

Disclosure of Proprietary Information

All proprietary portions of proposals must be clearly marked. Restrictive notices notwithstanding, proposals may be handled and read for purposes of evaluation by NERC, NRI Participants, NIST officials and selected external reviewers.

Intellectual Property

NERC expects proposals to comply with the policies and procedures of NRI concerning Intellectual Property (IP). In return for sponsoring research, NERC receives a royalty-free, nonexclusive, worldwide license to intellectual property (including software, copyrights, patents, mask registrations). Universities own and are free to license this intellectual property to companies outside the NERC community. Certain IP rights will also have to be provided to NIST. NERC may be available as a resource, to assist awardees strategically and financially, as appropriate, to develop IP rights developed under their awards.

Blocking Background Intellectual Property

Blocking Background Intellectual Property (BIP) is defined as patents, patent applications, or computer software of any party that is required to practice the anticipated results of the research. NERC funds University research on the condition that NERC Member companies will have the freedom to practice the results of the research. The existence of Blocking BIP of any party can seriously impair or even block the ability of NERC Members to exercise this freedom to practice. Therefore it is important that NERC be informed as early as possible of the extent, if any, that the proposed research requires the use of Blocking BIP.

B.3 Evaluation Criteria and Selection and Award Process

Evaluation Criteria

The selection criteria used in the technical review of the proposals, in order of relative importance and priority, are:

1. Overall scientific and technical merit, including:
 - a. Impact of the proposed work on the NRI research agenda
 - b. Plan for producing data necessary to prove-out a new technology
 - c. Ultimate potential of the technologies being pursued
2. Ingenuity, novelty, and feasibility of the proposal.
3. Investigator(s) capabilities and related relevant experience.
4. Access to the needed personnel, resources, facilities, equipment, and data to perform the work.
5. The potential for leveraging NRI funds with university, state, and federal funds.
6. Quality of the industrial and/or NIST collaboration plan.
7. Intellectual property issues and policies which may preclude timely execution of the contract.

Selection and Award Process

Proposals will be evaluated by a Proposal Evaluation and Selection Committee, comprised of a group of senior researchers from NRI participating companies and NIST. The proposer will be notified of selection or non-selection in a timely manner.

All non-selected proposals will be destroyed, except one copy which may be retained for file purposes, unless the applicant has requested that the proposal be made available for consideration of alternate funding by other NRI participating company funding instruments.

Not all proposals submitted in response to the invitation by NERC and selected in the *proposal review* will be funded. Decisions to fund proposals will be based on funds available, scientific and technical merit, and potential contribution and relevance to the NRI goals. All *proposals* selected for award will be funded through NERC and will be subject to oversight by NERC.

Any awards are tentative pending formal agreement of the fellow's host institute to accept and administer the funds in accordance with a research agreement with NERC. The investigator(s) will be expected to facilitate administrative matters if needed.

B.4 Solicitation Schedule

Proposal Timetable	
Event	Deadline
Publication of Request for Proposal	August 1, 2012
Deadline to Submit Proposals to NERC	November 13, 2012
Awards Announced	January, 2013
Award Start Date	First quarter, 2013