

RA S201209

FCRP Proposer Information Pamphlet

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This pamphlet provides further technical information on the areas of interest, as well as information on the submission, evaluation, and funding processes, proposal and proposal abstract formats, and other general information.

The Focus Center Research Program (“FCRP”), a consortium of industrial participants and the Defense Advanced Research Projects Agency (“DARPA”), (the “Consortium”), solicits white papers from U.S. universities for collaborative, multidisciplinary, multi-university research in selected areas of principal interest. These topics include: (i) highly complex, multi-scale, integrated networks of systems and (ii) new semiconductor technologies beyond digital Complementary Metal-Oxide Semiconductor (“CMOS”).

The goal of this collaborative effort between the Department of Defense and the industrial participants is to increase substantially the unprecedented multi-decade record of uninterrupted performance improvement in information processing power and storage capacity of integrated circuits and related systems. This historical advance in IC and related systems technologies resulted from research and development efforts that benefitted both the military and industrial sectors. It has provided the Department of Defense with an unmatched technological edge in advanced weaponry and provided the U.S. economy with the productivity enhancements critical to U.S. economic growth.

The Consortium seeks to address emerging challenges in semiconductor and systems technologies by concentrating resources on high-risk, high-payoff, long-range innovative research to accelerate the productivity growth and performance enhancement of semiconductor integrated circuits and multi-scale systems. To this end, the FCRP is focused on exploratory research beyond the horizon of the International Technology Roadmap for Semiconductors (ITRS), and seeks to undertake off-Roadmap opportunities.

A two phase selection process will be used:

1. First, a "Proposers' Conference" will be held to review this solicitation with interested university teams. A white paper is then requested to outline a university team's proposal for a Center. These white papers will be reviewed by the Consortium, and the most promising will be selected to invite full proposals. The university teams selected to submit full proposals may be given feedback by the Consortium on ways they could strengthen their proposal to meet the research goals, i.e., there will be an opportunity for these teams to discuss potential collaborations to create combined Centers.
2. Second, full proposals for multi-university Centers will then be submitted for final selection for award by the Governing Council of the Consortium. The selection timeline is given below:

Research Announcement Release	April 23, 2012
Bidders' Workshop	May 14
White Papers Due	June 15
Response to White Papers	July 9
Full Proposals Due	September 14
Proposals Selected for Award	October 15
Contracts Completed	January 15, 2013
Launch Centers	January 15

This collaborative research initiative will operate under the direction of the Governing Council comprised of representatives of industrial and government participants. Industrial participants include a select number of defense, semiconductor and IT systems companies. DARPA is the government participant. The FCRP is administered by the Microelectronics Advanced Research Corporation (MARCO), a not-for-profit, special purpose entity that acts on behalf of the Consortium.

To engage the best research ideas in each field and topic, it is anticipated that a Center (or other administrative or collaborative structure, hereinafter referred to as 'Center') will be comprised of multiple institutions that may be geographically separated. Therefore, each Center is to be a virtual institution, comprised of a lead university that serves as the contracting institution, and one or more affiliated universities. All activities within a Center are to be managed by a Center Director at the contracting university. Each Center is expected to achieve a level of cooperation between academic departments, institutions, and industrial firms such that the total output is much more than the sum of the individual research projects.

Unlike many other industry-university research programs, the FCRP is intended to sponsor revolutionary research that results in the elimination of technology barriers and broadly impacts the entire semiconductor and defense industries. FCRP researchers are expected to create new technology options and establish new semiconductor and complex systems design technology directions through exploratory research focused on the long-term needs of the semiconductor, defense and applications systems industries. The major payoff of these research efforts is expected to be commercially viable 8-12 years from project initiation. Although the general scope of research topics is bounded, program objectives are defined with less granularity than is customary for industry-university programs. Proposing institutions should emphasize how a proposed Center and its organization will operate to produce new knowledge by the faculty investigators and associated researchers (e.g., research associates, post-doctoral scientists, industrial researchers-in-residence, graduate students, technicians and undergraduate students). Proposers should also emphasize opportunities being pursued within the Center to enhance the technology infrastructure available to the FCRP participants through the Center. The organization of each Center is critical to the eventual success of the program. Universities responding to this solicitation should ensure that their proposals address the following key attributes, at a minimum:

- A compelling and well-articulated vision for long-term, exploratory research illustrating its importance to U.S. semiconductor and defense industry competitiveness and to U.S. Department of Defense superiority; a vision that is both embraced and enthusiastically deployed; a vision that leads to the conception, demonstration, and evaluation of revolutionary technology options;

- A crisp, motivating and empowering mission that is used by all Center participants as a guiding principle to make decisions;
- An interactive, cross-disciplinary, multi-institutional environment, where the implications of all research plans and results are adequately comprehended by the entire team of Center investigators;
- A dynamic process for Center research evolution, including a methodology for adding, subtracting and modifying research directions within the Center, and involving new researchers and institutions as appropriate to enhance and renew the effectiveness of the Center;
- Acknowledged global leadership in the field based on pioneering contributions;
- An up-to-date understanding of all significant technology barriers within a Center's area of focus, and an understanding of the larger context in which the Center's work is performed;
- A plan and methodology for interacting with other appropriate Centers on collaborative research technology transfer between Centers; and
- A clear, well-defined management plan.

Each Center should have formal recognition and support from the university administration at the participating institutions, as appropriate. This might include cash, in-kind support, facilities, resources, access to space as needed to integrate the Center with the departments and programs at participating institutions. Each Center requires a team of faculty that is willing and able to work synergistically across departments and across institutions. This team must strive for a unified strategic vision, and then optimize the utilization of all Center personnel, resources, and facilities to achieve the vision. The institutions participating in the Center should develop practices to ensure that geographical separation and different institutional cultures do not prevent synergism. In addition, the participants in the Center should establish formal mechanisms for supporting individual projects that pursue non-conventional research approaches to overcome specific technology barriers.

The Center management style and structure for administering individual research projects or multi-project tasks is a critical subject that should be clearly addressed within the proposal. At a minimum, the organization and management of a Center requires a single, senior-level director who reports directly to at least the level of dean. The director's primary role is to guide and coordinate Center research by providing intellectual and organizational leadership. To enable success in this role, the following key characteristics should apply:

- The Center director is an employee of the lead institution in the Center;
- The position of director cannot be shared or rotated;
- The director is responsible for administering the award on behalf of all participating institutions within the Center;
- The director is responsible for initiating the evolution of the Center program, including but not limited to, originating and eliminating tasks and projects within the Center as opportunities and results arise; and
- The Center director is responsible for handling the administration of the awards on behalf of all participating universities.

AREAS OF INTEREST

Introduction

The objective of the FCRP is to look beyond today's technology horizon and to lay the scientific groundwork for the semiconductor and defense systems industries' enhanced delivery of technological and cost-effective solutions for the high-level issues facing the systems-based industries. Specifically excluded is research that primarily results in evolutionary improvements to the existing state of practice. To address effectively the needs for such long range and innovative research in the various target areas, the FCRP uses the concept of virtual Centers. As such, a Center consists of a lead university and a number of associated institutions. The Centers will:

- (i) Concentrate attention and resources on those areas of microelectronics and systems research that must be radically advance the technological capabilities of these industries as well as to drive new applications;
- (ii) Strengthen the university research infrastructure and expand its capabilities to perform microelectronics and systems-focused research;
- (iii) Achieve critical mass through relatively large blocks of funding together with the active participation of industrial visiting scientists, and
- (iv) Provide the optimal balance of creative freedom and targeted objectives.

To optimize innovation, Center researchers have more autonomy and are expected to have a longer-term perspective than is traditional with other industry-university programs. ***Research funded under the FCRP, being high-risk and innovation oriented, is commensurately long-term. The economic benefits of FCRP-funded work are expected to be realized 8-12 years from initiation.***

Each of the research areas described below is of equal importance for funding. However, these areas may not necessarily be funded equally. The Consortium does not guarantee that all areas will be funded. In general, the research should be directed toward the challenges well beyond the horizons of the ITRS. Proposers are encouraged to focus on projects that are devoted to investigating "new frontiers" of research in semiconductor technology, design, components, and multi-scale systems.

In addition to providing enabling technologies, the research scope for each Center represents a critical hierarchical component in the development of systems for both the semiconductor and defense industries and the Department of Defense. The success of the FCRP is contingent upon the cooperation and movement of ideas between the Centers. The research direction of each Center is formed in response to the needs defined by the program participants.

Under this RA, submitters may propose innovative research Centers in one or more of the following topical areas:

NEXT - Highly Complex Systems

Technology Areas for NEXT – The mission of the NEXT thrust area is to enable highly complex systems with capabilities well beyond those available today, i.e., to augment beyond the “sum of the parts.”

1. High performance analog for high speed wireless; THz electronics for imaging, sensing, novel power devices
2. Vehicle and Distributed Sensor Networks
3. Computing System Architectures based on CMOS technology
4. Tools and methods for design, verification, and predictive modeling, including physical modeling of thermal and structural impacts on functionality and the physics of failure of proposed components.

ACCEL - Semiconductor Technologies beyond CMOS

Technology Areas for ACCEL – The mission of the ACCEL thrust area is to identify and accelerate progress for new mainstream technologies beyond digital CMOS.

1. Nonconventional material systems
2. Quantum engineered devices and new sensors and transducers
3. Integrated circuits and computing architectures

Out-of-the-box research proposals that address these areas in novel ways are encouraged, and proposers are further encouraged to combine topics in order to produce ground-breaking research.

In the following sections, each topical area is outlined with a statement of scope, background, and a list of research needs identified by the Consortium. None of the topical area descriptions contained in this solicitation should be considered entirely comprehensive or exhaustive; your white paper/proposal should outline your own vision and plan for achieving the vision. White papers/proposals that show in-depth knowledge of the topic and of the significant problems faced by industry and researchers for that topic will receive the most positive evaluations from the proposal review team.

Offerors must clearly identify the area addressed by their white paper/proposal on the cover page. If Offerors choose to address multiple topical areas in their white paper/proposal, they should clearly state the areas and illustrative challenges being addressed.

Technology Areas for NEXT – The mission of the NEXT thrust area is to enable highly complex systems with capabilities well beyond those available today, i.e., to augment beyond the “sum of parts.”

1 – High performance analog for high speed wireless; THz electronics for imaging, sensing, novel power devices

Scope: Development of new analog and mixed signal circuit architectures and techniques are needed that enable the efficient transmission (generation), reception (sensing), manipulation and processing of analog signals (information)

as well as conversion of analog signals to the digital domain. (Note: Analog refers to RF signals from MHz through THz frequencies.) Of particular interest are techniques that support multifunction systems (transmission of multiple waveforms through a common aperture/antenna), ultra wide operational and instantaneous bandwidths, high resolution/sensitivity (high dynamic range) and sensors that adapt to their environment, all while minimizing power consumption for dynamic operating conditions. Circuit approaches that exploit advances in CMOS technology (scaling and integration density) as well as 3D integration and, heterogeneous integration of ‘higher performance’ non-Si semiconductor devices and MEMs with CMOS, are of interest as are emerging materials, devices and new phenomena. Circuits and architectures that interact with, enhance and/or mimic human (sensing) functions are also of interest.

Background: Advances in microelectronics performance and integration have led to the proliferation of portable personal communications, entertainment and computing devices as well as revolutions in health care, security and automotive electronics. Much of this innovation is a direct result of the exploitation of CMOS scaling (increased integration density and lower ‘digital’ power consumption) and ‘digitally assisted’ analog/RF design techniques. Further advances, however, are encountering significant challenges – i.e., the need for wider information bandwidth, operation in cluttered electromagnetic environments, increased overall power consumption, etc., not to mention increased expectations and demands of the end user.

Research Needs: While digital circuitry directly benefits from CMOS scaling, analog circuitry does not. For example, while CMOS scaling leads to higher switching speed and lower power consumption, the lower operating voltage (or voltage swing) limits dynamic range, linearity and output power of RF circuits and analog circuit efficiency suffers. This problem is exacerbated as the technology is extended to sub-millimeter and THz frequencies. Thus, there is a compelling need for even greater advances in microelectronics design techniques and circuit architectures that offer greater energy efficiency, **especially under high operating voltages**, greater sensitivity, higher resolution, greater selectivity, wider bandwidth and that can ‘intelligently’ adapt to/interact with its physical or electromagnetic environmental and/or end user (human).

Analog circuit/architecture examples include (but are not limited to):

- Dynamically field programmable (adaptive, scalable) RF multifunction components/arrays
- High efficiency, wideband, linear low noise and power amplifiers (with dynamic RF power control)
- High power mm-wave sources
- Self-healing/self-calibrating RF circuits
- Cognitive sensors (radios)
- High dynamic range, energy efficient, millimeter wave direct sampling (RF to bits)
- RF photonics
- Biometrics (including standoff biometrics detection)
- On-chip adaptive/tunable, high Q filters
- On-chip power conditioning circuits
- On-chip thermal management
- On-chip oscillators for high fidelity frequency sources

Finally, continued advances in material and device technologies and the emergence/exploitation of new materials, devices and physical phenomena (e.g. multiferroics, carbon electronics, magnetic, spin, ...) will provide designers with substantially improved performance or novel capabilities that can serve as the basis for innovative design techniques. Thus there is a need to develop circuit architectures that exploit these emerging devices and physical phenomena.

In addition to new circuit architectures/techniques, new high performance analog processes, devices, and materials are needed. In general, these new processes, devices, and materials should offer higher analog performance, including higher transconductance, lower noise (especially 1/f), higher output impedance, and improved energy efficiency. Passive device performance improvements are also needed, including precision capacitors with 'high' capacitor density and excellent linearity and matching; and precision resistors that offer excellent matching, TCR, and current-carrying capability at reduced feature sizes.

One critical focus area/need is in the area of novel power devices and integrated power technologies that offer improved power performance, low loss power combining strategies, and energy efficiency. These include but are not limited to:

- 1) Next generation high voltage, high power devices – modelling, device architecture and design, and process implementation for power devices using materials such as Diamond, BN, etc. These will help drive power device performance beyond that currently achieved by just GaN or SiC.
- 2) Creation of a solid state power combining approach to generating technologically significant levels (1W) at 1 THz.
- 3) Heterogeneous integrated power in a cost effective manner of widely used Si material and attractive WBG material like GaN to create smart power devices and integrated systems (using GaN on Si) where devices are simultaneously fabricated on both GaN and Si substrates. This should be closely coupled with appropriate materials research in improving interconnect and packaging technology, **including on-chip thermal management and fine-granularity thermo-mechanical-electrical co-design**, to help drive to much higher power densities in future power systems.
- 4) Other heterogeneous systems should be explored to exploit the full potential of not only driving new power devices but also integration of power and sensors, **with their distinct thermal management requirements**, enabling additional applications for the future.

Another critical focus area/need is in the area of Integrated MEMs Sensors and Systems. These systems should be able to integrate all elements, including the appropriate sensors, signal processing, power management, calibration, and interfaces for future consumer, automotive, industrial, and defence applications.

2 – Vehicle and Distributed Sensor Networks

Scope: Design and implementation of integrated modular architecture (IMA) communication networks (i.e. distributed systems) are needed, including methodology and tools for choice of synchronous/asynchronous communication systems and the co-design of functionality and implementation platforms.

Regarding *functionality* there is a need to address communication, computation and control of mechanical and electrical systems. This includes focus on requirements modeling and analysis-based and contract-based design methodology

Regarding *integration* there is a need to co-integrate heterogeneous systems including testing protocols and specification of subsystems for reuse across multiple platform instantiations.

There is a strong interest/need to enable *autonomous* operation and fault tolerant technologies.

Research Needs: Heterogeneous system design is needed including verification and integration. This includes extensions of platform-based design and contract-based design requirements to address mechanical, electrical, computing and communications in a unified setting. Uncertainty in requirements and description of a layered set of abstractions moving from conceptual design to detailed design to implementation and integration using meta-modeling framework should be addressed.

Research is needed to address the dynamics of joint design of protocols and performance in “specify then design” paradigm rather than current “design then verify.” This includes dynamics at all phases of requirements, design, and integration to ensure composability constraints can be satisfied.

The issue of scale shall be addressed via exploring single and multiple autonomous systems including at least 10^4 nodes/loads and multiple hierarchies of (sub)networks. Detailed fidelity of mechanical and electrical modeling (multiscale in time and length including communication scales) shall be included.

3 – Explore Computing System Architectures based on CMOS Technology

Scope: Highly parallel computing including data and interconnection architecture, nonconventional computing systems based on CMOS.

The goal of this research implies highly parallel and efficient systems including computing, interconnect and storage architecture, with the ability in the architecture to cover a range of implementations in size and energy proportional performance by a factor of 100x or larger in the same generation. In addition, this goal implies architectures that will enable systems whose performance will scale throughout time for at least one decade, delivering 30x or more performance at a constant size and power consumption at the end of the decade.

Background: Considering that projections of existing CMOS-based components are not expected to be able to continue to deliver on the desired metrics, new architectures must be capable to effectively integrate emerging CMOS-based capabilities such as 3D silicon, novel memory devices, reconfigurable logic, heterogeneity, etc., in

addition to already established principles such as massive parallelism, workload optimized systems, extreme energy efficiency, and reliability. These elements must be combined in a scalable and efficient manner, including the enablement techniques required for successful and lasting exploitation as well as evolution from current system architectures. The exploration should include system modeling tools, system architecture, system software, middleware, application software, programming models, software development tools, circuits, devices, hardware design and verification tools.

Research Needs: Explore computing system architectures based on CMOS technology that allow continued performance and efficiency improvements in line with historic growth, namely doubling device density every two years, in the presence of diminishing or even stalling benefits arising from technology scaling, addressing workloads end-to-end. Such exploration shall target new computational and physical architectures that will bridge the gap between ultimately scaled CMOS and a beyond-CMOS approach until this non-CMOS technology becomes widespread. This beyond-CMOS or non-CMOS technology might need to break away from the pure von-Neumann model so that it or they can incorporate new mechanisms that are more scalable and efficient than traditional ones, while at the same time continue to support and evolve the software practices that are prevalent and emerging. The efforts shall address continued evolution in efficiency and scalability of existing systems architectures, as well as non-conventional architectures that introduce novel computing structures and programming models, all based on CMOS technology. The exploration should include the integration of these complementary approaches into a unified and adaptable system architecture. The resulting architectures must address improvements in: single-thread performance for Amdahl's law effects; scalability for parallel workloads and code regions; programming models for effective exploitation of the new architectures; energy proportional performance; reliability and security. The research efforts shall also address system modeling tools as well as methodologies and techniques to ensure the evolution of current systems to the new architectures. The research shall focus on architectures that are amenable for multiple generations of systems, covering the entire period up to the emergence of beyond-CMOS technologies and systems.

4 – Tools and methods for design, verification, and predictive modeling, including physical modeling

Scope: Explore and develop the tools that will enable realization of the new systems, components, and technologies that will be developed in the 10 year timeframe. The timeframe for introduction of these systems into the market would be between 2020 and 2025.

Background: This program element addresses the need for energy efficient multi-scale systems, 3-D chips and architectures, multi-dimensional transistors, nanotubes and nanotechnology with 1-D and 2-D transport mechanisms. Optimizing these systems for energy, performance, density and cost are key to their success in the market. Verification and test of these extremely complex systems will be critical to their deployment. Architectural design and construction will require new models and paradigms to be developed that optimize multi-scale and multi-dimensional systems with completely new materials and components. None of the existing tools enable us to model or verify such systems today.

Research Needs: Strong ab-initio understanding of new materials properties is needed as is modeling of the behavior of materials in the novel devices. Specifically, areas such as quantum electrodynamic transport modeling will be needed to ensure the accuracy of highly non-linear behavior of these nanostructures. Accuracy also requires

the capability to extract the device parameters, and verify the models against actual devices in a straightforward characterization laboratory.

Variations and the effect of variations need to be modeled at all levels of the design hierarchy especially as we approach complexities where compound errors can result in gross failure of the final product.

Many new systems are expected to operate in the 100's of GHz to 1's of THz range. Modeling capability at these frequency ranges is going to be critical to successfully build complex systems. What used to be considered to be parasitic at sub-GHz operation are integral part of the operation at these frequencies and modeling passives, interconnects, substrate behavior, package components, and the systems need to be developed. Measurement techniques and models at these frequency ranges are not easily available today and those that are available require a high level of expertise to even begin to apply them. Tools and models that can be used by a wide range of engineers need to be available if these products are going to enable high volume markets to grow.

Systems of the 2020s will consist of trillions of transistors (or switches) working together in a system. Modeling and verification need to be capable of modeling these systems statistically and considering the operation in an environment where reliability and unreliability have no meaning. Truly statistical modeling should be able to take advantage of the large number of available switches to enable adaptive systems to be developed for optimized performance and power.

Architecture development for large-scale systems, and even for distributed small-scale systems, will require understanding of the system requirements, the structural and performance needs, partitioning, connectivity and interconnectivity, communications, storage, power, energy management, etc., and models will need to be developed to enable system-level architecture to leverage block designs effectively.

It is expected that 3-D integration, and maybe even 4-D (taking advantage of time dependent behavior), will become an integral part of the design in the 2020s. Models need to comprehend 3-D structural optimization including partitioning for performance, heat flow in and out of the system, access to the system for connectivity as well as for test, and the complexity of verification. Modeling of the interconnect system at all levels needs to be developed to be fast and accurate – well beyond what is available today.

The development of new verification methodologies will be critical to the success of these extremely complex systems. There will be no such thing as a digital or analog system any more with most systems having a large number of mixed signal blocks. Analog verification today is hardly automated, and mixed signal verification is very limited and expensive. Tools need to be able to comprehend these integrated mixed signal systems. Beyond today's chip-level integrity modeling and verification, system-level integrity and verification is essential in these complex systems.

In addition, to support the development of these advanced circuits/architectures, particularly 3D circuits, there is a need for integrated design tools that seamlessly integrate digital, electromagnetic, mechanical and thermal simulations capabilities.

As digital, mixed signal and analog circuit complexity/density continue to increase there is a growing need to protect IP as well as prevent the inclusion of ‘malicious’ cells into these circuits. Thus there is a compelling need to advanced anti-tamper circuit design techniques and architectures, particularly for analog/mixed-signal circuits, while maintaining performance, energy efficiency and size.

The above are just a small number of examples of what would be needed in the area of modeling and verification for the systems of the future. Package modeling, thermal modeling, cooling and fluid flow models as they apply to electronic systems will need to be developed with levels of accuracy and ease of use that do not exist in the industry today. In the emerging era of gigascale and multi-scale systems, the requirements for modeling and verification are going to increase exponentially especially if industry is to maintain a trajectory of reducing development costs and time-to-market for new products.

Technology Areas for ACCEL – The mission of the ACCEL thrust area is to identify and accelerate progress for new mainstream technologies beyond digital CMOS.

1 – Nonconventional material systems

Scope: Improved and novel materials that enable 3 basic technologies: analog, memory and logic devices. These materials should address both new devices and applications as well as enhance existing device performance and provide new functionality.

Background: Over the past two decades introduction of new and improved materials to Si ICs has contributed prominently to the successful scaling of circuit density and performance. Two classes of materials illustrate this point. The first is introduction of Cu – Low k interconnect technology at the 180 nm technology node. The second is introduction of high k/metal gate technology at the 45nm node. New materials certainly will impact analog, logic, and memory applications as discussed in Research Needs below. New materials may introduce useful new functions (e.g., spin transfer torque)

Research Needs: In the analog arena new materials are needed for resistors, high voltage and high temperature electronics, capacitors, inductors, energy generation, and on-chip high density energy storage. The following materials currently being developed need better fundamental understanding and better growth processes to be integrated in commercial devices:

- 1) Epitaxial GaN, SiC, and diamond and associated integration materials such as dielectrics (e.g. AlN) and electrode materials for high voltage applications.
- 2) Complex metals and metal oxides for resistors with good temperature coefficient of resistance (TCR) e.g. CrSiCNO, CoAlO, and TiCrAlO
- 3) High-k capacitor materials – e.g. PLZT, ZrO, HfO, STO, AlOx, Ta₂O₅, Nb₂O₅ and electrodes and processes to integrate them into the back-end-of-line (BEOL)
- 4) Thin Film Batteries – Li based, or other
- 5) Organic materials for chemical sensing

- 6) Substrates for wide-bandgap semiconductor-based devices (e.g. diamond) for high temperature electronics

In the memory arena there is a need for materials enabling denser and more robust embedded non-volatile memories for the next decade and beyond. Some of the materials currently under consideration are:

- 1) Complex binary metal oxides for ReRAM, that can also enable multi state memory. These materials while seemingly common are not well understood for ReRAM applications. Some examples are: SiO_x, HfO_x, TiO_x, etc.
- 2) Ferroelectric materials with high-k, polarization, etc:
 - a. Atomic layer epitaxy (ALE) of thin sub 20 nm complex metal oxides including ferroelectric (FE) materials. Some examples are ALE of SrRuO₃ for MIM electrodes, and ALE of PbZrTiO₃ for both planar and 3-D MIM stacks.
 - b. Perhaps new FE materials to replace PZT

Many materials are needed to create logic devices with new levels of performance and power efficiency, specifically new channel/SD materials, other than Ge and III-V based materials. These latter materials are receiving a sufficient level of effort. However other materials are needed for logic devices that could also have a significant impact, for example:

- 1) New materials for low contact resistance to replace silicides and/or to obtain better silicides
- 2) New resistors with very low TCR (-40C to 150C)
- 3) Defect-free strain engineering of electronic materials
- 4) New materials for ultra-low-power spintronics applications; e.g. ferromagnetic semiconductors – mostly oxides, Topological Insulators, multiferroic materials, spin filter materials.
- 5) New materials for electrical and thermal interconnect
 - a. New materials with electrical and thermal conductivity and electromigration limits better than copper
 - b. New low-k materials with superior mechanical strength and breakdown voltage as well as appropriate chemical properties
 - c. New materials for chip-to-chip interconnect
 - d. Topological insulators
 - e. Carbon-based materials
- 6) Integration of the above materials
- 7) New Materials for alternative operation logic devices

Since many of the effects responsible for the function of future devices will depend largely on interface control, the integration of any of these materials is critically important and thus the physics and chemistry of interfaces will have to be clearly understood. Therefore, any materials research program will have to include a critical effort on the physics and chemistry of surfaces and interfaces.

2 – Quantum engineered devices and new sensors and transducers

Scope: Next generation technologies based on exploiting quantum level physics to provide capabilities well beyond state-of-the-art. Efforts should accelerate the integration of new material systems and quantum phenomena as the basis for the era beyond CMOS based devices. Preference will be given to ideas that have a clear path towards stable use in applications, e.g., at room temperature and with minimal shielding.

Background: As the CMOS scaling underlying the current era of improving computing performance can no longer provide the necessary reductions in power, there is a need for alternative energy efficient options for the next generation of microsystems. Quantum engineering of new physical phenomena, including many-body states and strongly coupled collective behaviors, offer promising opportunities for meeting these needs.

Research Needed

Summary of research needed to realize advanced devices based on quantum engineered effects

The MOSFET's dependence on a charge barrier to control the "off" leakage current, requires every electron to cross the nkT energy barrier. However if a robust state variable with improved transport properties were available there is the possibility of reducing the energy required to control the barrier by orders of magnitude. Examples of quantum engineered states include, but are not limited to, anomalous quantum Hall states, transduction through opto-electro-mechanical states, topologically insulating states, 1-dimensional and 2-dimensional transport, and a variety of spintronic and magnetic states. Preferred approaches will architect the most energy efficient logic gate based on alternative state variables, while allowing scaling into the sub-10 nm spatial dimensions, and will include work on a compatible interconnect.

Beyond transistors there are a broad range of devices where combinations of nonconventional materials and quantum engineering offer the potential for significant innovation. These should target providing novel capabilities and improving performance over existing state-of-the-art by at least 1000X. Examples include utilizing spintronics to achieve improved energy times delay products compared to electron charge based switches, excitonic states for efficient transport, unique mixing of static electric and magnetic fields in collective states of topological insulators, and the protected spin and/or electronic transport with minimal back scattering made possible by engineering strong spin-orbit coupling. These physical phenomena and others offer the potential of novel control between magnetic and electric fields, high throughput interconnects, and unique combinations of low-power and high-speed devices.

Scope: Research in sensors and transducers is needed to identify technologies that can accelerate integration of new materials into CMOS integrated circuits and to identify new devices and sensors that move integrated circuits for computation and analog signal processing into the era of Beyond CMOS.

Background: Interfacing electronics with the "real world" involves sensors and transducers, the development of which has been a historical driver of integrated-circuit technology. This synergy should continue into the future as it becomes possible to sense and control the IC environment in new ways. In some cases, it will be efficient to integrate new sensors and transducers directly, adding new types of functionality to system-on-chip circuits and improving performance and efficiency of the overall system.

Research Needed

Summary of research needed to realize new Sensors and Transducers

While computation requires dramatic improvements in energy and delay, this computation will open up new applications through high performance signal processing at the interface between humans and their world. For example, some of these applications will require higher performance sensors and transducers for temperature, position and speed (using accelerometers, gyroscopes), gas and chemical sensing, and health care for the detection of diseases and even cancer by manipulating DNA and peptides. A challenge that needs to be addressed is for these sensors to detect the target element or material in its “dirty” environment, where other elements or materials are present.

It would also be beneficial to find the means to efficiently convert from electrical to optical with a processing method that is compatible with the MOSFET integration. The closer the transduction of electrical to optical is made to the MOSFET, the more efficient and higher performance the communication (interconnect) between logic functions. When viewed from the system level, interconnect is the dominant power consumer in computing and requires new technology to address this challenge.

3 – Integrated circuits and computing architectures

Scope: This research topic is chartered to find a new energy efficient architecture to replace the Von Neumann Computer Architecture and to understand how to optimize the overall performance and energy by optimally partitioning the computational system between signal processing in the analog domain at an I/O interface, and computation in the digital domain. Hybrid analog and digital computation is envisaged to be applied to increase computation performance and efficiency (general purpose or application-specific with adaptation and learning) by exploring software, architecture, algorithms, circuits and beyond-CMOS devices and interconnect.

Background: Today’s computer architecture has not changed significantly for over sixty years since the Von Neumann architecture was developed. While it has been an extremely successful and versatile architecture and has undergone many changes in terms of its micro-architecture, it will face increased performance challenges in terms power efficiency (operations/joule) as well as power flux (W/cm-squared) and power density (W/cm-cubed) due to approaching scaling limitations with the fundamental underlying CMOS nano-technology.

However there are application specific computational algorithms and computer architectures emerging that have started to address improved efficiency for important and widely applicable applications such as pattern recognition, adaptable signal processing and machine learning. Application specific architectures have been found to be most energy efficient, and together with adaptability and reconfigure-ability, they can be applied across a large field of computational tasks while tolerating errors. Two examples of these are the machine learning algorithms that use Associative Memory and Bayesian Networks.

The input and output functions of a computing system are analog due to the nature of signals that they need to handle. Computers need to process data from numerous sensor networks, recognize events, and drive a variety of peripherals accordingly. In order to decrease the power dissipation of the system, it is of advantage to treat these

signals in the analog domain and to postpone digitizing them. Thus there is a need to develop novel analog signal processing techniques/algorithms. Architectures like cellular neural networks need to be further developed to cover such tasks.

There is also an increasing amount of understanding developing about the architectural principles of biological function and this has created an emerging area of application specific computational techniques that use hybrid analog and digital circuits. Such circuits are built with similar design principles as electrical and chemical operation of neurons. By using high redundancy of operation and normally OFF operation, these circuits could be made robust to electronic noise and unreliable electronic components while remaining highly energy efficient.

Research Needs: Hybrid analog and digital computation is envisaged to be applied to increase computation performance and efficiency (general purpose or application-specific with adaptation and learning) by exploring software, architecture, algorithms, circuits and beyond-CMOS devices—interconnects. Examples include, but are not limited to:

1. Hybrid analog and digital techniques that are bio- or cell- inspired to lower the energy of certain application specific computations.
2. Hybrid analog/digital systems where the analog/digital ratio has been optimized consistent with the application requirements
3. Stochastic techniques that incorporate or exploit variability in devices.
4. Machine learning algorithms such as Bayesian Networks that use associative memories and the probabilistic nature of the data.
5. Efficient spatial temporal data flow in massively parallel architectures such as Cellular Nonlinear Network (CNN) systolic arrays for pattern recognition.
6. New computational elements; examples include, but not limited to, coupled oscillator arrays for pattern detection and associated memory architectures.
7. Massively parallel systems that manage data locality consistent with the time-space dynamics of the application (e.g. Cellular Wave Computing)

Breakthroughs using these thrusts are being sought that will enable 100x-1000x improvements in computational efficiency and are based upon new beyond-CMOS manufacturing technology that can provide a scaling path in the future.

GENERAL INFORMATION FOR OFFERORS

Multi-disciplinary teams of individual investigators at U.S. universities are encouraged to submit white papers, and if selected, proposals to establish a research Center focused on creating innovative capabilities in the areas defined above to meet future application requirements. Teams of university investigators with coordinated research efforts are encouraged to respond, with the lead institution being a degree-granting academic institution. Active student participation in the proposed research is desired.

- A. Guided by the specific area(s) selected by the offeror, a white paper/proposal should target research to solve basic and revolutionary topics in that area(s).

- B.** Offerors are encouraged to consider providing cost-sharing funds. The formal establishment of a means to exchange personnel amongst the performers and industrial source sponsors is also strongly encouraged. It is intended that the management of the Center will be established such that each participant in the Center has the opportunity to make the Center succeed.
- C.** Teams may be formed with participation from any type of organization or entity, but the intent is that only universities will obtain direct funding under this initiative. Careful consideration should be given to how best to provide access to expensive fabrication equipment and facilities.
- D.** In their white papers/proposals, offerors should clearly describe the sources of cost sharing; furthermore, the proposed Center should adopt a management oversight structure which ensures academic freedom and is adequately flexible to allow resources to be reallocated in a dynamic fashion.
- E.** Following proposal selection, awards pursuant to sponsored research agreements with the Consortium will be made as appropriate, for base periods of up to five years, to accommodate student education and provide adequate time for discovery and progress in new areas. The research is expected to start in January 2013. There will be a checkpoint at 2.5 years to allow for re-direction as needed within the Centers; this will not be a re-competition. Overall program funding may reach a level of \$40M per annum, depending on research progress and availability of funds. The funds may not be equally divided among awardees. The administrative point-of-contact for this effort is Director, FCRP (fcrp-s201209info@src.org).
- F.** Awardees and sub-awardees are encouraged to pursue and retain ownership of intellectual property developed under their awards, or under subsequent sub-awards. MARCO is available as a resource, to assist awardees strategically and financially, as appropriate, towards this end. Awardees will be expected to have or to implement policies and agreements whereby MARCO, and through MARCO, participants in the Consortium will be granted world-wide, non-exclusive, irrevocable, royalty-free licenses to all foreground technology, inventions, or other intellectual property developed under the award. Consistent with its past sponsored research agreements with universities, MARCO seeks access to any and all background intellectual property needed to exercise its rights to the foreground intellectual property. It is highly desirable that awardees agree to identify and provide access to MARCO to relevant background intellectual property.
- G.** A two phase selection process is anticipated:

 1. First, a "proposers' conference" will be held to review this solicitation with interested university teams. A white paper is then requested to outline a university team's proposal for a Center. These white papers will be reviewed by the Consortium, and the most promising will be selected to invite full proposals. The university teams selected to submit full proposals may be given feedback by the Consortium on ways they could strengthen their proposal to meet the research goals, i.e., there will be an opportunity for these teams to discuss potential collaborations to create combined Centers.

2. Second, full proposals for multi-university Centers will then be submitted for final selection for award by the Governing Council of the Consortium. The selection timeline is given below:

Research Announcement Release	April 23, 2012
Bidders' Workshop	May 14
White Papers Due	June 15
Response to White Papers	July 9
Full Proposals Due	September 14
Proposals Selected for Award	October 15
Contracts Completed	January 15, 2013
Launch Centers	January 15

- H. Proposals and white papers will be evaluated by technical review, to be conducted by an assigned White Paper/Proposal Evaluation and Selection Committee, comprised of a group of strategic technologists from Program Participants. Evaluation will be in accordance with the guidelines set forth in the RA. The FCRP Governing Council will have final approval authority over proposals.

The selection criteria used in the white paper and proposal reviews are, in order of relative importance and priority: (1) Overall scientific and technical merit, including the likely impact on meeting the identified technology challenges; (2) Ingenuity, novelty, and impact of overall Center and new frontier projects; (3) Potential contributions to the Consortium missions; (4) Offerer's capabilities and related experience, including personnel, resources, facilities, equipment, and data to perform the work; (5) Cost realism will only be significant for proposals that have seriously over or under-estimated the cost to complete.

After the white paper evaluation is completed, each offeror will be notified of its status regarding its selectability to submit a full proposal. Feedback may be given to those offerors authoring successful white papers regarding suggested improvements for their consideration in preparation of their proposal. Non-selectable white papers will be destroyed.

When the proposal evaluation is completed, the proposer will be notified of selectability or non-selectability. Selectable proposals will be considered for funding; non-selectable proposals will be destroyed. (One copy of non-selectable proposals may be retained for file purposes.) Not all proposals deemed selectable will be funded. Decisions to fund selectable proposals will be based on funds available. However, proposals that were deemed selectable but not funded initially may be considered for funding for a period of up to one year after submission. The Consortium reserves the right to select for award all, some, or none of the proposals received. Proposals selected for funding will result in a sponsored research contract. If warranted, portions of resulting awards may be segregated into pre-priced options. Also, the complete program will be reviewed comprehensively by the Consortium at the midpoint of the five-year program.

WHITE PAPER FORMAT

A white paper should be no longer than 6 pages (including references) and, as a minimum, should contain the information given below. Responses should be electronically submitted as a single PDF document generated with

10 point or larger fonts and 1-inch margins and must be submitted via the FCRP Web Site (<http://fcrp.src.org>). Limit document size to 6 pages or less sized to the US standard (8.5 by 11 inches). Non-compliance with these guidelines may exclude white papers from consideration.

Identifying Information

- Project Title
- Topical Area(s) Addressed
- Lead University and Participating Universities
- Center Director and Lead Principal Investigators. Please include Center Director's Telephone Number, e-mail address, and mailing address.

Topical Information

- Topical Area(s) Addressed
- Executive Summary: Provide a brief description of the proposed Center and its key features and structure. Include a table clearly indicating the estimated costs by year and task.
- Vision of the proposed Center
- Summary of Research Plan
- Strategic Plan
- Innovative claims and expected research results

Management Plan

- Center Leadership and Management
- Program Evolution
- Research Personnel
- Facilities and Research Equipment

PROPOSAL FORMAT

All full proposals must be in the format given below. Non-conforming proposals may be rejected without review. Proposals shall consist of two volumes. All pages shall be printed on 8-1/2 by 11 inch paper with type not smaller than 12 point with 1-inch margins. The page limitation for proposal abstracts and full proposals includes all figures, tables, and charts. Volume I, Technical and Management Proposal, may include an attached bibliography of relevant technical papers or research notes (published and unpublished) which document the technical ideas and approach upon which the proposal is based. Copies of not more than three (3) relevant papers can be included with the submission. The bibliography and attached papers are not included in the page count given below. The submission of other supporting materials along with the proposal is strongly discouraged and will not be considered for review. Except as otherwise noted, Volume I shall not exceed fifty (50) pages. The number of pages for each section is at the discretion of the proposing institution.

VOLUME I, TECHNICAL AND MANAGEMENT PROPOSALS

- A. Cover sheet to include:** (1) RA number; (2) Center Technical area; (3) Lead Organization Submitting proposal; (4) Other Academic Institutions participating in the proposed Center; (5) Lead Organization's reference number (if any); (6) Other non-academic team members (if applicable) and type of business for

each; (7) Proposal title; (8) Technical point of contact to include: salutation, last name, first name, street address, city, state, zip code, telephone, fax (if available), and electronic mail (if available); (9) Administrative point of contact to include: salutation, last name, first name, street address, city, state, zip code, telephone, fax (if available), and electronic mail (if available); and (10) total funds requested and the amount of cost-share from other sources (if any).

Official Transmittal Letter

Note: Section A is not included in the page count limit

B. Table of Contents (not included in the page count limit)

The Table of Contents should be keyed to the page numbers of the proposal sections.

C. Executive Summary

Provide a description of the proposed Center and its key features and structure. Include a table clearly indicating the proposed costs by year and task. Also indicate cost share from any other sources, as appropriate.

D. Statement of Work

Statement of Work (SOW) written in plain English, outlining the scope of the proposed effort and citing specific tasks to be performed and specific contractor requirements.

E. Vision and Rationale for the Center

Present the vision of the proposed Center in conducting long-range exploratory systems and technology research beyond the ITRS horizon. Indicate the suite of topics and disciplines deemed relevant to the Center. Indicate the projected research results targeted by the Center.

F. Research Plan

Problem Statement: Discuss the goals of the Center, the current state-of-the-art, and the technical obstacles envisioned.

Strategic Plan: Present a high-level strategic research plan for surmounting those technical obstacles to be addressed by the Center.

Thrust Area Objectives: Organize the research program by thrust area. Provide information on the objectives and plans for each thrust area, show their relationship to the proposed Center's overall strategic research plan, and describe linkages and information flows between thrust areas. For each area, give examples of critical research issues to be addressed, providing a discussion of key barrier issues driving the research and methodology to be used. Describe any experimental test beds needed to explore and validate research results.

Innovative Claims and Expected Research Results: This section is the Centerpiece of the proposal and should succinctly describe the uniqueness and benefits of the proposed approach relative to the current state-of-art and alternate approaches.

G. Synergy

Delineate the unique contribution of each institution, and the synergy among the participating institutions. Describe the management approach of the Center that will result in synergy and close collaboration of research programs across the participating institutions, departments and disciplines. Show how the Center's multi-disciplinary synergistic approach and organization are used to solve key technical obstacles. Also, provide detailed descriptions of any historical and/or any current, on-going research relationships among the lead and participating proposed institutions.

H. Utilization of Outside Scientists

Describe the proposed Center's intentions to utilize researchers-in-residence to be assigned from Consortium members. As appropriate, in Section L, include letters indicating projected involvement of industrial researchers from Participants.

I. Management Plan

Center Leadership and Management: Present the management approach for the proposed Center. Discuss the role and responsibilities of the Center director and provide a plan for the administration and management of the Center. Describe the approach used to ensure that the relationships between contracting and affiliated universities are well defined and structured. As appropriate, provide a chart depicting the organizational structure of the Center.

Program Evolution: Describe the process that will be used in selecting and deselecting Center thrusts, projects, investigators or institutions such that maximum progress is made toward the Center mission in the midst of an ever-evolving environment of scientific and technological progress. In particular, identify the process that will be used to originate or maintain new frontier projects in the overall Center portfolio (either through current Center participants or additional participants). Describe the process for maintaining an up-to-date understanding of all significant technology barriers within a Center's area of focus.

Research Personnel: Provide an overview of the team and their backgrounds relevant to the proposed Center's goals. Describe the qualifications of the team for conceiving, demonstrating, and evaluating revolutionary options. As appropriate, provide evidence, other than biographical, of pioneering and innovative contributions by Center investigators in relevant fields of research.

Facilities and Research Equipment: Describe the facilities and research equipment currently available to the proposed Center, and those to be added with the establishment of the Center. Justify major items of equipment to be purchased in the context of setting up the Center. Describe the administrative arrangements and physical logistics for use of all major equipment by Center personnel. For equipment not purchased with Center funds, state the terms under which access by the proposed Center will be maintained.

Accounting Support: Provide information on the management method to be used to provide support to projects, and the strategy for gaining support beyond that provided by MARCO and DARPA through this award.

Role of Center within the Institution(s): Discuss the role of the proposed Center and the key factors affecting its integration into the structure and function of the institutions involved. Provide information on the relationship of the management of the Center to the management of participating departments. In particular, discuss how participation in the activities of the proposed Center will be considered in reward, promotions and other personnel decisions for institutional employees, as well as the role that the Center Director will have in such decisions.

J. Key Personnel (not included in page count)

Provide a list of the Key Personnel participating in the proposed Center. The list should identify disciplines and affiliations (e.g., departmental, institutional, industrial, etc.). Biographical information on Key Personnel should be provided.

VOLUME II, COST PROPOSAL – (No page limit)

A. Cover sheet to include: (1) RA number; (2) Center Technical area; (3) Lead Organization Submitting proposal; (4) Other Academic Institutions participating in the proposed Center; (5) Lead Organization's reference number (if any); (6) Other non-academic team members (if applicable) and type of business for each; (7) Proposal title; (8) Technical point of contact to include: salutation, last name, first name, street address, city, state, zip code, telephone, fax (if available), and electronic mail (if available); (9) Administrative point of contact to include: salutation, last name, first name, street address, city, state, zip code, telephone, fax (if available), and electronic mail (if available); and (10) total funds requested from the Consortium and the amount of cost-share from other sources (if any).

B. Detailed Cost Breakdown

Provide a summary cost chart which includes cost to per task, per team member, per year, with totals for each task and each team member for the program. Provide a detailed cost breakdown to include: (1) total program cost broken down by major cost items (direct labor, subcontracts, materials, other direct costs, overhead charges, etc.) and further broken down by year; (2) major program tasks by year; (3) an itemization for subcontracts and equipment purchases; (4) an itemization of any information technology (IT) purchases; (5) a summary of projected funding requirements by month; and (6) the source, nature, and amount of any cost-sharing. Where the effort consists of multiple portions which could reasonably be partitioned for purposes of funding, these should be identified as options with separate cost estimates for each.

C. Handling of Intellectual Property

Describe treatment of intellectual property under the proposed Center. Indicate the degree to which intellectual property rights will match the principles outlined above. Identify any known, perceived or anticipated issues in the handling of intellectual property.

D. Supporting Cost and Pricing Information

Include other supporting cost and pricing information in sufficient detail to substantiate the summary cost estimates. Include a description of the method used to estimate costs and supporting documentation.

NOTIFICATION

This notice, in conjunction with the RA S201209 constitutes the total Research Announcement. No additional information is available, nor will a formal Request for Proposals (RFP) or other solicitation regarding this announcement be issued. Requests for the same will be disregarded. The Consortium reserves the right to select for award all, some, or none of the proposals received. All responsible sources capable of satisfying the FCRP needs may submit a white paper, which shall be considered by the Consortium. Historically Black Colleges and Universities (HBCU) and Minority Institutions (MI) are encouraged to submit white papers and join others in submitting white papers; however, no portion of this RA will be set aside for HBCU and MI participation.

Any objections to the terms of this Research Announcement or the **RA S201209 Proposer Information Pamphlet** must be presented in writing within fifteen (15) calendar days of the online publication of this RA. Any objections to the conduct of receipt, evaluation or award of contract must be presented in writing within the (10) calendar days of the date the objector knows or should have known the basis for its objection. Objections must be provided in letter format, clearly stating that it is an objection or protest to this RA or to the conduct of evaluation or award of a contract, and providing a clearly detailed factual statement of the basis for objection. Objections must be received at the address stated above for delivery of proposals within the times indicated in order to be considered. Other administrative correspondence and questions related to this solicitation, including requests for information on how to submit a white paper or proposal, should be directed to: fcrp-s201209info@src.org.