STARnet Call for Research
Revolutionary Interconnect Technology Solutions
For End-of-The-Roadmap and Beyond CMOS
Needs Document

I. The Problem:

There is a major bottleneck, which appears to be insurmountable, with metal interconnects below dimensions of 10-15 nm in width (20nm –30nm pitch, width+space) due to the non-linear increase that is occurring in resistance. There will be a need in the future to realize CMOS integrated circuits with interconnect (conductor) width dimensions equal to and below 5 nm. In addition to this bottleneck in interconnect (conductor) resistance per unit length, there is limited opportunity for reduction in effective dielectric constant for the insulator surrounding the metal interconnect, e.g. below 1.5 to 1.8.

Thus the RC delay of interconnects for logic is now the major contributing factor that is limiting improvements in computation performance and reductions in energy. It will be the limitation to computation performance improvement and power reduction in the future.

Another interconnect challenge is that thermal solutions for interconnects are required as self-heating occurs when power dissipation is increased with the increase in interconnect resistance and the integration density.

Interconnect scaling also limits the opportunity transistors have of realizing monolithic RF mixed signal circuits at RF frequencies >100GHz. Here the requirements of low loss propagation of RF signals with the required signal integrity and noise isolation are key.

As the research for a beyond CMOS device makes progress, there is the question of what will be the delay and energy of the interconnect solution if a new computational variables such as spin is used.

II. The Need: A Revolutionary Solution to the Interconnect Bottleneck in CMOS and Mixed Technology Monolithic ICs.

The main source of resistance (and signal attenuation/loss) in scaled metal wires is due to edge/surface/dielectric interface-caused scattering and grain boundary-caused scattering which prohibit the wire from seeing its intrinsic bulk resistivity. A means to eliminate the components of inelastic scattering of metals at nanoscale dimensions and approach ballistic transport is needed. STARnet is interested in revolutionary research to address this challenge that can apply to: charge transport for charge-based logic devices, propagation of mmWave/THz signals (EM waves) and coherent electron spin transport for spin-based logic devices. Solutions must be compatible with homogeneously and heterogeneously integrated (2Dand 3D) ICs.

The scope of this research request for white papers could include but is not limited to the following;

Scope - Focus I:

a) For “short” length interconnects (<700nm long, <7 nm wide – within standard cell interconnect) and “near-short” length interconnect (<15 □m long, <15 nm wide – between standard cell interconnect):
    i. Physics in metals, metal-metalloid alloys and liners that can realize scattering mitigation or improve resistivity scaling with critical dimension or thin/no liner options (e.g. effect of texture, grain boundary dopants).

ii. High Density of State (DOS) materials with low scattering or near ballistic transport (e.g. graphene clad metals).
iii. Physics and materials science that can support high-density 2-D electron gas creation and ballistic propagation at the interface between metals and oxides, or between two oxides.
iv. Physics that can support spin polarized 2-D electron gas creation and propagation at the interface between metals and oxides, or between oxides, e.g. by way of the Rashba effect.
v. Ultra scaled vias and contacts: low resistance via, or contact at 10nm dimension or less with high aspect ratios (>10).
vi. Dielectric materials that can enable negative differential capacitance, or low permittivity over the frequency range of 10MHz - 10 GHz.
vii. Relevant short distance interconnect based upon low loss plasmonics that can interface to either an electronic or a spintronic logic device.
viii. Low thermal conductivity dielectrics or phase change thermal materials.

Scope - Focus II:

a) For semi-global interconnect and global across chip interconnect (0.05-20mm long, <100 nm wide):
   i. Materials/structures to support low loss propagation of mmWave/THz signals (EM waves),
   ii. Dielectrics /structures to maintain signal integrity (signal isolation) in highly (2D and 3D) integrated mixed signal/mixed technology (digital, RF) systems.
   iii. Materials/structures to support for high current density
b) For global across chip interconnect (0.05-20mm long, <100 nm wide):
   i. Energy efficient, high bandwidth, high isolation monolithic or 3D analog/Terahertz RF sources, waveguide and detectors, including terahertz passives for Terahertz transceivers.
   ii. Energy efficient, high bandwidth, monolithic or 3D integration of Optical sources, waveguides and detectors, including high bandwidth density Optical-Electrical transceivers. ~100 nm scale sub 10 fJ/bit E-O and O-E transduction elements for global across chip and off-chip data propagation (including optical source considerations).
   iii. Scalable transducers for interfacing electrical/spin/optical functional units to electrical/spin/optical interconnect (e.g. optical to spin transduction via angular momentum transfer, spin to charge and charge to spin via spin orbit effects).
   iv. Long range spin interconnect and transduction solutions based on extremely long spin diffusion lengths in 2D metals, magnon interconnects, magnon condensates.
   v. Interconnects based on electrical solitons.

Modeling and simulation suitable to validate applicable theory or to drive experimental exploration within the scope of this call will be accepted.

The white papers must clearly identify the energy/bit, linear bandwidth density (Bandwidth/pitch), areal bandwidth density (Bandwidth/area) and the potential of the proposed solutions.

This request for white papers is on identifying and demonstrating the potentially revolutionary but high reward opportunities based on physics for new materials to address the interconnect bottleneck.