STARnet Call for Research
Memory Vectors and RF Circuits
Needs Document

Memory Vectors:
Two device technologies still dominate large-scale memory, NAND Flash and DRAM. Each has well-known shortcomings like the relatively slow speed write of NAND and the volatility of DRAM. Currently explored, new, memory device technologies have fallen short on delivering a competitive package of performance metrics to compete with these mainstream memories. It is thus highly desirable to find alternate memory technologies or novel methods to surmount the shortcoming of studied memory systems such that they can become competitive technologies. Memory architectures that enhance memory array scaling, such as cross-point (aka x-point) cells, also require new methods for providing access (charge or other state variable input) to the cell. In-line (2-termnial) access devices with attributes necessary for switching and sensing of new memory technologies go hand-in-hand with this call. Additionally, new memory and scaling of current technologies generally require new and more sensitive sensing or state detection methods and architectures for effective implementation.

- New stand-alone capable memory devices, especially those that exploit alternate state variable, e.g. spin, material phase, exciton, etc.
- Methodologies to vastly improve properties of currently studied memory systems, e.g. lower programming current, high on/off ratio, size and energy scaling, long cycling and retention, etc.
- Advanced, two-terminal, bidirectional select devices with properties suitable to access particular, or multiple, memory cell technologies.
- Advanced sensing schemes and/or architectures for low resistance and low voltage (small signal) memory cells

This call is not meant to augment projects currently funded within STARnet, but rather to seed new and hopefully "revolutionary" ideas in memory technology. Ultimately scaled devices are targeted at <20 nm, with consideration toward multi-bit potential, such that maximum number of bits per unit volume may be achieved. Targeted memory materials and select devices without a clear path to functionality at >100 C will not be considered.

Architectures for Many-core Computing Systems Enabled by Extremely-scaled Memory Technologies

Emerging memory technologies such as PCM, RRAM, STTRAM (for example the recently announced 3D XPoint memory) as well as new ways to integrate traditional memories like DRAM promise to radically re-shape the traditional memory hierarchy. One example of this is the integration of PCM into the platform, with latencies in the 1 us range. The latency of PCM is two orders of magnitude faster than NAND, i.e. far too low to justify the high latency of OS managed paging. However, with latency 10 times higher than traditional DRAM and the need to minimize writes, the careful allocation of DRAM resources remains critical. These constraints motivate expanded hardware control over the movement of data between emerging memories and DRAM. This, in turn, motivates a re-examination of prefetching and replacement algorithms in the context of heterogeneous memory systems with large integrated memories (STTRAM, RRAM, DRAM) backed by a much larger, slower memory.

Research vectors:
- Integration: The most efficient memory hierarchy supporting 1GB/mm^2 density and TBytes of local memory
- Performance: Memory hierarchies for extremely scaled local memories with 1TB/s bandwidth; sensitivity of system performance to memory parameters across workloads
- Compute-in-memory: Exploration of filtering and/or preprocessing functions that could be performed close to the memory
- Power: Power-efficient memory architecture studies for extremely large datasets (data center in a box)
- Resilience: Memory architectures for resilience (RAID in a package)
- Coherence: Power-efficient memory schemes for coherent computing

RF and Analog Circuits

- **Verification and Self-Healing Methods for Analog/RF Modules.** Develop new methods and corresponding circuit design demonstrations for efficient analog/RF verification and self-healing. Extend Statistic Element Selection (SES) to exploit large-scale random variations that are expected for future technologies to provide a wide tuning range with fine-tuning resolution. Initiate techniques for formal verification of self-healing loop stability and intended module functionality. Demonstrate success via circuit level ADCs and a module-level wireless transceiver.
- **Self-Synthesizing, Adaptable, Reconfigurable, Mixed-signal Systems.** Develop a programmable, adaptable, reconfigurable, mixed-signal ADC/DAC/filter architecture for nanometer CMOS. For example using a flexible, sea-of-analog cells approach. This architecture should configurable to perform filtering, analog-to-digital conversion or digital-to-analog conversion. On-chip self-optimization and system configuration to meet performance objectives. This work should be targeted at emerging processes with poor analog performance and reliability and extreme variability, but also applicable to enhancing the performance and behavior of circuits in analog friendly processes beyond what can be expected without these techniques.