

Ferroelectric Materials and Devices: AC Impedance Characterization, BEOL FE-TFTs for Analog AI Accelerators

Jesús A. del Alamo

with Taekyong Kim, Yanjie Shao, John Huang, Elham Borujeny, Tyra Espedal, Jorge Navarro,
and Dimitri Antoniadis

Massachusetts Institute of Technology

SRC Exploring Frontiers:

Ferroelectric Materials and Devices Workshop – Unveiling Challenges and Opportunities

Sponsorship: SRC LMD, MIT AI Hardware Program



MIT AI Hardware Program



Workshop discussion topics

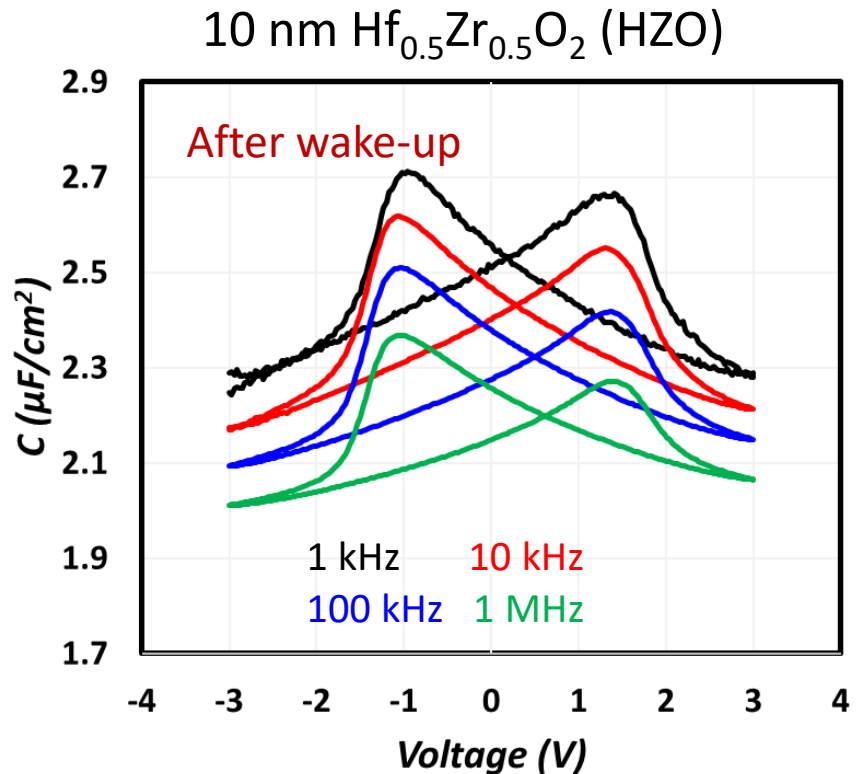
2020-LM-3000

2024-LM-3237

2023-LMD 3140

1. What innovations are required for improving endurance?
2. Metrology needs in characterizing FE material defects with respect to fatigue, wakeup and dielectric breakdown?
3. What is the roadmap towards developing low voltage FE transistors?
4. FE thin films for tunnel junction devices – Three years from now?

AC Impedance characterization: C-V and G-V



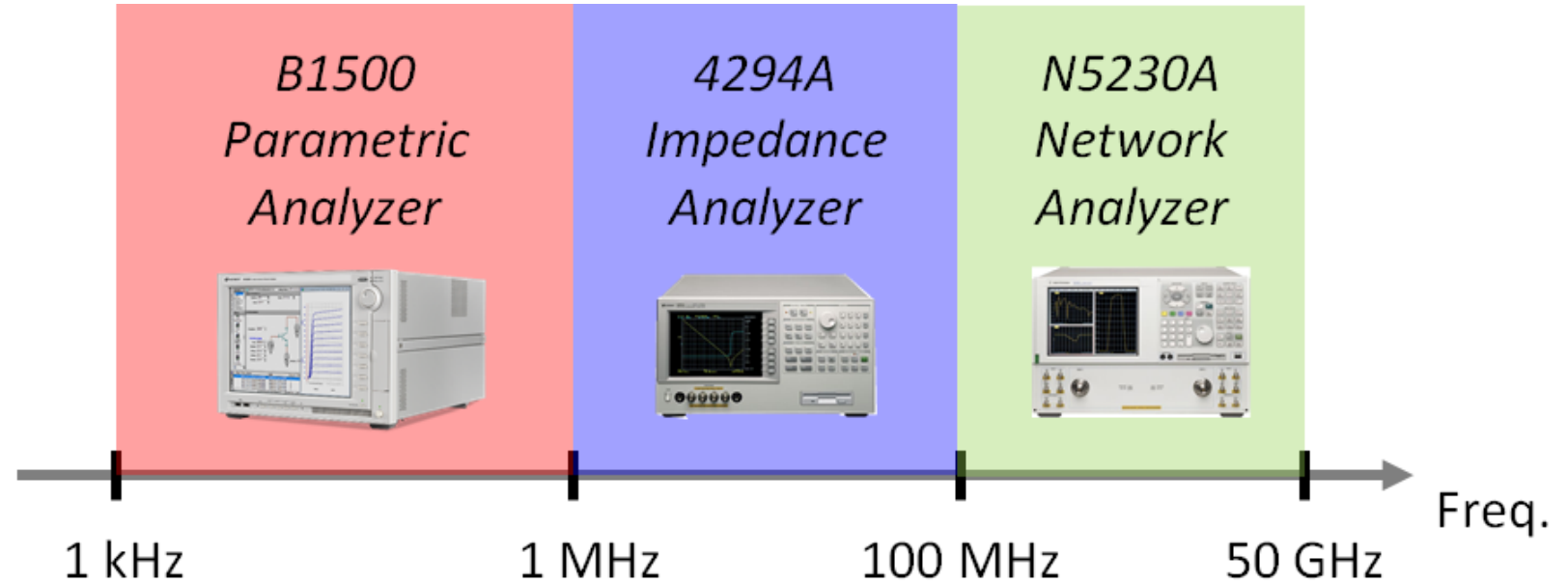
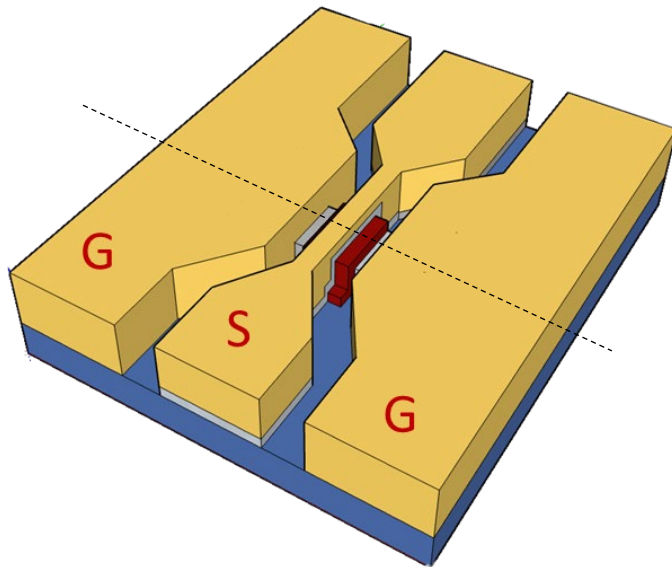
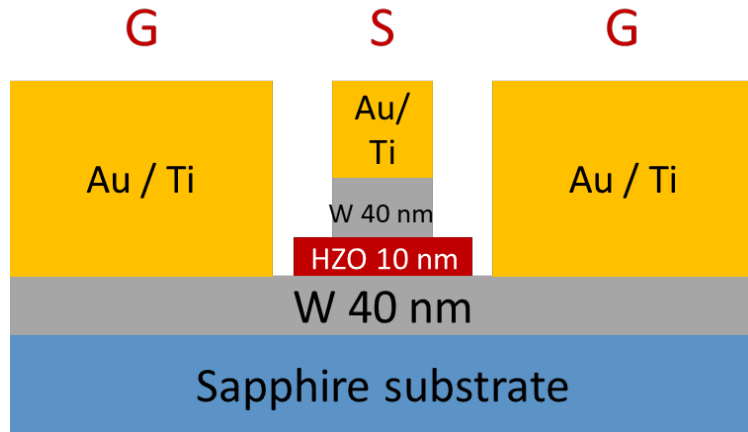
C-V characteristics:

- “Butterfly” shape
- Asymmetric
- Frequency dispersion

Our goals:

1. Accurate AC impedance characterization
2. Physics of C-V and G-V characteristics
3. Application to understand endurance, imprint, wake up, fatigue, etc.

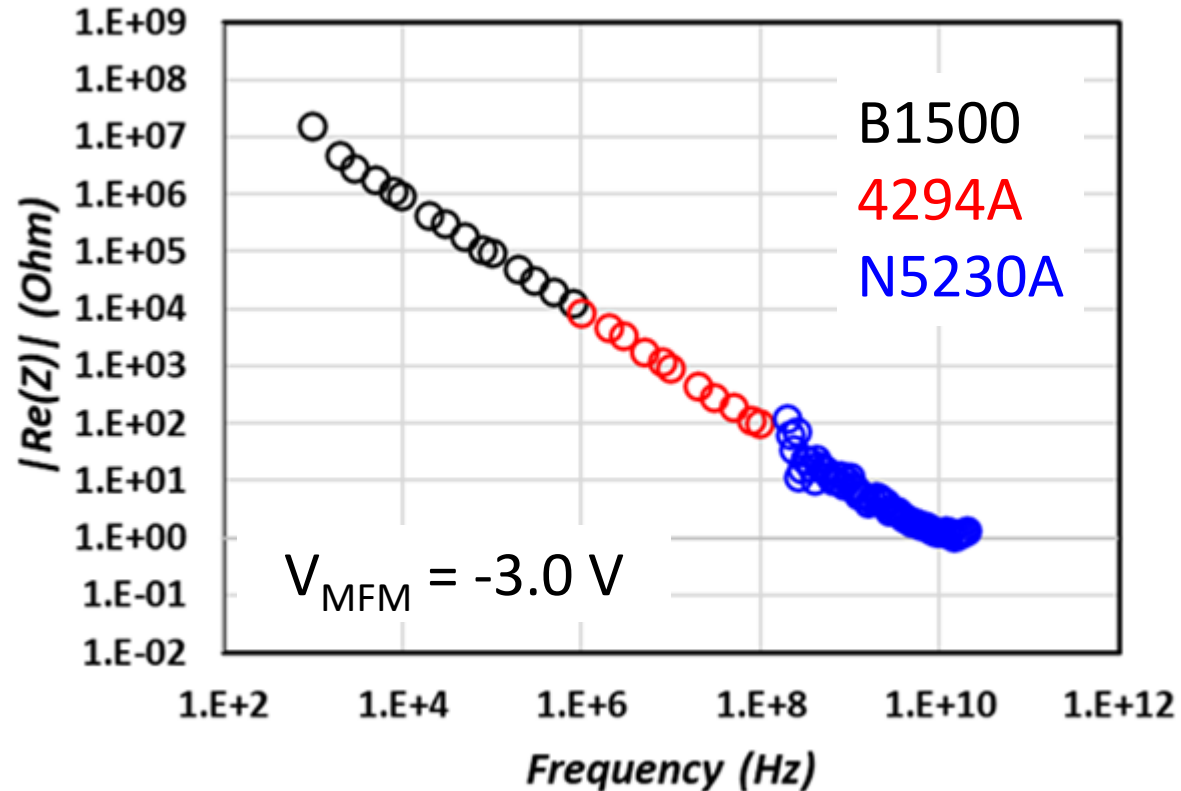
Experimental



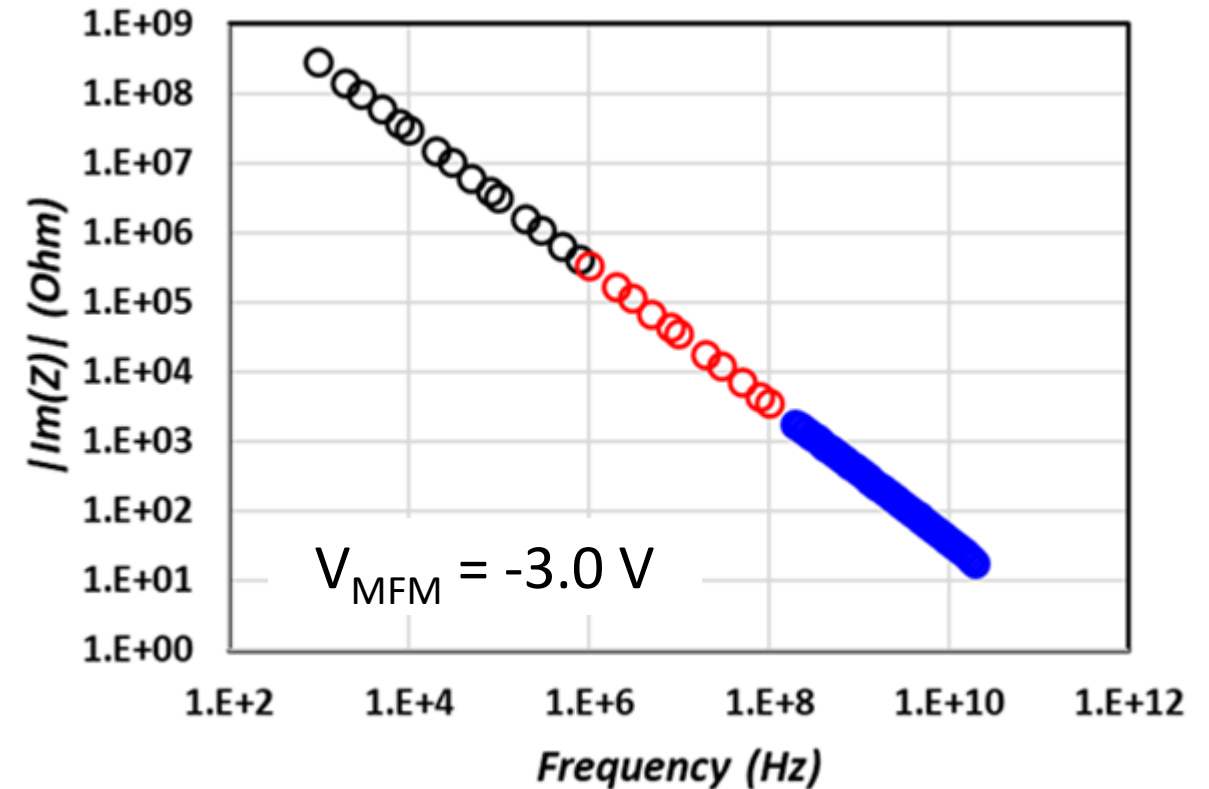
- MFM structure on low-loss coplanar waveguide
- Characterization from 1 kHz to 10 GHz
- Accurate calibration and de-embedding of parasitics

Intrinsic impedance measurements

$|\text{Re}(Z)|$

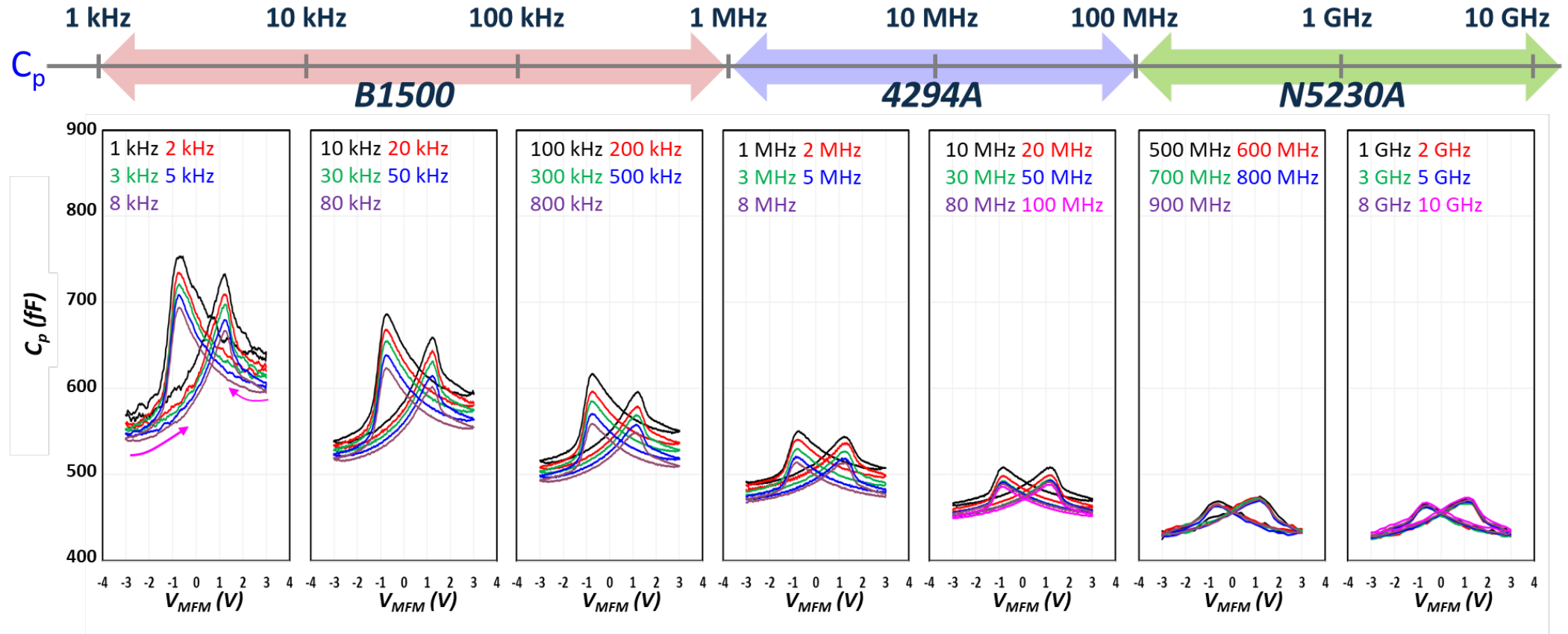
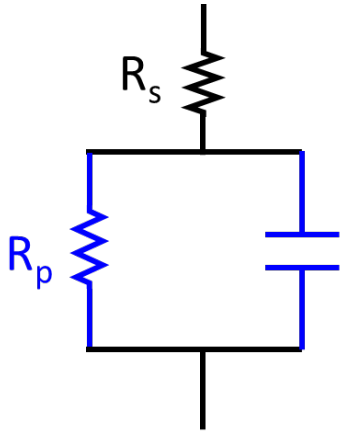


$|\text{Im}(Z)|$



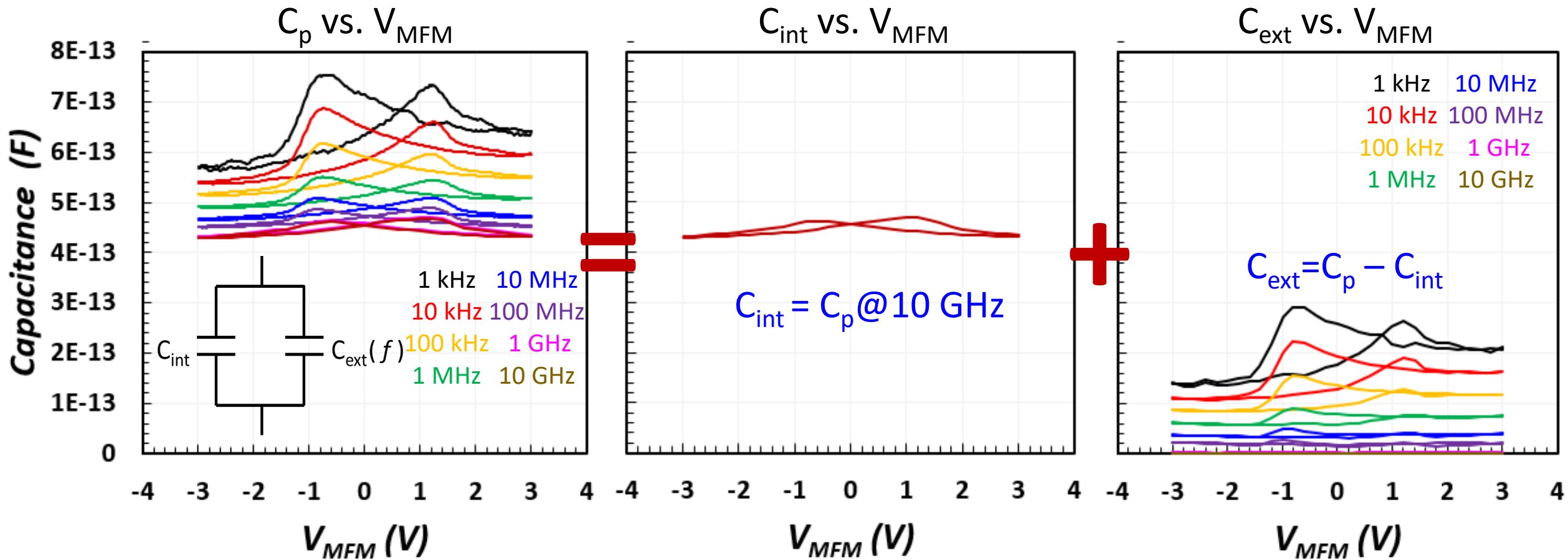
Accurate stitching at frequency boundaries

C_p : bias and frequency dependence



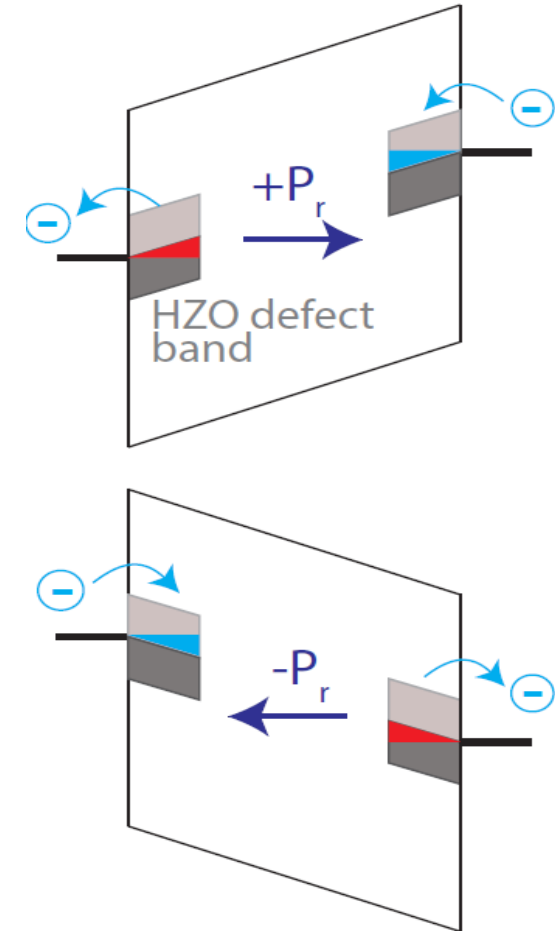
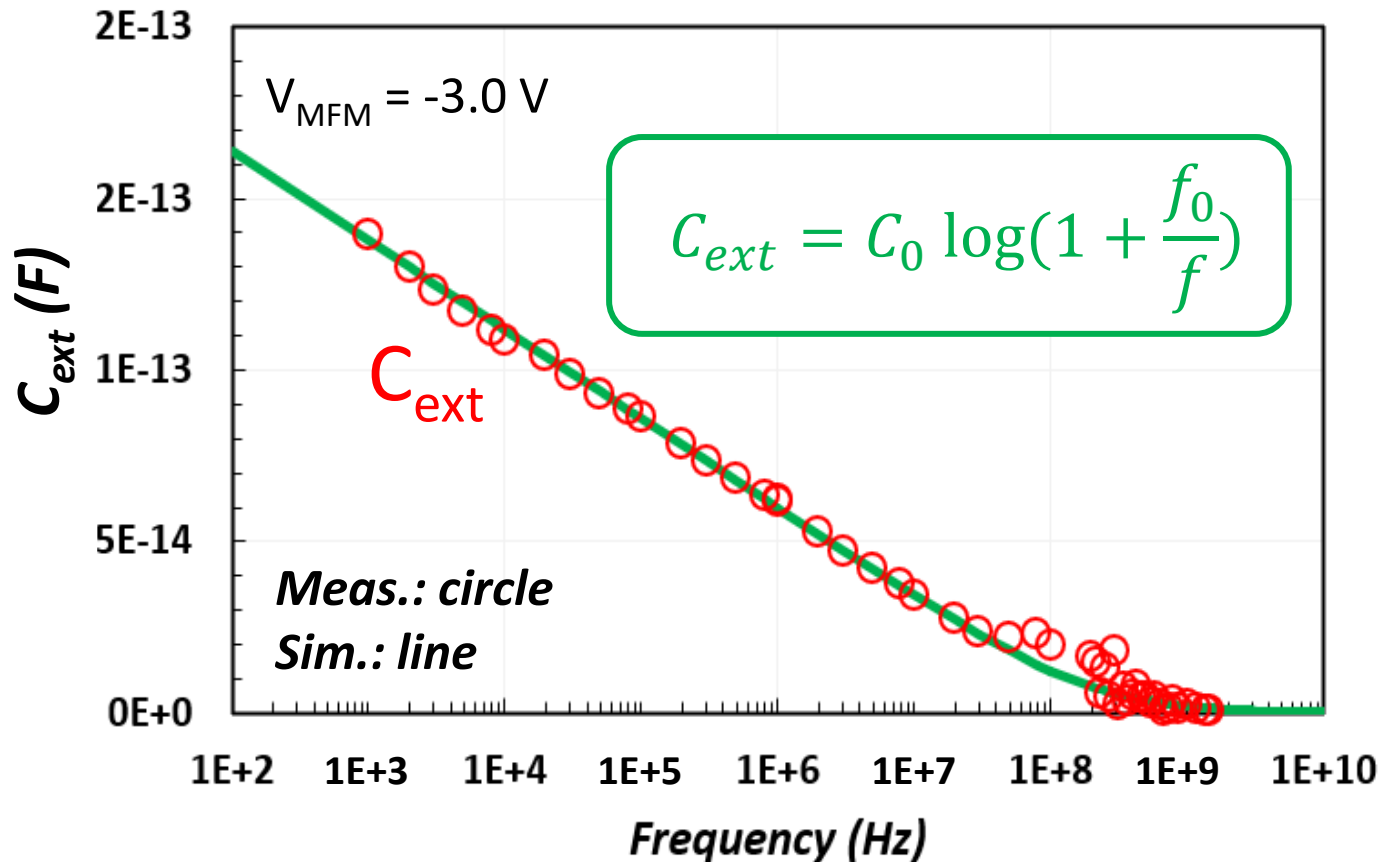
- V-dependent butterfly behavior persist in GHz regime
- $f \uparrow \rightarrow C_p \downarrow$ until about 1 GHz, then f independent

C_p interpretation: $C_p(f) = C_{int} + C_{ext}(f)$



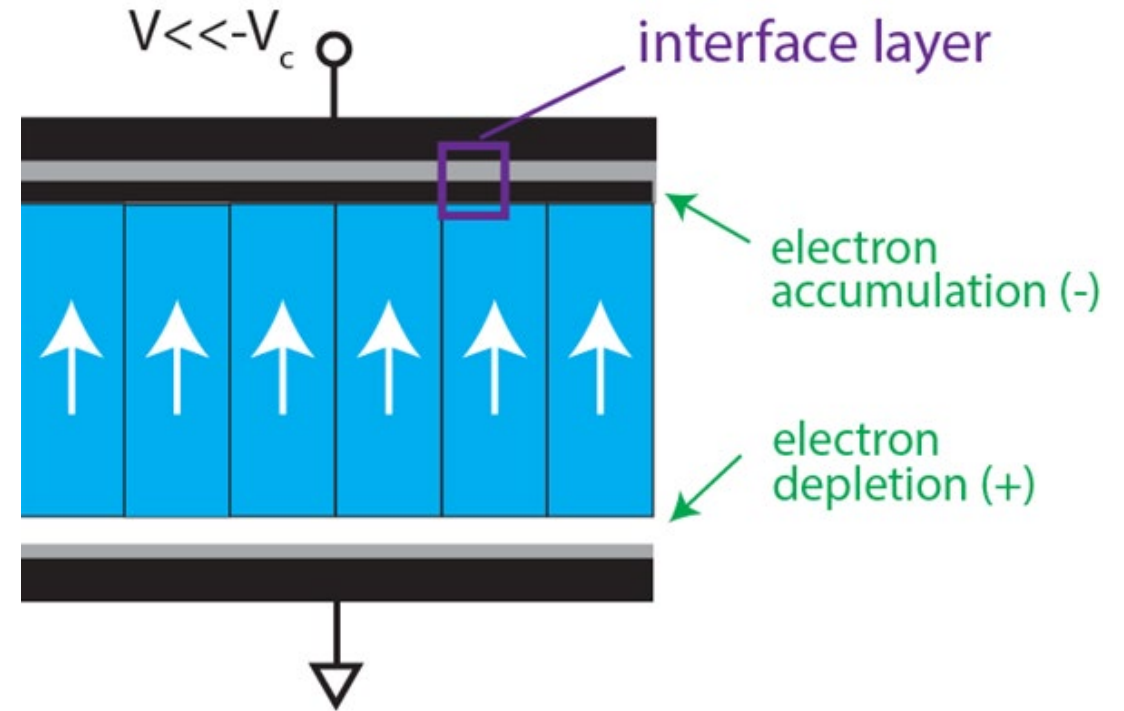
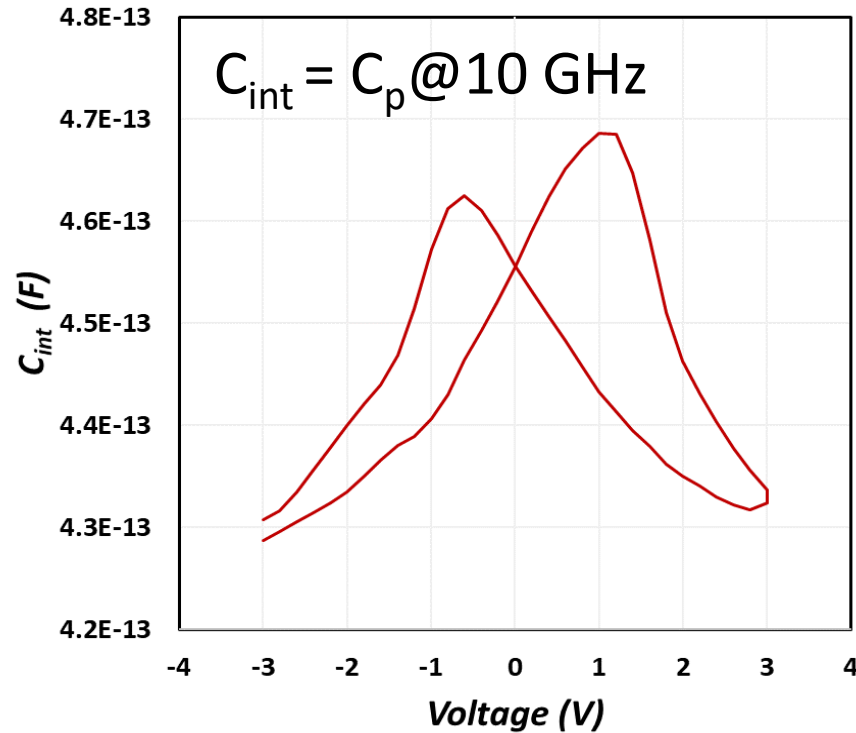
- *Intrinsic* C (C_{int}): butterfly shape, frequency independent
- *Extrinsic* C (C_{ext}): butterfly shape; $f \uparrow \rightarrow C_{ext} \downarrow$

Physics of frequency-dependent C_{ext}



- $C_{ext}(f)$ well described by logarithmic decay function with $f_0 \sim 0.1 \text{ GHz}$
- Consistent with e^- trapping in HfO_2 border traps (Cai, TED 2020; Johansson, TED 2013)

Physics of C_{int}

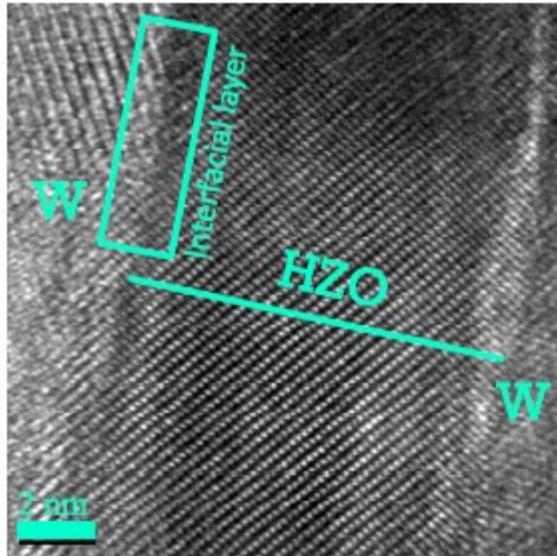


Hypothesis:

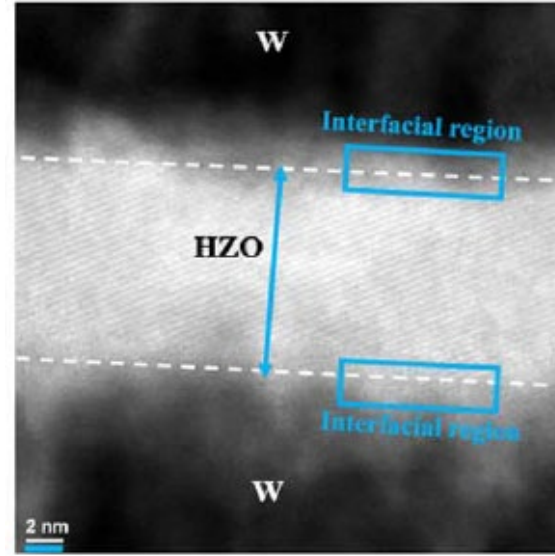
- Interfacial layers at M/F boundaries in good electrical contact with metal plates
- Charge at plates supported by electron depletion and accumulation at interfacial layers
- $C_{int} \approx 1/|Q|$

Nature of interfacial layer

Metal oxide at metal/HZO interface



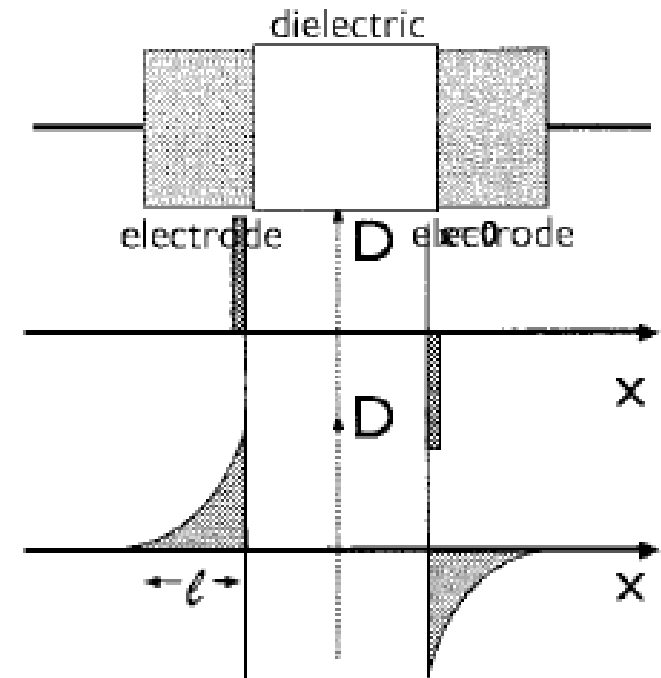
Kashir, AEM 2021



Yadav, Nanotech 2022

WO_x at interface

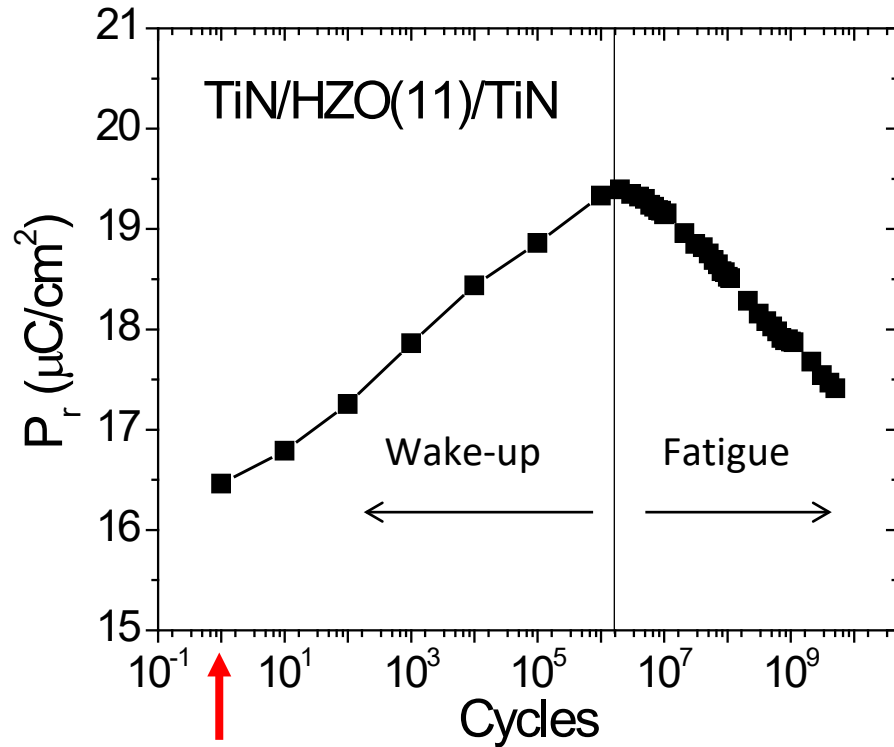
Electric field penetration into metal (finite screening length)



Black, TED 1999

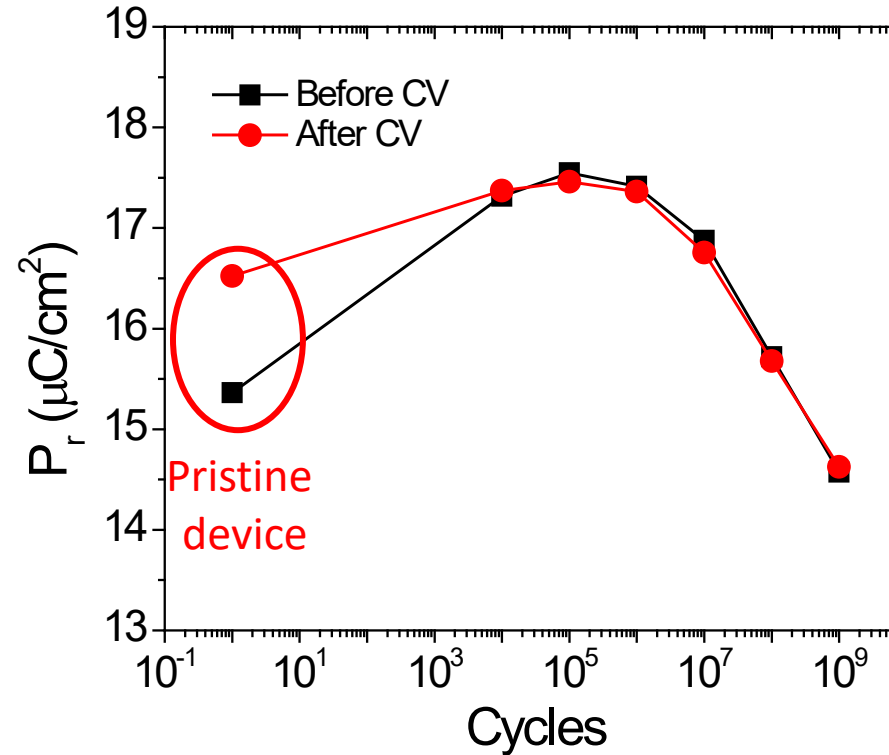
C-V study of wake-up and fatigue: evolution of P_r

Typical bipolar endurance experiment



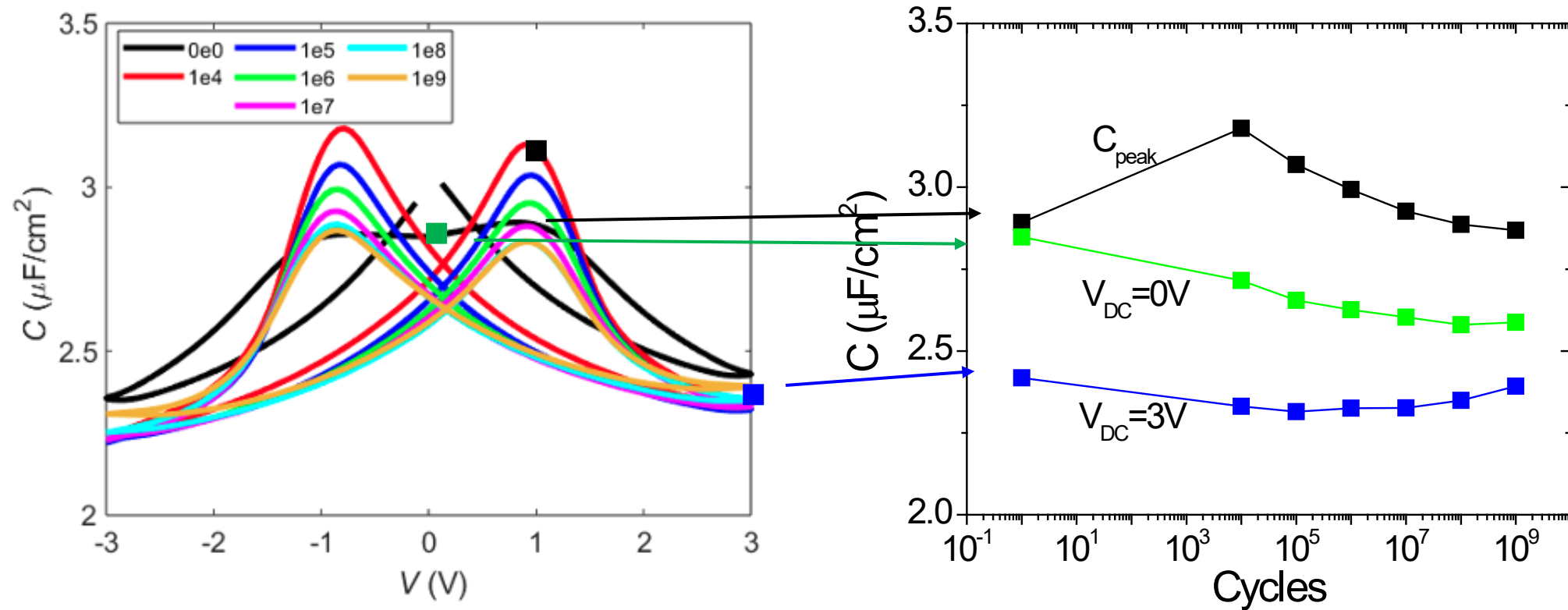
Virgin
device

Including CV



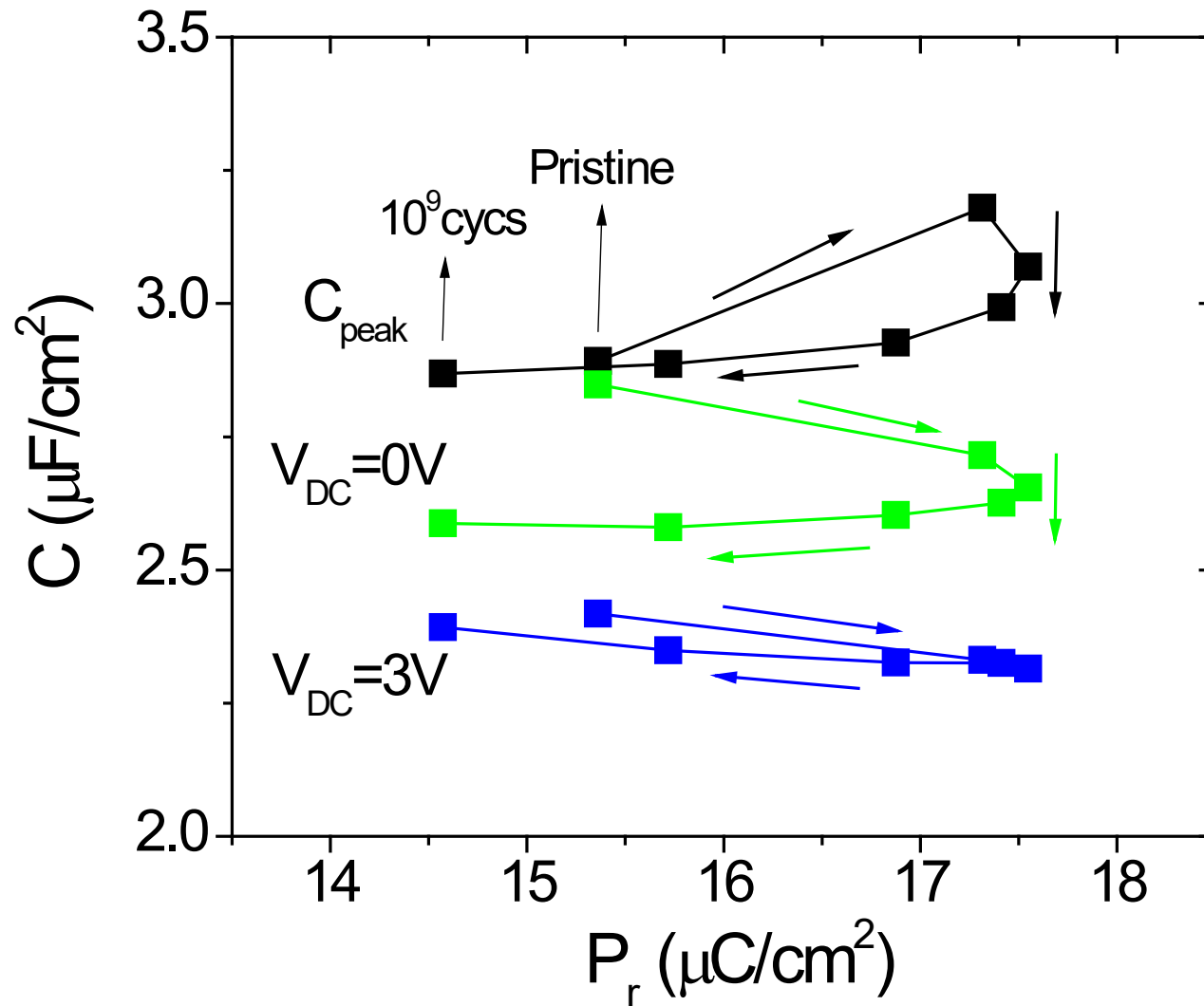
- CV speeds up wake up
- CV doesn't affect fatigue

C-V study of wake-up and fatigue: evolution of C



- C peak emerges during wake up
- $C(0\text{ V})$, C_{peak} and $C(+3\text{ V})$ fatigue in different ways

C-V study of wake-up and fatigue: correlation of C and P_r



C_{peak} :

- *increases* during wake up
- *decreases* during fatigue

$C(0\text{ V})$:

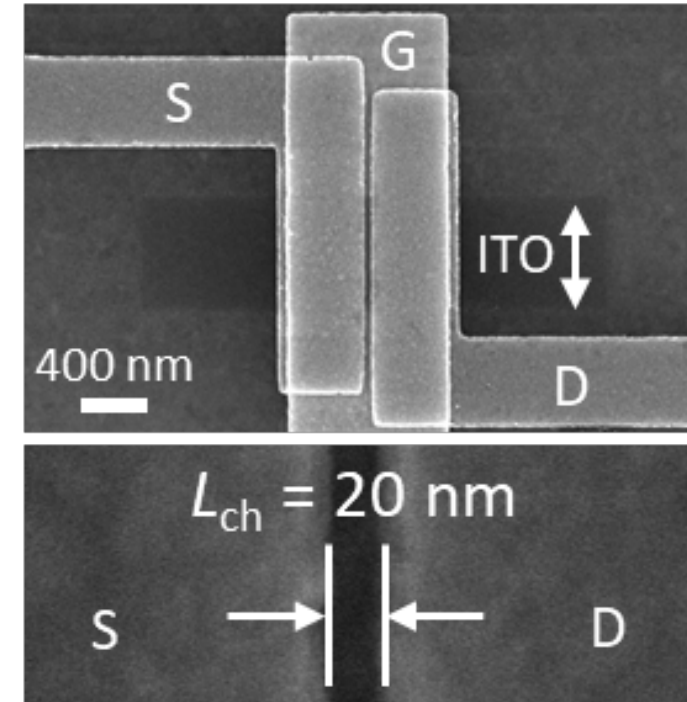
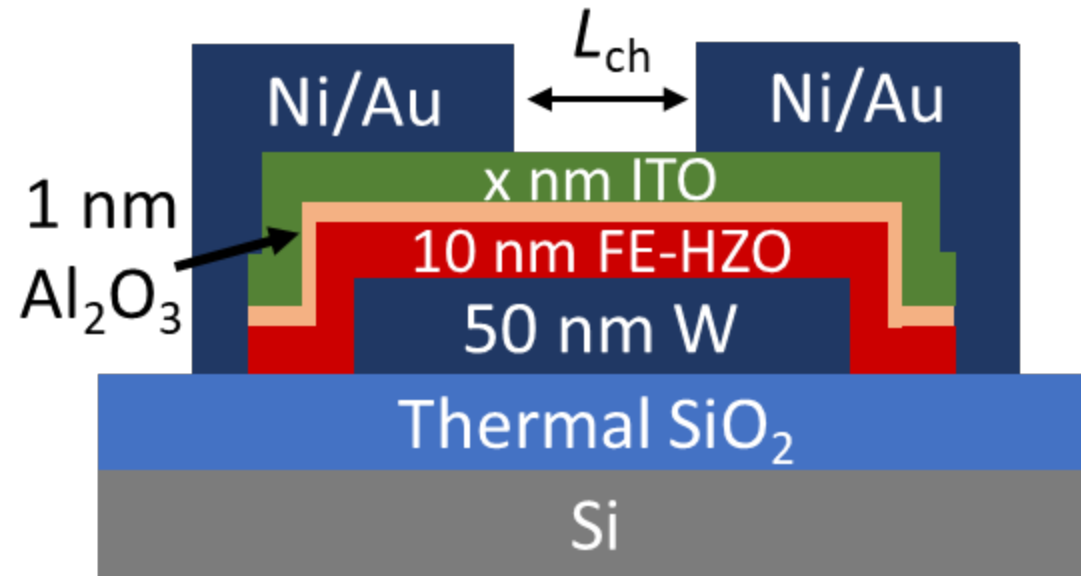
- *decreases* during wake up
- *stable* during fatigue

$C(+3\text{ V})$:

- *decreases* during wake up
- *increases* during fatigue

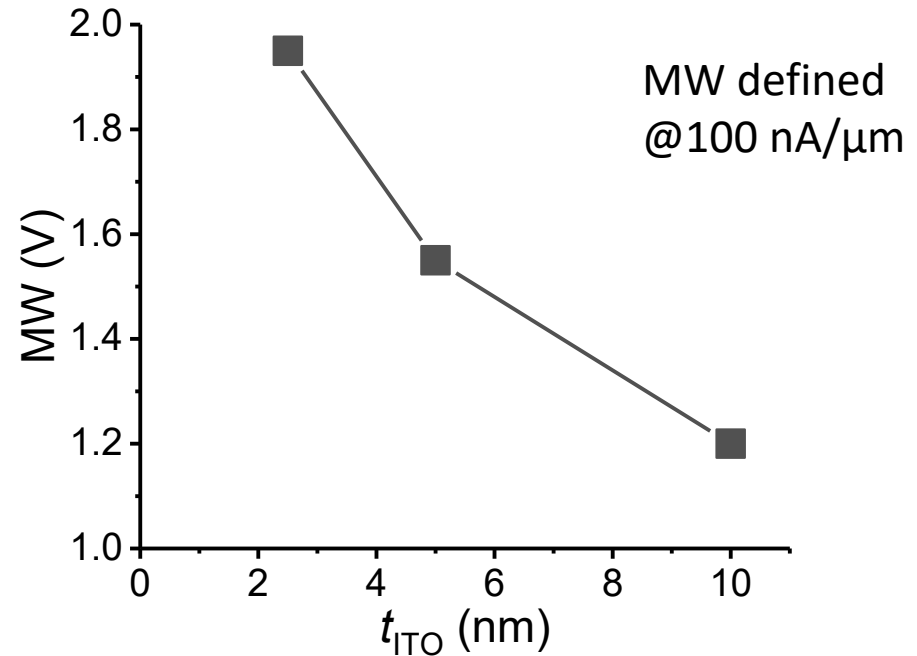
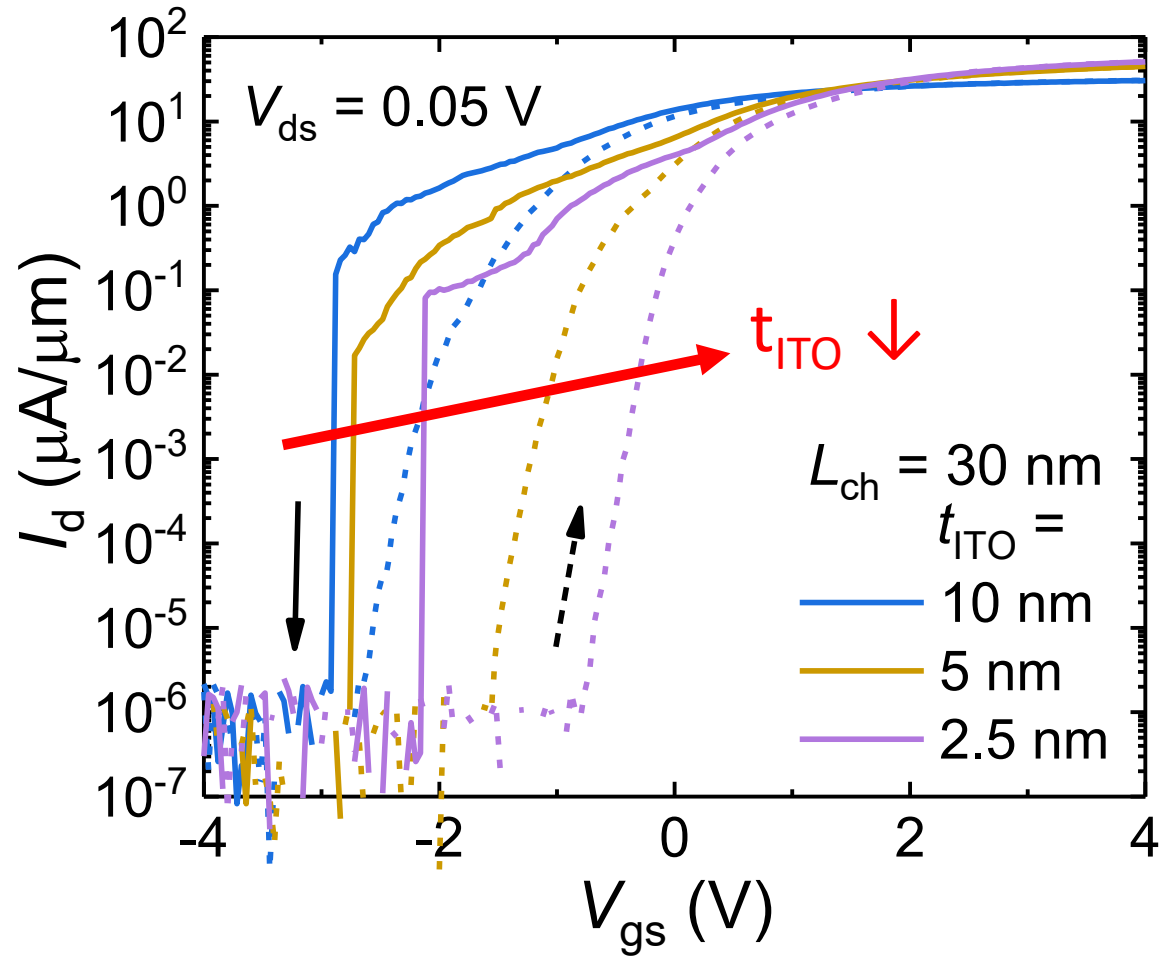
Next steps: Why??

Scaled BEOL FE-FETs with ITO channel



- Back-gate configuration with MFIS structure
- Path for low V operation: thin, highly doped channel → ITO
- BEOL-compatible thermal budget

Memory Window: ITO thickness scaling



Next steps:

- studying analog polarization switching
- endurance

ITO thickness $\downarrow \rightarrow$ MW \uparrow , $\Delta V_t > 0$