Introduction

This paper seeks to identify and characterize research needs in the basic physical sciences that are required to sustain the exponential progress in nanoelectronics. We believe that increased work in the physical sciences is essential to achieve ultimate limits for current integrated circuit technologies. Moreover, we believe that basic research is required to realize the opportunities for the creation of and transition to new nanoelectronic technologies that could offer unparalleled advances in device density and performance. For the first time, the 1999 International Technology Roadmap for Semiconductors (ITRS) recognized technical barriers having no known solutions that are on the five-to-ten year implementation horizon. It is our thesis that if these barriers are to be bridged, the knowledge base in the physical sciences must be enhanced. Herein, we give examples of areas where additional research is needed to retain the current pace of progress of the semiconductor industry. We also argue that increased research in the physical sciences can provide the basis for a continuation of the unprecedented economic growth of the information technologies by enabling the creation of radical new devices, processes, and systems whose performance may ultimately be superior to that achievable through technology scaling.

Each section of the paper is designed to describe basic research that is needed to enable ultimate CMOS and related electronic device technologies and that will support the creation of post evolutionary technologies. Section 1 of this paper focuses on the chemistry, physics, and design of functional nanoscale structures as it pertains to nanoelectronics and discusses areas where more complete understanding is needed; including interfaces, conductivity, doping, spin phenomena, and functional synergy in electronic materials. Section 2 is devoted to nanoscale materials as they relate to nanoelectronics, with emphases on nanoparticles, nanotubes, and characterization. Section 3 concentrates on nanoelectronic devices beyond CMOS and, in particular, discusses three possible classes of future devices. Section 4 provides an introductory treatment of nanoscale processing and focuses on self assembly and nanopatterning.

Background

The end of CMOS scaling is foreseeable, although the specific combination of factors that will end scaling is not known [1]. As industry moves through the two to three year technology generation cycles, the complexity of the processes is increasing and the demands on fabrication equipment performance are more strenuous. For example, in order to construct 25 nm devices, lithography tools are needed that operate beyond optical lithography limits. Fortunately, there are several technology options; however an extremely costly R&D effort is required to translate these technologies into production tools in about one decade. The performance of the scaled device in the 25 nm regime is itself problematical. The gate oxide has been aggressively scaled to enhance device performance. However, as the thickness of the gate approaches 1 nm through scaling, tunneling through the gate oxide creates unacceptably large off currents, dramatically increasing quiescent power consumption, and rendering the device impractical for analog applications due to unacceptable noise levels.

Limits also are evident for power supply voltage scaling; an approach that has been historically used to control power dissipation in high performance MOSFETS. The difficulty stems from the fact that the device current drive is roughly proportional to the difference between the power supply voltage and the threshold voltage. Unfortunately, if threshold voltage is decreased to accommodate supply voltage scaling, the off-current increases to unacceptable levels due to thermodynamic phenomena that are
relatively insensitive to device design choices. The scaling of power supply voltage is probably limited to about one volt in order to maintain a reasonable level of off current. Challenges also are prevalent in source/drain design tradeoffs. Heavily doped and deep source and drain regions are needed for low contact and low source/drain series resistance, however, shallow junctions are required to minimize short channel effects and source/drain capacitance.

We project that the evolution of the bulk planar CMOS device will plateau around the 25 nm technology node and that these devices will find their primary use in products for which performance is a tantamount consideration, and power consumption is not a primary driver. Analog applications of bulk CMOS technology likely will lag about two technology nodes behind high performance digital and may coexist on the same chip. Analog design may be facilitated by incorporation of SiGe bipolar devices on the same chip. At the limit, bulk CMOS devices may not suffice for low power applications.

There are several technology options that may extend CMOS technology beyond 25 nm. Various forms of dual gate devices have been proposed as possible options for CMOS. The use of dual gates can be shown to increase current drive for the transistor. However, the processes required to fabricate dual gate devices are very complex, demanding, for example, precise alignment of the gates. Other options that show a promise to extend CMOS technology include silicon-on-insulator technologies and cooled CMOS devices. It has been projected that by exercising some or all of these options, CMOS technologies might be extended to the 10 nm technology node [2].

Density scaling will gradually give way to functional scaling where the focus will be on the effective utilization of transistors and interconnects. This will probably add new functions to CMOS that will lead to hybrid technology integration at the die, package and board levels. New 3D structures will be needed at the nano, meso and macro levels to move information and heat. As we see it, the physical and chemical understanding necessary to reach the ultimate limits of CMOS technology also will provide the basis for inventing new technologies that will eventually supplement CMOS. Throughout the paper, we provide connections to possible future technologies.

What is not included

This paper does not undertake to examine the role of system architecture on the direction of evolution of CMOS or emerging technologies. We acknowledge that desired system functionality is an important driver for the development and application of new technologies. Conversely, a proposed new technology can only find application if system architectures can be designed to accommodate its limitations and to take advantage of its new features. Unfortunately, this synergy between possible future system needs and potential new technologies is difficult to create; primarily due to the broad range of disciplines involved. Furthermore, the complexity of modern electronic systems is such that the design enterprise cannot succeed without access to powerful tools that are cognizant of the characteristics and constraints of underlying technologies. We believe that effective application of new technologies mandates a commensurate effort in the development of CAD tools and test methodologies. However, the research to develop these tools must await the definition of reliable manifestation, e.g. standard models of the new technologies.
1. Chemistry and Physics of Nanoscale Structures

A. The Chemistry and Physics of Interfaces

On the Chemical Nature of Interfaces

One consequence of scaling is that the stack of layered materials that comprise electronic devices is becoming more like a continuum of interfaces than a stack of bulk thin films. Conventional methods for characterizing bulk properties of thin film materials and near micron scale devices may no longer suffice for nanoscale systems. Consider the conventional dark and bright field images of a recently fabricated nanoscale gate stack structure shown in Figure 1a. These images suggest layers of homogeneous thin films that might lend themselves to conventional bulk film analysis. For a layer to be considered a bulk thin film, the distribution of elements and properties should remain constant over some specified region.

Figure 1a) Bright and dark field images of a gate stacked structure and b) an EELS analysis of the cross sectional stoichiometries of elements throughout the gate stack structure [3].

However, an atomic scale analysis of this same structure shows that such films may no longer be considered as a collection of bulk materials. Figure 1b represents an atomic level map of elemental distributions through this same gate structure. It shows that the gate stack is made up of a series of gradient-like materials. The stack is a series of interfaces. The point is that one cannot represent components of this stack by their bulk properties since component properties vary throughout the stack.

Topology effects arising from surface(interface)-to-surface(interface) interactions now dominate the formation of potential barriers at interfaces. Consider Interface Ingomogeneity effects, that vary inversely with feature size. These include morphological and compositional inhomogeneities. Morphological inhomogeneities, typically manifested as atomic-scale roughness, are often responsible for increased leakage current in MOSFET gates. The fluctuations in elemental distribution in Figure 1b are expressions of compositional inhomogeneities. For finite dimensions and numbers of atoms, interface domains can not be represented as superpositions of a few homogeneous thin film regions. Instead, the challenge of characterizing this complex system requires accurate atomic level information about the three dimensional structure, geometry, and composition of atomic-scale interfaces.

Chemistry in the nano space is essentially surface and atomic level chemistry. An understanding of fundamental issues of the nanochemistry is important for manufacturing and operation of nanodevices. For example, the creation of specific surface sites for selective molecular attachment might be a promising approach for nanofabrication. Today, similar ideas are already exploited for gene analysis using conditioned silicon devices.
Discovery and innovation are needed to provide fundamental insights into the atomic level chemistry, architecture, and novel properties of these nanoscale materials, devices, and systems.

**Interface Physics**

There are five generic material interfaces whose operation is fundamental to semiconductor device operation. These are: (1) metal-semiconductor interfaces; (2) pn-junction (doping interfaces); (3) heterojunctions; (4) semiconductor-insulator interfaces, and (5) metal-insulator interfaces [4]. Most of these basic interfaces can be found in a MOSFET structure as shown in Fig. 2. Understanding and management of interfaces properties is most important both for nano MOSFET research and for alternative nanoelectronic structures and devices.

The transition from infinite to finite dimension impacts several fundamental properties of semiconductor interfaces, such as surface dominance and interface inhomogeneity. Surface dominance results from the relative increase of surface area relative to volume as dimensions of a component decrease, as shown in Figure 3. For cube dimensions less than 3 nm, more than 50% of all atoms in the particle are surface atoms. In this case, the electronic properties of the system are determined by surface effects, rather than bulk effects. In practice, at these dimensions, material and device properties reflect the nature of unavoidable surface adsorbates and contaminants rather than “bulk” doping, structure etc. In other words, it is becoming increasingly difficult to define ‘intrinsic’ properties that are free and independent of environmental factors. Under conditions of surface dominance, the relative surface area, dopant-to-dopant distance, and device properties depend on the shape and geometry of the nanostructure.

Interfaces in nano MOSFET structures

There are several critical issues in the nano MOSFET research directly related to interfaces:

- **Gate dielectric materials**
  - What are the ultimate limits of SiO₂?
New materials are needed, such as: Al₂O₃, Ta₂O₅, TiO₂, HfO, ZrO, BST
Practically all alternative materials require an ultra-thin pad SiO₂ isolation layer. This is an area of urgent research today, but materials offering solutions for several technology generations remain elusive.

Interface layers
- manufacturing of atomically controlled interfaces
- Metrology methods are needed for the ultra-thin and novel composite layers, specifically: thickness, architecture, composition, and dimension measurements

- New gate electrode materials
- Advanced Gate Modeling
  "First principles" approach involving the thermodynamics of the gate materials as well as combinatorial chemical synthesis
- Surface cleaning, conditioning, and engineering
  This research need area represents the interface between patterning and surface engineering of nanomaterials. Challenges associated with surface cleaning and conditioning require a bottoms up, molecular level, surface chemistry approach to cleaning and engineering interface structures.
- Silicon Resonant Tunnelling Devices (RTD) for MOSFET circuits
  An ideal RTD in the Si system would use SiO₂ barriers with standard Si processing. For useful tunneling currents, however, this scheme requires and oxide thickness of about 1 to 2 nm without pinholes or defects. Such an oxide, in application to RTDs is presently difficult to obtain and so most Si-based RTDs have used Si/SiGe heterolayers.

Research vectors:
- Develop a fundamental understanding of interface architectures that enable contact engineering for nanoelectronic devices based on the physics and chemistry of interfaces
- Explore transport properties in nanosystems, where interface properties dominate
- Correlate atomic and molecular level structures with mechanical properties of interfaces, e.g. interface stress and adhesion properties
- Establish quantitative relationships between interacting environmental factors and the influences of local functional groups (e.g. surface adsorbates) with the electronic properties of nanostructures
- Create predictive models of geometry-dependent properties of nanostructures
- Understand the relationships between the number of atoms and specified properties of interfaces. For example, how does a given property evolve as the number of atoms on a substrate transitions from an adsorbate to a monolayer to a thin film and, finally, to a bulk material?

B. Conductivity at small dimensions

Ultimately, material conductivity must be comprehended at molecular dimensions. Today’s generation of emerging chemists, materials scientists, physicists, and engineers have at their disposal new tools that offer unprecedented opportunities for probing and manipulating atoms, functional groups, molecules, and nanoscale structures, such as rational design tools based on structure-activity relationships and molecular dynamics. There are several levels in this problem classified according the scale. Mesoscopic wires with spatial dimensions (i.e. width, diameter) of 10-100 nm represent the 1st level. Such wires will probably be used for interconnects in future generations of ICs. Some of the problems here still can be treated with “macro” physics, e.g. metallurgical aspects arising from the grain size – dimensions relationships, corrosion, electromigration, current carrying capacity etc. As feature sizes approached 10 nm, several new effects will determine conductivity. The most important effects are the surface effects described in section 1A, and quantum conductance. Surface effects primarily imply dependence of conductivity of a mesoscopic wire on surrounding materials, impurities, surface inhomogenities etc.
Conductivity at small dimensions is usually described in terms of quantum conductance theory that gives value for fundamental conductivity (or resistivity) as $e^2/\pi \hbar$ or 77.5 $\mu$S (12.9 k\ resistor). Quantum conductance theory describes behavior of the quantum point contacts or short conductors, including the MOSFET channels, and is becoming an important consideration with scaling.

The second level in the sequence of decreasing conductor dimensions is represented by molecular wires that are formed, for example, by conjugated aromatic organic molecules (Fig. 4). The mechanism of electron transport through such a molecular chain is not well understood. Also, the optimum candidates for building the molecular wires need to be defined.

\[
Q = 0 \quad Q = -1 \quad Q = -2
\]

**Figure 4.** Orbital structure of the lowest unoccupied molecular orbital [LUMO] of a bridging molecule with one extra electron (conducting state), $Q = -1$, and two extra electrons (nonconducting state), $Q = -2$. The colored areas correspond to regions where electrons may flow [5].

At the smallest level, atomic wires that are linear chains of atoms were recently reported [6] (Fig. 5). However, no reliable measurements of electrical properties of such ‘ultimate’ wires have been performed at this point. Also, there is little understanding of how to treat such a one-dimensional structure – as individual atoms or as a system with collective properties?

**Fig. 5.** A high resolution image (15nm x 15 nm) of In lines on Si(001). Reprinted from [6], with kind permission from Kluwer Academic Publishers, copyright © 1997 Kluwer Academic Publishers.

Nanotubes, shown in Figure 6, serve as a potential bridge between atomic and micron scale wires. Their electronic properties depend on structural parameters such as diameter, helicity, location and type of defect, and functionality. An important feature of the CNT is that atoms are self-assembled to form a cylindrical structure, thus the position of each atom and geometry of the structure are well defined. The conductance mechanism through the nanotubes is not yet well understood.

A single molecule is probably the minimal amount of matter that could be used as a practical conductor. The first convincing demonstration of current passing through single molecule was reported in 1997 [7].
Both extensive experimental work to characterize various molecules and preparation of theoretical description of the conduction process are needed.

Fig. 6. Carbon nanotubes as nanowires [8]

Research vectors:
- Provide foundational understanding of conductivity in mesoscopic, molecular, and atomic wires
- Characterize electrical properties of atomic wires for different sets of substrate materials and different kinds of atoms in the wire
- Experimentally explore electron transport through single molecules and correlate results with theory.
- Conductivity quantization in nano MOSFET channels
- Ultimate metal-dielectric interconnects: manufacturing and reliability issues

C. Deterministic doping effects

Opportunities arising from single dopant control may have an impact similar to the revolution in electronic materials that resulted from the transition from polycrystalline to single-crystal materials. Standard MOSFET structures rely on the statistical distribution of large numbers of dopant atoms in the junction region to effect desired device properties. Within the next ten years, if scaling continues, semiconductor devices will require less than one hundred dopant atoms in the junction region. At that time, the number and location of each dopant atom will play an important role in determining device behavior. The challenge of precisely placing small numbers of dopants may represent a brick wall and could end conventional MOSFET scaling. However, if single dopant control can be achieved, opportunities for novel materials, structures, and functionality may arise.

Doping is used to gain control of electrophysical properties of a semiconductor and operational parameters of electronic devices by control of type, concentration and distribution of impurities (e.g. dopants). The distribution of dopants is traditionally treated as continuum in semiconductor physics that implies (a) the number of impurity atoms is small as compared to the total number of atoms in the semiconductor matrix; (b) the impurity atoms distribution is statistically uniform, while the position of an individual atom in the lattice is not defined, e.g. is random. The assumption of statistical uniformity requires large number of atoms where the mean distance between the neighboring impurity atoms is 

\[ L_{dd} \sim \sqrt[3]{\frac{1}{N_D}}, \]

where \( N_D \) is impurity concentration. The interdopant length \( L_{dd} \) is an important characteristic of nanoscale semiconductor structures.

* nano MOSFET research
To date, the appearance of discrete character of dopants arising from decreases of device size has been addressed in the literature only in regard to statistical device-to-device variations of transistor parameters due to decrease of numbers. There are however, more fundamental aspects of the problem directly related to the nature of semiconductors that are based on two fundamental ‘concentration’ parameters – intrinsic concentration and effective density of states.

From statistical physics, the error in estimate of the parameters of an n particle system varies as $1/\sqrt{n}$. Application of this rule to silicon nanostructures gives us inaccuracy (uncertainty) $\Delta P$ of a generalized parameter, $P$. Statistical physics predicts that beginning from 8 nm, the fluctuation in physical parameters of a silicon structure exceed 1%.

At this point however, it is not clear, how sensitive are various parameters (e.g. band gap, dielectric constant, mobility, activation energy etc) to the $\sqrt{n}$-effect. It is more or less clear for the case of doping (Fig. 7), which shows significant variation in parameters in the 1 nm regime.

**Single dopant effects**

As indicated above, in classic semiconductor physics, the doping of semiconductor materials has been treated only as a macroscopic phenomena level, e.g. for large number of atoms. From this statistical perspective, doping effects a shift of Fermi level in semiconductor. In this macroscopic case, the contribution of one extra dopant/electron to the system will not induce a significant change the potential distribution. However, the situation changes for very small volume semiconducting materials.

Consider a silicon cube with dimensions 100 nm x 100 nm x 100 nm. The addition of only one dopant atom, such as phosphorus, to the cube results in a donor concentration of $1 \times 10^{15}$ cm$^{-3}$. The resistivity of bulk silicon at this doping level is approximately 5 Ω-cm, which is much lower than the resistivity of $10^4 - 10^5$ Ω-cm for very pure undoped silicon. For smaller cube dimensions [d], the impact of single dopants on resistivity becomes even more pronounced. In this domain, effective doping concentrations increase and resistivities vary with decreasing device dimensions, as shown on Table I.

**Table I. “Single-dopant” parameters for sub-100 nm silicon structures.**

<table>
<thead>
<tr>
<th>d, nm</th>
<th>Number of Si atoms</th>
<th>Single-dopant concentration, cm$^{-3}$</th>
<th>Equivalent resistivity, Ω-cm</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>50,000,000</td>
<td>1E+15</td>
<td>5.00</td>
</tr>
<tr>
<td>50</td>
<td>6,250,000</td>
<td>8E+15</td>
<td>2.00</td>
</tr>
<tr>
<td>10</td>
<td>50,000</td>
<td>1E+18</td>
<td>0.04</td>
</tr>
<tr>
<td>5</td>
<td>6250</td>
<td>8E+18</td>
<td>0.01</td>
</tr>
</tbody>
</table>

We see approaching challenging limitations of semiconductor microelectronics in what we call single-dopant problem: How do properties of a semiconductor subunit change with addition or removal of one impurity atom? Semiconductors handbooks give two fundamental concentration parameters for a semiconductor material: intrinsic concentration $n_i$ and effective density of states in the conduction (or valence) band $N_c$. For silicon, $n_i = 1.45 \times 10^{10}$ cm$^{-3}$, and $N_c = 2.8 \times 10^{19}$ cm$^{-3}$. In classic ‘statistical’
semiconductor physics addition/removal of one dopant atom does not change the concentration/distribution of carriers. However, as illustrated in Table I, this is not the case for small dimensions. In fact, the single-dopant induced concentration is the minimal concentration that can be practically achieved. In the nanoscale domain, the ‘single-dopant concentration’ can be a more valuable indicator of material characteristics than the intrinsic concentration. In this domain, the number, location, and type of dopant atoms, as well as the dimension of the nanostructure will drive the macroscopic properties of the system.

**Deterministic doping effects in nano MOSFET**

In the nano MOSFET, the channel will contain only 50-100 atoms of impurity dopant atoms. The exact position of a single dopant atom will influence the device properties. This scenario represents the transition between a stochastic approach to junction engineering and the precise control of dopant atom location, distribution, numbers, and type that should be applied to all issues of source/drain/channel engineering, such as: Dopant solubility and activation in the nano scale, optimization of channel doping profile, design of shallow junctions and abruptness of the source and drain regions. Metrology for dopant profiling will be a critical issue for nano MOSFET.

**Research vectors:**
- Develop a structure-property knowledge base sufficient to design desired properties, such as band gap, dielectric constant, mobility, activation energy, and etc., into nanosolids based on the type and number of atoms in the nanostructure.
- Manipulation of single dopant atoms and control of their positioning within a host matrix
- Prepare regular nanoscale arrays of dopants
- Devise novel metrology techniques for monitoring single dopant positions, types, and states
- Probe and understand stability issues associated with deterministically doped structures, e.g. disordering due to thermal diffusion, interactions of dopant atoms with point and extended, defects, segregation at surfaces, and etc.

**D. Nanomagnetics and Spin Electronics**

To date, active components of microelectronics have been exclusively based on the electrical constituent of the electromagnetic field, and electron charge serves as the information carrier. Recently, device concepts basing on spin as information carrier were introduced [9-12]. One of the advantages of spin-based electronics is that the characteristic length for spin-dependent effects is only 1 nm compared to 10 nm for semiconductor electronics; therefore, potentially, spin based devices would provide much higher integration density. Spin electronics is a new emerging research area with many fundamental questions still open, beginning with materials issues. “The emergence of this field, as is a common experience in all of the solid state physics, has stemmed from the discovery and development of new materials” [9].

**Magnetic nanoparticles** represents an important research direction with many unresolved scientific challenges and potential technological applications. Finite size and surface effects determine structural and magnetic order in nanoparticles. The quantitative agreement between theoretical and experimental moments is not very satisfactory [10]. The nature of the spin structure in small ferrite particles has not been well understood. From an experimental point of view, the synthesis and manipulation of nanoparticles having well-defined size, shape, and material properties is of great importance. Metrology tools for imaging magnetization are necessary.

One of most important physical effects to be understood and utilized for practical applications is spin injection, or more generally, spin-polarized transport. The opportunity to switch the magnetic configuration of a device by injecting a current pulse is of considerable importance for applications. There are many device opportunities for Spin Electronics, among them non-volatile RAM constructed from
magnetic elements (Honeywell Corp.), spin-polarized transport devices, such as metal-base transistors and spin valves (IBM).

There are three research areas that are vital for further progress in spin-polarized transport. First, 100% spin-polarized materials are needed. It is only with 100% polarized materials that one can hope to address some of the most important applications. For example, the spin-polarized devices could form the basis of a reprogrammable logic technology thus building a base for a universal processor which could be reprogrammed by software, in mid-calculation, to be optimized for any particular calculational step. Also, reprogrammable logic might allow realization of self-evolving circuits. The second research area is “spin injection”. “Spin injection” is the process by which a highly spin-polarized current is transmitted from the ferromagnetic metal into another material, while retaining its spin-polarized character. At this point, the injection through a ferromagnetic/superconducting interface is not understood.

The most difficult, and perhaps the most important, case of spin injection is that from a ferromagnet into semiconductor. Although interesting examples of potential devices have been presented as far back as 1990, there is as yet no report of successful spin injection into a semiconductor. One of the problems may lie in the fact that the metal/semiconductor interface generally forms a Schottky barrier. Although one might expect this tunneling barrier to be no more destructive to the spin polarization than the insulating barriers used for spin-dependent tunneling studies described earlier, the nature of the electronic states at the metal/semiconductor interface are poorly understood. If the physical challenge of injecting spin-polarized carriers electrically into semiconductor devices can be overcome, then the whole panoply of semiconductor nanodevices can be reconsidered to include spin polarized effects.

Spin Electronics could potentially enable realization of Quantum Computing and Quantum Communications [12]. Theoretical efforts must be directed towards understanding the physics which determines the spin lifetime, the coherence of the spin state and the interactions between the spin current and the micromagnetic configuration of a system.

One of barriers in experimental development of Spin Electronics is lack of cross-links between electronics and magnetics communities. Workers in magnetism and magnetic materials have generally ignored issues of electronic transport. Similarly, researchers in the field of semiconductors, intrinsically transport oriented communities, generally have little understanding of solid state magnetism.

**Research Vectors:**

- Discovery research needed to identify and characterize spintronic materials for use in spin electronics based semiconductor devices
- Prepare and understand the magnetic properties of nanoparticles
- Develop a detailed physical understanding of spin dependent tunneling
- Discover novel and practical polarized materials that enable spin-polarized transport and spin-valve metal base transistors
- Increase coherence times for spin degrees of freedom. Microsecond decoherence times would be acceptable for beginning experiments on quantum gate operations, while times of milliseconds would be adequate for even large-scale quantum computing applications
- Explore mechanisms of coupling spin states and the role of the environment and nuclear spin states in the decoherence process.
- Measure spin phenomena at the single-spin level. Explore single spin devices forming the analog to single electron devices.
- Explore optical pumping and ‘optical spin-injection devices’ which could operate without any electrical connections.
  - Fabricate and optimize spin quantum dots
  - Explore materials issues in heterogeneous systems, such as the integration of semiconducting and magnetic materials
The convergence of nanoelectronics and biotechnology

Interdisciplinary discovery research in novel molecular designs and architectures is beginning to enable new devices and integrated functionality. It also facilitates exploring the convergence of tops down research of macroscopic systems with the bottoms up research, represented by the basic physical sciences. Consider Moore’s Law that provides direction and momentum for advancing semiconductor technology and the trends, shown in Figures 8 and 9, as drivers for change. The message is not in the specific data, which represent estimates, but in the long range trends in bit volume and density. Note that a bit is defined as the capacity to store one unit of binary information. Figure 7 summarizes the trend in the number of atoms per bit since 1948. These estimates are reckoned from the National Technology Roadmap for Semiconductors and assumes a cubic volume element for each bit. Another assumption is that silicon, with covalent radii of 1.17 Å, is the dominant materials component. In this figure, time = 0 corresponds to 1999. While one could consider sub-atomic and nuclear information storage strategies for multilevel logic, atoms are easily recognized as discrete units of matter. Consequently, this analysis selected the atom to represent the discrete information storage element. The log-linear plot of atoms per bit over time appears almost linear, though it suggests some deceleration of MOSFET technology for future semiconductor technology nodes.

Extrapolation implies that bit volumes will approach single atoms within forty to fifty years. Note that this data assumes nothing about the nature nor the architecture of the information storage, processing, and communication technology.

To provide a frame of reference, consider the human brain. An average brain has a mass of 1.1-1.2 kg, occupies a volume of 1 liter, and contains roughly $10^{12}$ neurons, each interacting with approximately $10^3$ synapses [13]. Hence, the information storage, processing, and communication capacity of the human brain is about $10^{15}$ bits, which is more than the projected number of stars in the heavens. Based on the total number of bits and the brain’s volume, the information capacity density of the brain is on the order
of $10^{12}$ bits per cubic centimeter. This corresponds to a device with a silicon atom density of approximately $10^{11}$ Si atoms per bit. Assuming the trend in Figure 7 continues, integrated circuit bit density should approach that of the human brain within the next fifteen years. The capability to manufacture integrated circuits at these dimensions would enable forays into new frontiers of biotechnology. This suggests that the approaching convergence of biotechnology and nanoelectronics will catalyze a new technology revolution and new industries. This opportunity is within the career horizon of today’s students and most likely will become a strong driver for discovering more biomimetic and/or biocompatible information storage, processing, and communication technologies.

Finally, consider 3D compatible memory and processing technologies. Figure 8 compares the relative storage capacities of traditional 2D, chip-like, versus 3D technologies. For similar bit volumes, 3D options offer a 15-20 year lead over conventional 2D strategies. In other words, the performance of products based on a 3D application of current geometries would exceed the projected performance specifications at the end of the 1999 International Technology Roadmap for Semiconductors. Furthermore, a packaged 3D device would provide a $10^8$ fold advantage over comparable 2D technology, by the year 2040.

![Trends in Information Storage](image)

**Figure 9. Comparison between 2D and 3D information storage trends.**

Suppose breakthroughs are made which enable inexpensive, non-silicon based, all optical storage and/or processor technologies. Also, suppose they are compatible with the existing software infrastructure. What if this new addressable memory medium was malleable?

**Non-equilibrium based systems**

New materials with unusual properties may free the electronics community from conventional materials, with properties governed by *equilibrium thermodynamics*. Equilibrium thermodynamics requires minimum energy and maximum entropy for a system at equilibrium. One of implication of this requirement in materials is that the equilibrium materials have a uniform volume distribution of constituents, impurities, defects etc. Such materials have very low informational content. When crystalline materials are driven away from thermal equilibrium by external mechanical, physical, or chemical forces, they display several types of interesting phenomena which modify their macroscopic properties. An example is silicon crystal with a special distribution of donors and acceptors prepared by ion implantation or diffusion. These donors and acceptors form p-n junctions, bipolar structures,
source/drain and channel areas of MOSFETs etc. Such a silicon crystal with non-equilibrium distribution of impurities is a core part of integrated circuits. An important result was that integrated circuits were enabled there by reducing external (three-dimensional) interconnects. Today, interconnect technology again represents a difficult challenge for future generations of ICs. A radical solution of the interconnect problem might involve utilization of the complex collective behavior of materials constituents such as atoms, molecules, defects, crystallites etc.

In the near future, monolithic “smart” electronic materials may substitute for assemblies of many parts. Functionality is achieved by deliberately introducing and controlling inhomogeneities; such as dopants, defects, pores, alternate layers of conductors and insulators; within the material. One can think of high functionality materials in terms of a *Turing machine* embedded in a solid, where the information processing occurs at the level of material components. A grand challenge is to determine how much functionality can be designed into a given nanostructure.

*Deterministic Doping* (section 1C and ref. 14), *Defect Engineering*, and device realizations of *Quantum Computing* [12] could provide the basis for constructing smart electronic materials. An important step towards realizing practical applications of smart electronic materials was the recent introduction of concept of “architectonic” *quantum dots solids* [15], that potentially allows for designed materials with a prescribed set of electronic properties. The term architectonic was suggested by the UCLA team to describe the design of materials with prescribed electronic properties based on the size of and spacing between quantum dots. Other developments in Smart Electronic Materials have been achieved by combining these disciplines with *self assembly* principles (section 4A). Integrating these concepts in the fabrication process could lead to reconfigurable and defect tolerant smart matter [16], that utilizes individual molecules as electronic building blocks. These building blocks embody the potential for a molecular “macro” language. Ultimately, molecular devices might be manipulated within a template and assembled or reassembled, depending on the needed functionality.

**Quantum computing**

Quantum computing is new emerging area of computation and communication basing on physical implementation of quantum bits or qubits, that is information stored in a two-state quantum system. An example are the two spin states of electron or nucleus often referred as “up” (↑) and “down” (↓). In quantum systems, besides storing classical ‘1’ and ‘0’ information there is also the possibility of storing information as a *superposition* of ‘1’ and ‘0’ states. Another intriguing feature of quantum systems is *entanglement*. Entangled states can be created whenever quantum systems interact with one another. When subsequently the systems (e.g. particles) become separated, the influence of one member of the pair over the other persist independent on thickness between them! Although, the entanglement as a paradox of quantum mechanics was debated many years ago, its experimental studies has been started only recently [17]. Extended experimental and theoretical studies of entangled systems may not only lead to new breakthroughs in physics (including possible emergence of new theory that may eventually supplant quantum mechanics!), but also may build absolutely new information technologies.

Qbit devices include quantum computers, quantum gates, quantum key receivers, quantum teleporters, quantum robots etc. [17].

The couplings of the qbits to both their internal and external environments will inevitably result in quantum decoherence. The decoherence is the main obstacle in practical qubit device development. A practical universal quantum computer is presently not feasible, and must await further revolutionary discoveries and advances [17]. However, specialized quantum computers could be designed for several specific tasks that can not be accomplished by using of classical computers. For example, although a quantum factorizer capable of factoring a 250-digit number does not presently exist, if and when one does, the widespread cryptosystems relying on difficulty of factoring large numbers will be rendered
insecure and obsolete. However, to date, not even a 5-digit number has been factored with a quantum computer.

Several concepts for practical implementation of qubit devices were proposed, and some of them were experimentally verified. However, at this point all experimental realizations are limited with macroscopic systems with small number of qubits. Examples are NMR quantum computers, optical and ion-trap Qbit devices. All these examples can be regarded as partial feasibility demonstrations, rather than practical devices. Experiments are needed that target the demonstration of solid state quantum computing. Several realizations of solid-state quantum computer have been proposed. For example, a concept of Si-based Quantum Computer was proposed by Kane utilizing nuclear spins to form qbits [18]. The proposed quantum computer would be based on a regular distribution of $^{31}$P atoms in Si matrix. Donors must be introduced into the material in an ordered array, furthermore, precisely one donor must be placed into each array cell. In this approach, the qbits are the spins of atomic nuclei of the dopant $^{31}$P atoms.

There are several difficult technical problems to be overcome for practical realization of the Si-based quantum computer, including positioning of individual phosphorus atoms in a prescribed regular array; limitations of the decoherence rate of the phosphorus qubits in the presence of spin impurities and crystal defects. There are very strict requirements to the purity and perfection of Si matrix.

Another solid state approach to quantum computers is the quantum-dot quantum computer. A qubit here would be the two spin states of an electron in a single-electron quantum dot, and a quantum register would consist of an array of coupled single-electron quantum dots. Quantum gate operations would be performed by gating of the tunneling barrier between neighboring dots, to produce controlled entanglements of qubits. This concept relies on the advances in Spin Electronics, that are yet to be achieved.

Opportunities for quantum computing have stimulated renewed interest in the superconducting quantum interference devices (SQUID). Quantum coherence of the charge states in a single-Cooper-pair box or the flux states in an rf SQUID can be used to create qubits for quantum computation [23]. Quite recently, the first experimental demonstration of a quantum superposition of truly macroscopically distinct states was reported [24]. It should be also noted that SQUID is perhaps the only potential implementation of quantum computing which does not require reproducible fabrication of sub-1-nm components, since SQUID qubits may operate with 50-nm-scale minimum features [25].

**Research Vectors:**
- Provide foundational knowledge in biomimetic and biocompatible nanelectronic osystems,
- Explore concepts and strategies for realizing intelligent and evolving materials
  - Investigate the potential of deterministic doping, nanoporous electronic materials, and defect engineering in nanoelectronics
  - Characterize “architectonic” Quantum Dots Solids
  - Correlate experimental and theoretical studies of collective behavior (i.e. synergetics) effects in solids
  - The physics of entanglement and quantum decoherence should be more extensively investigated
  - The qubits based on solid-state concepts such as determinisitic dopants in Si, quantum dots, Josephson junctions and SQUIDS remain to be experimentally demonstrated
  - Provide foundational knowledge base on mobile qbits and transport of entangled qbits
  - Sources of large-scale controlled entanglements should be found
  - Studies of picosecond optical excitation as a mean for coherent control quantum-dot states
- **Gather basic materials data sufficient to characterize nanoelectronics related materials and structures:** Much remains to be learned about the electrical properties of both single molecules and self-assembled structures. Limited results were mentioned regarding the I-V characteristics of individual molecules and their potential as semiconductors. It was reported that fundamental resistivity of 12 KΩ/molecule is possible
and that contact resistance of $<1\times10^{-7}$ $\Omega\cdot$cm$^2$ was achieved with gold nanoclusters. In general, however, there is lack of systematic data on resistivity, stability at high current densities, reliability of electrical measurements, or the influence of environment on the electrical characteristics.

<table>
<thead>
<tr>
<th>Summary: Basic Science Needs related to Nanoelectronics</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Research Direction</strong></td>
</tr>
<tr>
<td>Interfaces</td>
</tr>
<tr>
<td>Conductivity at small dimensions</td>
</tr>
<tr>
<td>Deterministic doping effects</td>
</tr>
<tr>
<td>Nanomagnetics</td>
</tr>
<tr>
<td>Discovery research towards Functional Synergy in Nanoelectronics</td>
</tr>
</tbody>
</table>

2. Nanoscale Materials

A. Nanoparticles and Nanotubes

In the nanometer domain, fabrication of silicon devices to achieve integrated functionality could be as difficult for silicon as for other materials. We need a “re-definition” of properties that makes a material suitable for the fabrication nanoelectronic systems and a reconsideration of other classes of potentially useful materials. For example, the conventional approach to fabricating electronic devices requires a dual, but interdependent, material and process strategy for fabricating transistors [Front End Processes] and the interconnects [Back End Processes]. This approach is complex and alternate approaches should be sought.

Nanosized building blocks could provide new opportunities for constructing electronic devices. However at this point, little is known about material properties in the nanometer domain. The physical properties of nanoscale structures (1-50 nm) are significantly different from those of microscopic or bulk materials of identical chemical composition. The fundamental differences between bulk materials and nanostructures are related to: 1) size effects, 2) gradient/interface effects, 3) control of atomic architecture, and 4) surface effects.

Size effects cause changes in such fundamental properties as electrical and thermal conductivity, band gap, density of states, dielectric constant and electron affinity. All these parameters depend on the size of an individual nanocluster. **Thus, all handbook data about electronic properties of materials is of questionable value for the nanoparticles.** Carbon nanotubes represent a new class of self assembled nanomaterials for possible use by the electronics community. They can grow in clusters or individually, as shown in Figure 10, and exhibit potentially interesting mechanical and electrical properties.

![Patterned Arrays of Nanotubes](image1)

![Selective CNT Growth](image2)

*Figure 10 (a) Patterned nanotube arrays and (b) selective growth of carbon nanotubes [19]*
Considerable effort has focused on modeling these systems. However, much remains to be discovered about the basic chemistry and synthetic methods required to control the helicity, the alignment of molecular orbitals along and across the nanotube, dimensionality, degree of branching, functionality, and properties of nanotubes.

**Nanotubes in nano MOSFET devices**

With proper synthetic control, carbon nanotubes can grow with subtle differences in molecular structure and orbital symmetry and exhibit conducting, insulating, or semiconducting properties. Could they serve both as devices and interconnects? Also, these materials are mechanically and chemical stable at temperatures exceeding 1000°C. Consequently, this material may provide an opportunity for bridging the current Front End – Back End dichotomy of current microelectronics fabrication protocols, i.e. the increasing need for thermal budget control arising in conventional processing.

Table II shows some possible nearer term applications that could serve as vehicles to longer term nanoelectronic applications [20].

<table>
<thead>
<tr>
<th>Application</th>
<th>Property</th>
<th>Challenge</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNT-film as a low-K insulator</td>
<td>Inherent low density of the CNT-films</td>
<td>The CNT film would need to be deposited, planarized, patterned and etched with techniques compatible with the underlying silicon devices</td>
</tr>
<tr>
<td>CNT as interconnects</td>
<td>Low resistivity</td>
<td>Manipulation/attachment of individual CNT</td>
</tr>
<tr>
<td>Probes for metrology</td>
<td>High aspect ratio of tips</td>
<td>Attachment of a single CNT to the cantilever</td>
</tr>
<tr>
<td>Manufacturing with Micro- or Nano-Tools</td>
<td>High aspect ratio</td>
<td>Micro-tool arrays must be “fast, flexible, and inexpensive”</td>
</tr>
<tr>
<td>Field emitters</td>
<td>High aspect ratio, thermal conductivity</td>
<td>Performance of CNT field emitters?</td>
</tr>
<tr>
<td>Passive devices: capacitors and inductors</td>
<td>Geometrical characteristics</td>
<td>Is it possible to grow helical conducting nanotubes?</td>
</tr>
<tr>
<td>CNT for active electronic devices</td>
<td>Possibilities to control electronic properties by structural characteristics</td>
<td>The current standards should be met: low cost (1 µcent/transistor), high level of integration (10⁹ transistors/circuit); high reproducibility (+/- 5%), reliability (operating time &gt;10years)</td>
</tr>
</tbody>
</table>

**Research Vectors:**

- Synthesize and characterize the physical properties of different nanotubes and nanoparticles.
- Achieve precise control over nanotube and nanoparticle size, distribution, and molecular architecture.
- Explore the electronic properties of nanotubes and nanoparticles as function of size and structure.
- “Fine tune” the electrical, optical, mechanical, and sensing properties of nanomaterials by precise compositional and size control.
- Extend the nomenclature of calibrated nanomaterials. There is a need to branch out from the commonly used nanoparticles, that is, metals and the metal oxides, and the II-VI chalcogenides, into other materials that may be of interest to the electronics industry.
- Explore assemblies of different types of nanotubes into predetermined networks and functional
B. Metrology of Nanoscale Materials

Metrology of MOSFET Materials, Processes, and Devices

Explore novel and noninvasive concepts and methods for probing and characterizing the dimensions, composition, and properties nanoscale materials, features, and systems. Examples include, but are not limited to: Ultra low voltage electron beam imaging, secondary electron spectroscopy, and point projection holography.

Research Vectors: Characterization of nanoscale systems

- Design noninvasive tools and methods that enable molecular level measurement of materials and devices, facilitating correlations between structure, macroscopic properties, and functionality.
- Investigate the effects of local environment on the functionality of embedded components and nanosystems.
- Design enhanced interface spectroscopies to probe device junctions.
- Develop tools to rapidly screen for functionality in complex assemblies of materials.
- Create predictive models for energy transfer and dissipation mechanisms to guide investigations into the impact of these processes on the electrical properties of molecules and nanostructures.
- Cross train researchers across a diverse array of disciplines to develop a common language.

Summary: Nanoscale Materials issues related to Nanoelectronics

<table>
<thead>
<tr>
<th>Research Direction</th>
<th>Nano MOSFET</th>
<th>Beyond MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>A. Nanoparticles and Nanotubes</td>
<td>✓ (see table 2)</td>
<td>✓ Engineered nanoelectronic materials</td>
</tr>
<tr>
<td>B. Metrology of Nanoscale Materials</td>
<td>✓</td>
<td>✓ Molecular Electronics and Functional Materials</td>
</tr>
</tbody>
</table>

3. Nanoelectronic Devices

Modern microelectronics is based on the use of the transistor, a three terminal device with nonlinear input-output characteristics that offers forward gain, relatively good input isolation, and good current drive. To date, the devices proposed in the nanoelectronics domain have not been able to provide all of these attributes and many may be limited to niche applications. Indeed, many are two-terminal devices. Another challenge is the contact-to-device ratio. What today is called a nanoelectronic device typically consists of something VERYSMALL (e.g. nanoparticle, molecule etc.) attached to MACROSCOPIC electrodes. Such structures provide insight into physical processes, but have yet to realize viable and practical applications. Making and connecting a few of these nanodevices to make a simple function is still a challenge and requires an interdisciplinary approach to explore and understand the dynamics of electrons interacting with the molecular orbital network and band structure of integrated device components. Clearly we need technologies that provide commensurate device and contact scaling. Finally, paths to 3-dimensional chip architecture should be discovered and explored.

Research Vectors:

- Investigate novel nanodevice design that mimic 3 terminal or higher forms of device functionality
- Explore multifunctional and multibit components for molecular electronics systems
- Design and demonstrate novel nanodevices with gain
- Study the chemistry, physics, and engineering of orbital engineering and Ohmic contacts
Pursue concepts that test the feasibility of self powered devices

A. Molecular Devices

As device dimensions approach the nanoscale, it may be useful to consider approaching the design and fabrication of nanometer and subnanometer device structures as a synthetic chemistry challenge, analogous to the design and synthesis of high performance pharmaceuticals.

In Molecular Electronics, the molecules serve not just as building blocks of electronic components, but as the components themselves. In general, electronic devices are based on structures with pre-defined charge distribution that changes in response to an external electromagnetic field. The molecule is a minimum stable material structure with structure-defined charge distribution, and using individual molecules as active electronic components appears to be feasible. Clearly, this would open enormous opportunities to building ultra-dense electronic circuits. However, much research in this area is needed to realize the promise of molecular electronics.

Today, a natural, but not necessarily feasible approach to molecular electronics is to duplicate today’s microelectronics circuits using molecular components. This view has inspired researchers, to look for molecular analogs of conductors (e.g. polyphenylene chains) and insulators (e.g. aliphatic methylene groups) etc… One of the difficult problems is to connect the molecular devices to external electrodes in a circuit. A typical demonstration of molecular electronics device today involves a molecule (1nm size) attached between two macroscopic electrodes (1 µm size), or attached on the end of a STM tip. An alternative would be to seek out novel wireless interconnect nanostructures. Additionally, J. Heath’s/UCLA team is developing an original approach to making nanoelectronic systems from molecular components. Instead of testing individual molecular electronic components, without visible ways to connect them in an useful circuit, they considered architecture of a nanocomputer as a whole. J. Heath, along with colleagues at Hewlett-Packard, applied his expertise in development defect tolerant computer architectures to molecular electronics. The basic architecture of Heath’s molecular computer is an array of conducting wires randomly connected with “molecular switches” (i.e. single molecules changing their electron transport properties as a function of input signal). This may be a partial solution to the above problem; the electrode size in this case is equal to the diameter of wire (nanotube), and the interconnect system is not specified by nano-scale patterning. The theoretical density of elements in this approach can be very high, and 3D integration naturally emerges. An unsolved problem is that the 2-terminal molecular switches do not produce any gain, so a complex function may require unrealistically high input signal amplitude. Also, a “learning” process or mapping is a necessary step in making such a defect tolerant computer. This approach requires a very long instruction word (VLIW) to specify each computer, analogous to the m-RNA that codes for a specific protein in biological systems.

Research vectors:

- Experimentally demonstrate simple functionality by combining individual molecular devices
- Study the chemistry and physics of electron transport through a molecule
- Extend materials nomenclature to comprehend the molecular design of electronics materials
- Explore paths to achieve three-terminal molecular and nanoscale devices with gain
- Provide knowledge base sufficient to establish rules and expert systems for designing and engineering molecular and orbital level contacts, ie. making reliable, uniform electrical contacts with molecules
- Investigate novel nanoscale cross-wire and wireless interconnect architectures
B. **Single electron devices**

The single electron phenomena, where a relatively large change in the potential energy of a system occurs as a result of addition or removal of a single electron was extensively studied during the last two decades. Figure 11 illustrates a single electron effect known as *Coulomb blockade*. Figure 12a shows one of the simplest of the single electron devices; the single-electron transistor (Averin and Likharev 1986, Fulton and Dolan, 1987 [26], L. Guo et al. 1997 [27]). The device resembles the MOSFET, but instead of a diffusively-conducting channel, the drain and source are connected with a small island separated from the electrodes with tunnel junctions.

An important device category are various single-electron memory cells - for details, see, e.g., the detailed recent review (Likharev 1999 [28]). So far, high-density memory appears to be a most suitable application for the single electron devices. A single electron memory cell is shown in Fig. 12b,c. It represents an alternative floating-gate structure and it could be considered as an example of merging existing MOSFET technology and emerging nanoelectronic technologies.

![Fig. 11. Ideal current-voltage characteristics of electron transport with Coulomb blockade (assymmetric double junction system at zero temperature). Adapted from D. K. Ferry and S. M. Goodnick, 1997[21]. By adding of single electron from a reservoir to a very small particle (e.g. quantum dot, the potential of the dot increases by $e/2C$ ($C$ is capacitance of the dot) and no more electrons will be added to the particle unless applied voltage is increased by same value. This results in stair-like I-V characteristic.]

Beyond this hybrid structure, many concepts for single electron devices were proposed during last decade. Many journal publications and several books describe these concepts in details and provide rigorous physical description of operation of single electron devices. However, the single electron devices have not yet been reduced to practice. The difficult challenges are: Lack of a suitable structure and system architecture, lack of reliable manufacturing, and low operating speeds for existing architectures.

![Fig. 12. Different configurations for single electron devices (adapted from TREN 1999): a – SET; b – multidot nanoflash memory; c – single dot nanoflash memory]
Table V . Single-Electron Memory: state of the art and target parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>State of the Art</th>
<th>Near-term target</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits/chip</td>
<td>128 M (K. Yano et al. 1998 [31])</td>
<td>&gt;1 G</td>
</tr>
<tr>
<td>Method</td>
<td>e-beam</td>
<td>Mass productive method</td>
</tr>
<tr>
<td>Materials</td>
<td>Poly Si QD/poly Si</td>
<td>Optimum materials system</td>
</tr>
</tbody>
</table>

The most important advantages of single-electron devices are as follows:

- Physics of their operation is based of the ubiquitous electrostatic charging and does not depend on the particular material of their components, thus permitting a focus on materials beneficial from the fabrication point of view. For example, single-electron transistors operating at room temperature have been demonstrated using such different islands as organic macromolecules (Soldatov 1996 [29]) and metallic film islands (Matsumoto 1997 [30]).

- The devices may be scaled down to virtually atomic size.

Nevertheless, practical introduction of single-electronic integrated circuits faces several serious problems:

- Room temperature operation requires islands of the size below a few nanometers and these are difficult to manufacture.

- Transconductance of single-electron transistors is well below the fundamental value of 77 $\mu$S (see Sec. 1.B above). As a result, charging of long interconnects by single-electron devices may take unacceptably long time.

- High sensitivity of single-electron devices to electric fields make their switching thresholds highly vulnerable to even single charged impurities in their dielectric environment (Likharev 1999).

As a result of two last problems, application of single-electron devices in usual combinational logic circuits seems highly improbable. However, for single- and few-electron memory cells and certain neuromorphic logic architectures, several ways to circumvent the sensitivity to random charges have been found, and their implementation is now mainly dependent on fabrication of integrated circuits with a-few-nm features. In addition, a system for ultra-dense (beyond 1 Tbit/in$^2$) electrostatic storage, which requires only discrete single-electron transistors, has been suggested.

**Research vectors:**

- Continue study of a single electron memory operating under standard IC performance conditions.
- Explore fabrication methods compatible with the mass production requirements.
- Search for optimum materials for single electron devices, circuits, and systems.
- Explore different single-electron logic architectures which would be insensitive to random charges and low device transconductance; continue to explore new concepts in phase-shift and tunneling phase logic as well as in quantum cellular automata (QCA).
- Initiate study of ultra-dense electrostatic storage as a possible alternative to the mainstream magnetic storage.

**C. Deterministic doping devices**

Single-dopant effects not only set limitations, on the applicability of classical semiconductor physics, but they also offer new opportunities for nanoelectronic devices. For example, device operation based on controlled discrete distribution of single impurity atoms rather than on a stochastic distribution of dopants within a continuum environment was recently proposed [14]. The general principle of operation is based on single charge effects, when considerable change in the potential surface of a system occurs due to addition, removal, or displacement of a single charge. It is expected that a silicon structure with regular distribution of donor and acceptors (e.g. ultimate bipolar cells) will demonstrate unusual and perhaps useful properties.
Research Vectors:
• Develop a foundational knowledge base that enables the controlled manipulation of atoms and molecules and their interactions with surfaces and materials

Summary: Relation to near- and longer-term developments in nanoelectronics

<table>
<thead>
<tr>
<th>Research Direction</th>
<th>Nano MOSFET</th>
<th>Beyond MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>A. Molecular Devices</td>
<td>✔Gate stack</td>
<td>✔Molecular Electronics</td>
</tr>
<tr>
<td>B. Single electron devices</td>
<td>✔Single electron flash memory</td>
<td>✔Single Electronics</td>
</tr>
<tr>
<td>C. Deterministic-doping devices</td>
<td>✔Channel engineering</td>
<td>✔Functional and Smart Electronic Materials; Molecular Electronics</td>
</tr>
</tbody>
</table>

3. Molecular and Nanoscale Fabrication Methods and Processes

The vitality of the semiconductor industry depends on the ability of manufacturers to maintain the momentum of productivity enhancements projected by Moore’s law. With the emerging challenge of fabricating nanoscale systems, radical alternatives to conventional fabrication methods are needed to achieve these performance goals. Known concepts to explore with a nanoscale focus include, but are not limited to: Non-lithographic patterning – step and flash; micro-contact printing; Ultra-thin patterning materials; Alternate materials and processes for patterning; Alternate imageable materials; Resistless/additive materials and processes; Solvent-free/all dry processes; Molecular beam epitaxy for and beyond MOSFET; 3-D integration technologies; Defect tolerant materials, systems, and architectures; and Process integration. Other interdisciplinary approaches to fabricating functional molecular and nanosystems must consider: materials characterization, system design, synthesis, quantitative structure property relationships (QSAR), molecular dynamics, directed self assembly, variable building blocks, self limiting assembly, and control mechanisms.

A. Self-assembly

Self assembly represents an additive process. With respect to materials management issues, self assembly represents a more sustainable technology than conventional subtractive lithographic approaches to patterning, that waste much of the deposited and processed material. There is a hierarchy and progression of opportunities for self-assembly in nanoelectronics that converges with devices, applications, and systems. The first level is self assembly for patterning. The goal at this level is to discover a set of low cost, self assembled alternatives to conventional lithographic methods. A second level comprehends systems that are defect tolerant and/or self-repairing. This would enable robust fabrication of nanostructures and nanosystems. Finally, a third level would address the challenge of self-evolving systems and ultimately Intelligent Machines. This last level includes the challenge of designing smart materials. Not only would these systems be adaptable and reconfigurable, but grow three dimensional structures derived from a prescribed template. One example in nature is the synthesis of proteins, based on the interaction of t-RNA with m-RNA, as it is read through a ribosome. Novel ideas in this area may be coupled strongly with leading edge concepts for devices and nanoscale system functionality.

Research Vectors:
Near-term opportunities include:
• Hybrid approaches, such as photolithography modulated self assembly, to prove the feasibility of self assembly methods and to incorporate them into IC’s manufacturing process
• Self assembled resists for advanced lithographies
• Database of structure-property relationships and synthetic methods for designing self assembled structures.
• Bulk properties of self-assembled materials and processes should be characterized and catalogued to
enable broader use of these materials for microelectronics. A database for self assembly methods and material properties is needed.

- Investigate the potential of self assembled dendrimers and composite dendrimer systems

Medium-term opportunities include:

- Self-assembled systems for electronic or optical applications, such as retinal embedded in cone like structures for optical image processing.
- Molecular printing and alignment
- Self assembled MEMS
- Self assembled optical interconnects
- Polymer-based electronic devices, circuits, and systems
- Pursue novel concepts in Bio-inspired manufacturing, including directed or assisted self assembly, ie. DNA, ribosome assisted, etc.

**Self Assembled Materials and Fabrication Processes**

The heavy emphasis at present on empirical, almost trial-and error fabrication methods serves to highlight fundamental knowledge gaps. There is a need for theoretical validation and a more fundamental understanding of the chemistry and physics of self assembly, rather than an empirical approach to fabrication. Self assembled materials reported in the literature include: self assembled monolayers (SAMs), Dendrimers; Block copolimers; Polyphenylenes; CaF$_2$:Ca; Ge/Si; Ga,In,Sn/Si; SiO$_2$/Si, CoSi$_2$/Si, Au nanoclusters+molecular precursors; GaAs:As

**Research Vectors:**

- **Explore the fundamental driving forces for self assembly, including:** chemical affinity, thermodynamics, electrostatics, crystallographic orientation, strains due to patterns and/or compositional differences, external energy fluxes (i.e. electron irradiation), surface reconstructions. Thermodynamics of self assembly, ensemble energy should be basis of calculations, not single-island energy

- **Develop predictive and efficient simulation tools:** In contrast to experimental results, the efforts in modeling and simulation of self-assembled structures for nanoelectronics are in an embryonic state. It appears that much can be learned from other disciplines, e.g. from pharmacy where simulation of self-building, self organization etc of complex organic building blocks such as proteins is a well established research area. A promising approach for modeling of self assembly is Genetic based algorithms.

**A. Nonlithographic Patterning**

Patterning drives the cost of fabricating semiconductor devices and electronic systems. Conventional patterning imparts a three dimensional shape to a thin film material by a subtractive process of removing material not required by the design. There is a need to look to other disciplines for novel approaches to building structure and functionality into molecular and nanoscale systems.

A nonlithographic patterning approach could dramatically reduce the cost of fabricating patterned nanoscale systems. Concepts include soft lithography and maskless patterning. Maskless methods do not require a transmission, reflection, dispersion, or stencil mask or reticle as part of the patterning process. Soft lithography embodies a set of patterning methods, such as microcontact printing, injection molding, or passive material packing to fabricate nanostructures. These methods may be thermally or photonically assisted. Limited applications of soft lithography, one or two levels, may be compatible with current electronics manufacturing methods. However, much discovery and knowledge are required to realize the potential of these materials and methods. Examples in the early stage of exploration include imprint patterning, which embosses an image into a pliable thin film polymer, and step-and-flash patterning,
which creates structures through a nanoscale injection molding process. The latter represents an additive patterning alternative to conventional approaches. The challenges associated with these strategies are materials related.

Nano-probe patterning represents one class of maskless patterning options. It removes the cost and variability of a limited lifetime mask from the fabrication process. However, the viability of this approach requires a massively parallel approach to patterning with an array of probe tips. The challenges associated with the uniformity and longevity of tip behavior and data management are enormous.

**Research Vectors:**
- Explore the feasibility and limits of unimolecular pixels for high resolution patterning and data storage
- Uncover novel uses for chemically inhomogeneous materials, such as block copolymers
- Establish robust methods for fabricating certified nanotip and nanotube probes, with designed functionality
- Design and build nanoscale devices and structures via controlled atomic manipulation of dopants
- Provide foundational knowledge base sufficient to guide strategies for managing and directing massive amounts of information
- Investigate mechanisms of coupling between molecules and between molecules and their surroundings
- Establish quantitative relationships between physical/chemical linkers and the electronic properties of the junction
- Discover novel methods for patterning nonregular structures on substrates,
- Devise and fabricate electrical contacts to the outside world and to and internal interfaces

**Summary: Molecular and Nanoscale Fabrication Methods and Processes related to Nanoelectronics**

<table>
<thead>
<tr>
<th>Research Direction</th>
<th>Nano MOSFET</th>
<th>Beyond MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>A. Self-assembly</td>
<td>?</td>
<td>✔️</td>
</tr>
<tr>
<td>B. Nanometrology and Nonlithographic Patterning</td>
<td>✔️</td>
<td>✔️</td>
</tr>
</tbody>
</table>

**Appendix A. New physics – from analytical equations to computer codes**

The very aggressive scaling of traditional CMOS has fueled the affordability of high-speed, parallel computing in the form of large PC-based clusters. The concurrent realization of computational physics (as evidenced by the recent Nobel Prize in Physics for Density Functional Theory) in conjunction with the development of *ab-initio* (first-principles) methods, have facilitated the prediction of macroscopic material properties from the quantum-scale electronic structure. Although the temporal and spatial scales of these methods do not yet extend into the real world domain, the very decrease in device sizes makes a solution entirely from first-principles increasingly more feasible (see Appendix A).

The judicious use of modeling and simulation for the conductivity characteristics of the many device alternatives “beyond CMOS” can serve as a cost-effective methodology to “screen out” the choices which are either difficult to manufacture or do not provide superior system-level performance. In order to continue down the aggressive path defined by Moore’s law over the last several decades, the theoretical and/or computational endeavors should be tightly coupled with the appropriate experimental characterization or measurement techniques, thereby minimizing technology development cycle time.
The design of electronic devices/processes from the 1st principles is an ultimate goal of atomistic TCAD. Until recently, predictive 1st principle TCAD was considered non-realistic, at least in short term, mostly because of the very large number of atoms in real systems. These numbers, however, decrease as the size of the device decreases (Fig. 13). On the other hand, the computational power increasing at approximately the same rate (in part as result of scaling). Both Moore’s law and tendencies in computational power can be presented on a common scale, e.g. number of atoms per device and number of atoms in a system for which 1st principle calculations can be executed as functions of year. The intercept of both lines gives us an estimate for the time when full 1st principle calculations of electronic devices can be expected as shown in Fig. 14. According to Fig. 14, this happens approximately in 2010.

The development and broader use of 1st principle computer calculations may herald a new era in physics, e.g. a transition from the physics of analytical equations to a physics of direct modeling. Since the analytical equations in physics are approximations, they can fail to represent the atomic domain. For example, a typical working equation in semiconductor physics is:

\[ f(x) = c_1 g\left(\frac{x}{\lambda}\right) \exp\left(c_2 \frac{x}{\lambda}\right) \]

(Parameters \(c_1, c_2\) and \(\lambda\) are phenomenological.)

**Examples:**

\[ D(T) = D_0 \exp\left(-\frac{E}{kT}\right) \]
- diffusion coefficient

\[ n(x) = \frac{\phi}{\sqrt{2\pi\Delta R_p}} \exp\left(-\frac{(x - R_p)^2}{2\Delta R_p}\right) \]
- doping density of implanted atoms

\[ J = J_s \exp\left(\frac{qV}{kT} - 1\right) \]
- transport equation for a diode

\[ J_s = A \times T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \]
- saturation current density for a metal-semiconductor contact

The 1st-principle computational physics may open new horizons in nanophysics. Solution to many of the problem and questions of nanotechnology will require mathematicians working closely with experts in the physical and design sciences.
Acknowledgements

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