Welcome to ISMT / SRC Maskless Lithography Workshop

Chairmen:
Dan Herr / Semiconductor Research Corp
Scott Mackay / International SEMATECH
Information & Welcome

• Administration / Information / Facilities
• What is Maskless Lithography?
• Agenda
• What should we expect to accomplish today?
• Timing and Requirements for technology introduction
• Your job today...
Open Conference Confidentiality Notice

• This meeting is an OPEN CONFERENCE.

• Confidential or Proprietary information may NOT be disclosed.

• All meeting attendees are permitted to take notes or otherwise make a personal record of these proceedings.

• All presentations will be available to the public via the International SEMATECH public website following this meeting.
Meeting Room Floor Plan

- **SALON I**
  - Lunch
  - Tuesday 8/28

- **SALON II & III**
  - General Session
  - Tuesday 8/28

- **Registration Table**
  - Open Tuesday 0700

- **Exits**
Breakout Session Locations

- **Breakout session locations**
  - Green & Red in general meeting room
  - Yellow in Consulate Room
  - Blue in Ambassador Room
ML2 Workshop Meeting Groundrules

• What will be discussed
  – Questions/answers about ML2 technical challenges, risks, and readiness

• What will NOT be discussed
  – Politics
  – Program management
  – Confidential plans or technology
  – Business issues (funding, intellectual property, etc.)
What is Maskless Lithography?

• Beginning assumptions about “MaskLess Lithography”
  – No mask - data fed straight through from tape to tool
  – Large data transfer rates (multi-tips and/or high transfer rate) ~10 Tbits/sec
  – High throughput tools, ~20 WPH
  – Tool costs below competitive lithography strategies
  – Potential solution to:
    • Rising mask costs
    • Short-run and development activities in IC companies
Why Maskless Lithography?

- CoO models suggest that for small runner parts, ML2 may be most cost effective method of Mfg.

- Recent calculations suggest for 50nm node, TP=5 WPH has better CoO that other NGL <3000 wafers/mask!
What is covered in this Workshop?

• Review of SRC sponsored research
• Presentations from vendors with commercial tool programs
• Review of two topics critical to the success of ML2
• Audience Participation activity to set future direction
• Reminder:
  – These presentations are not completely inclusive of all activity in the technology, only as a starting point for further discussion
## Agenda

<table>
<thead>
<tr>
<th>Time</th>
<th>Event</th>
<th>Speaker</th>
</tr>
</thead>
<tbody>
<tr>
<td>0800</td>
<td>Welcome / Introduction</td>
<td>S. Mackay</td>
</tr>
<tr>
<td>0830</td>
<td>Review SRC Activities</td>
<td>D. Herr</td>
</tr>
<tr>
<td>0930</td>
<td>BREAK</td>
<td></td>
</tr>
<tr>
<td>0945</td>
<td>ETEC</td>
<td>M. Gesley</td>
</tr>
<tr>
<td>1030</td>
<td>Canon</td>
<td>N. Deguchi</td>
</tr>
<tr>
<td>1115</td>
<td>Micronic</td>
<td>J. Freyer</td>
</tr>
<tr>
<td>1200</td>
<td>LUNCH</td>
<td></td>
</tr>
<tr>
<td>1300</td>
<td>Emission Systems, LLC</td>
<td>H. Lockwood</td>
</tr>
<tr>
<td>1345</td>
<td>Source development</td>
<td>D. Lowndes</td>
</tr>
<tr>
<td>1430</td>
<td>Review of Data Path / Volume Issues</td>
<td>K. Standiford</td>
</tr>
<tr>
<td>1515</td>
<td>BREAK</td>
<td></td>
</tr>
<tr>
<td>1530</td>
<td>Breakout Sessions : Identify Critical Issues / Review Industry Impact</td>
<td></td>
</tr>
<tr>
<td>1630</td>
<td>Review Results / Wrap-up</td>
<td></td>
</tr>
<tr>
<td>1700</td>
<td>ADJOURN</td>
<td></td>
</tr>
</tbody>
</table>
What should we expect to accomplish?

• **Purpose:**
  – Review Progress in Maskless Lithography activities
  – Evaluate where industry can impact the progress of the programs

• **Expected outcome:**
  – Audience has a better understanding of the maskless lithography technology status
  – Vision as to when maskless lithography could make an impact to the ITRS (node and timing)
  – Identification of critical issues that need to be demonstrated
ITRS Roadmap Potential Acceleration

Minimum Feature Size (nm) (DRAM Half-Pitch)

1994 SIA
1997 SIA
1998 / 1999 ITRS

ISMT Litho 2001 Plan
(2-year cycle to 50nm)

2000/2001 ITRS

Proposed ML2 Introduction

INTERNATIONAL SEMATECH

RSM Maskless Litho Workshop Opening remarks 8/28/01
Timing and Requirements

- Survey of ISMT and SRC member companies
  - Focused on how the technology would be used
    - e.g., development (product/device/process) or production
  - Requirements for technology (tool) capability
    - Throughput / CoO
    - Wafer size / field (Die) size
    - Process compatibility
  - Timing
  - Progress on Critical Issues
  - Potential Research / development area
Survey Results.....

- **ML2 could be used for:**
  - Product / device development if:
    - Available for N+1 to N+3 nodes
    - Available now to early ‘03
    - 300mm capable and compatible with DUV processing
  - Production (possibly only for critical levels) -
    - Maintain throughput to tool cost ratio (CoO)
    - Available for~35nm node
    - Available in ‘04–’06
Survey Results.....

- Issues that still need to be resolved are:
  - Data handling for high data volumes
  - CD error sources in direct-write
  - Need to demonstrate high throughput approaches
  - Demonstration of parallel illumination sources
  - Solution for market acceptance
Your Job Today...

• **Listen critically!**
  – Are the programs tracking the needs of the industry?
  – Are the program timing and requirements meeting your expectations?

• **Develop opinions**

• **Constructively feedback in afternoon sessions**
  – Provide feedback on technology progress
  – Provide areas of further work (Critical Issues) that need to be addressed
A Brief Overview of SRC/DARPA’s University Research Initiative in Maskless Lithography

Maskless Lithography Workshop
Pasadena, CA
August 28, 2001

Daniel Herr
Semiconductor Research Corporation
Research Triangle Park, NC
With contributions from:
H. Levinson and colleagues from the SRC/DARPA Lithography Network
Lithography Exposure Tool Potential Solutions

Proposed 2001 ITRS Update - Work-in-Progress - Not for Publication
Proposed 2000 ITRS Update - 7/21/00, With Proposed Two Year Cycle ( — — )

1994

1997

1998 & 1999

Half Pitch

(IRCS Proposals 7/11/00)

MPU Gate Length

(printed in resist)

(post-etch)

(IRCS Proposals 7/11/00)
EUV is expected to be the NGL lithography of choice for 32 nm and 22 nm volume manufacturing.

EUV issues include:

• Need efficient, low debris-producing EUV light sources.*
• Need for high sensitivity resists*; What is the shot noise limit?
• Measure focus errors, when the focus budget is +/- 100 nm?
• How do we measure lens aberrations in-situ?*
• Methods for identifying and mitigating contaminants on EUV mirrors in situ are needed.
• @\lambda mask defect inspection needs further development.*
• How can we make an EUV phase-shifting mask?*
• Mask Blanks*

* Research supported by SRC/DARPA
Barriers Ahead to Current Roadmap: Cost/Performance Slowdown

LITHOGRAPHY IMPROVEMENTS

$100M litho tools in ~3 generations

1.0 Cost of lithography tool ($M)

248 nm

193 nm

i-line

next generation

Courtesy of K. Brown [NIST]
Exposure tool prices over time

Historical tool prices

Short wavelength tool prices

Year

Exposure tool price

$0

$5,000,000

$10,000,000

$15,000,000

$20,000,000

$25,000,000

$30,000,000
$1.8M Mask Set, assuming 8 critical EUV layers, @ $165K/layer, and 16 noncritical layers, @ $30K/layer

Source: Brian Grenon, Grenon Consulting Inc.
Projected Mask Prices: 50 NM Node

1st vs. 3rd Year in Production

**$2.5M Mask Set**, assuming 8 critical EUV layers, at $250K/layer, and 16 noncritical layers, @ $30K/Layer

Courtesy of G. Gross
Mask vendors deny high cost

Despite all the wailing about $1M mask sets looming in the future, Photronics Senior VP Steve Carlson noted that prices for average reticles have actually increased at a slower rate than the consumer price index, or a stereo set, or pork bellies. In fact, only advanced masks have reached parity with pork bellies, while the average price actually lags the pork belly price. And I think that technology is mature,” Carlson noted at Semicon West. While prices of advanced masks increased at a CAGR of 14% over the last 10 years, the price of low-end masks actually declined.

But new technology leads to $1,000,000 pork bellies

and are increasing only at about the rate of pork bellies.

Dr. David Sachs, right, developed the strain of miniature pigs, above, as a potential source of organs for human transplant.
So, Why do users want maskless lithography?

Projected Annual Mask Costs:

**ASIC Companies:**
- ~$600 M/yr 100 nm node\(^a\)
- ~$900 M/yr 50 nm node\(^a\)

\(^a\) at one design test per day

**IC Manufacturers:**
- ~$ 90 M/yr 100 nm node\(^b\)
- ~$130 M/yr 50 nm node\(^b\)

\(^b\) at one mask set per week

Production Impact ~ $10/chip

Source: Ed Muzio, International Sematech
“Direct-Write” Maskless Lithography

What is maskless lithography?
Pattern generation on the wafer

How?
Typically viewed as e-beam turf: “EBDW”
Many proposals for multi-e-beam wafer writers as well as cell projection
But there are many other possibilities - the key is *massively parallel arrays* of writers

When?
Minimum of 5-7 years to beta tool
Fact: Strong user interest in Maskless Lithography

Nikon, Canon, Toshiba back direct write e-beam for 0.1-micron SoC production

By Jack Robertson
Semiconductor Business News
(12/08/00 05:13 a.m. PST)

TOKYO -- Direct write electron-beam lithography was endorsed at this week’s Semicon Japan trade show here as potentially "the only affordable solution" for production of next-generation 0.1-micron system-on-a-chip (SoC) designs.

Japanese lithography leaders Nikon Corp. and Canon along with Toshiba Corp. separately proposed direct write e-beam systems under ……
What is Status of Commercial Maskless Lithography?

Existing Products

Cell and Character Projection E-beam (Hitachi and Advantest, respectively)
- \(< 1 \text{ W/hr}\)
- \(> 150\text{nm}\)

High-resolution e-beam (Jeol, Hitachi, Leica)
- \(<<0.1\text{W/hr} \text{ (but very high resolution)}\)

Low resolution Optical (e.g. Intelligent Micro Patterning)
What is Status (continued) ?

Intended Products

Ion Diagnostics multicolumn e-beam (6432 beamlets)
   Funding ran out – now aimed at inspection

Etec “Microcolumn multi e-beam” (148 – 624 columns)
   Still alive, but in very early stage of development

Micronic Eximer-based “DLM” writer
   ~ 250nm resolution evolving to 150nm node
   ~ $10^6$ - $10^7$ mirrors
   ~ 5-10 W/hr goal

Canon, Toshiba direct write e-beam

Maskless Lithography: Opportunities

Direct writing exhibits the nearest term potential for prototype and development work.

With exponentially rising mask costs, @$0.5M/set today, will maskless lithography be viable for:

• Mask patterning?
• Low volume ASIC testing?
• High volume manufacturing?
Maskless Lithography: Research Issues

Energy sources*

Data Delivery: data path architecture and implementation*

Write engine: best hardware and architecture?*

Infrastructure: resists, CAD, technology, memory, computation speed, and communication*

* Research supported by SRC/DARPA
Energy Source Issues

E-beam
- TFE source: high power and short lifetime
  → Laser-photoemission source
  → Nanotube field-emitters

EUV
- Laser-plasma source: high cost
Data Delivery Challenge

Assumptions:

- Gray Scaling (about 20X penalty over MFS grid)
- 10cm²/sec write speed (~50 300mm wafers/hour)
- No overhead
- MFS = 100 nm
- Raster Scan 100% Coverage (“bit map”)

BIT RATE = \(20 \times 10 / (100 \times 10^{-7})^2 = 2 \times 10^{12}\) bits/sec

Compression is required!
Write Engine

Two Examples

- “Line Scan” using continuous source
- “Flashing Illuminator” using pulsed source

Both examples use same assumptions of last slide
“Line Scan” using continuous source

Assume maximum stage speed of 100cm/sec

Assume requirement of 10cm$^2$/sec:
  at 100cm/sec ➞ 0.1cm scan width

Assume 50nm spot size
  ➞ 2 $\times 10^4$ beams modulated at 100MHz

(or fewer “wobbled” beams modulated faster)

Redundancy requires more beams

Multipass requires more beams and/or faster scan
Flash on Fly (pulsed source)*

Assume maximum pulse rate of 10 kHz

10 cm²/sec at 10⁴ flashes/sec $\Rightarrow$ 10⁻³ cm²/flash

10⁻³ cm²/flash at 50nm spots $\Rightarrow$ 4 x 10⁷ spots/flash

Redundancy requires even greater number of elements per flash

* (See USP 5,691,541)
Maskless Lithography: Network Research Vectors

**Scanning Probes:** Demonstrate lithographic patterning with large arrays of probes scanning simultaneously, demonstrate durability of tips

**Multiaxis E-beam:** Determine limits and performance potential of several novel approaches including multi-column shaped-beam, and NEA photocathode arrays

**EUV:** Demonstrate viability of fabrication approaches, mechanical and thermal viability of sub-micrometer mirrors using both deflection and phase-modulation approaches

**Droplet-on-Demand:** Determine limits and performance of drop-on-demand jet printing and investigate applications to low-cost electronics

**Data Path and Circuitry:** Analyze tradeoffs in compression efficiency and on-chip decoding complexity & estimate feasibility and circuit complexity as limited by space and power dissipation.
Example of EBDW: Arrayed Microcolumns

Source: Phillip Chang, Etec

MICROCOLUMNS (1 TO 2 kV)
PROBE SIZE <10 nm (@ 1nA)
PROBE PITCH ~ 1cm

30 nm PMMA
1KeV
Direct Write with Proximal Probe
ZnO / PR Cantilever Design

Source: Quate group, Stanford
Distributed Axis E-beams Maskless Lithography
Direct Write with EUV: The concept

13.4 nm light-source

Condenser Optics

Mechanical scan

Wafer

“Electronic mask” is an array of tiny mirrors (10^5 - 10^8 mirrors)

“Electronic mask”

Electronic scroll of pattern

Source: Oldham group@ Berkeley & Dave Markle@ Ultratech

WGO SRC Summer Study 2001
EUV Maskless Lithography

Structure of Elastomer SLM

Reflective multilayer electrode

Elastomer electrode

Silicon Substrate

81 layers R~70%

N

Operational Principle

- When all of the pillars are of the same height, the incident light is specularly reflected.
- When the difference between adjacent pillars is $1/4 \lambda$, all of the light is diffracted and a dark pixel is formed.
- The simple structure of the pixels allows scaling to large arrays.
Fabrication of Comb-Structure Nanomirrors

Unpolished Mirror

Hinge

Maskless Lithography for Low-Cost Electronics

The Holy Grail: Reel-to-Reel Fab

Inkjet System

Inkjet System

Low cost – no clean rooms, cheap substrates

More examples of Direct-Write approaches

Zone-plate lithography (ZPAL): MIT
Droplet-on-Demand ("resist jet") Lithography: Berkeley
Near-field optical lithography: Stanford
Maskless ion-beam lithography: Berkeley

Each is a massively parallel array of writers
### Data Flow Management: Specifications

<table>
<thead>
<tr>
<th>Device</th>
<th>Direct-write</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum feature</td>
<td>50 nm</td>
</tr>
<tr>
<td>Pixel size</td>
<td>25 nm</td>
</tr>
<tr>
<td>Edge placement</td>
<td>&lt; 1 nm</td>
</tr>
<tr>
<td>Pixel depth</td>
<td>5 bits / 32 gray</td>
</tr>
<tr>
<td>Chip size</td>
<td>10mm x 20mm</td>
</tr>
<tr>
<td>Chip data (one layer)</td>
<td>1.6 TBits</td>
</tr>
<tr>
<td>Wafer size</td>
<td>300 mm</td>
</tr>
<tr>
<td>Wafer data</td>
<td>560 TBits</td>
</tr>
<tr>
<td>Writing time (one layer)</td>
<td>60 seconds</td>
</tr>
<tr>
<td>Data rate</td>
<td>9.4 TBits per second</td>
</tr>
</tbody>
</table>
Projected Compression Needs

According to 2000 ITRS:
I/O bandwidth and required data rate diverging, i.e. compression ratio growing
128 pins at 3.125 Gb/s possible by the end of 130 nm generation
Lossless Layout Compression for Maskless Lithography Systems: 50 NM Node System Architecture

- Throughput from processor board to on-chip decompress is limited (1000 pins at 400 MHz or 128 pins at 3.125 GHz)
- Real-time decompression must be done with limited on-chip circuitry; no rasterization
Compression Results

* Compression results over a 2000 x 2000 block of 5-bit gray data

<table>
<thead>
<tr>
<th>Layout</th>
<th>Rectangle</th>
<th>SPIHT</th>
<th>ZIP (LZ77)</th>
<th>2D-LZ</th>
<th>BZIP2 (BWT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>active_a</td>
<td>33.9</td>
<td>8.44</td>
<td>45.7</td>
<td>111</td>
<td>&gt; 2D-LZ</td>
</tr>
<tr>
<td>active_b</td>
<td>61.1</td>
<td>9.69</td>
<td>61.1</td>
<td>144</td>
<td>&gt; 2D-LZ</td>
</tr>
<tr>
<td>active_c</td>
<td>18.7</td>
<td>5</td>
<td>46.4</td>
<td>328</td>
<td>&gt; 2D-LZ</td>
</tr>
<tr>
<td>active_d</td>
<td>24.5</td>
<td>7.44</td>
<td>60.1</td>
<td>273</td>
<td>&gt; 2D-LZ</td>
</tr>
<tr>
<td>active_e</td>
<td>72.8</td>
<td>9.37</td>
<td>47.3</td>
<td>145</td>
<td>&gt; 2D-LZ</td>
</tr>
</tbody>
</table>

Decoder buffer requirements:
- 4 KB
- 200 KB
- 900 KB
Maskless Lithography Data Path Design

Chip Architecture

- Highly parallel architecture to meet throughput
- Writer array circuitry must be dense to fit mirrors

I/O => 128 pins @ 3.125 Gb/s
Demux + Buffer
16000 Parallel decompression paths
Writers built on compact memory array 16000 x 16000

25mm

Summary

Maskless lithography, direct write, appears to offer potential solutions that could co-exist with NGL systems.

Compatibility with the emerging NGL infrastructure will be compelling (EUV vs. e-beam).

Both the writing engine and the data-path /processing architecture are key areas for research. => \( \beta \) tool 5-7 yrs.

\[ \text{\textbullet I/O bandwidth is biggest concern, low power circuit design can reduce power consumption to reasonable levels} \]

Data flow management challenges will impact insertion options, such that maskless lithography likely will write masks and test ASICs before entering IC manufacturing.
Multi-ebeam Direct Write (MEBDW)

Aug 28, 2001
SRC/ISMT Direct Write Workshop

Mark Gesley
Purpose of presentation

- Review current progress in Multi-ebeam Direct Write (MEBDW)
- Assess what is necessary to implement the technology for 50/35nm manufacturing
- Identify what SRC/ISMT can do to facilitate technology development
Outline

■ A few assertions
■ System architecture considerations
■ Features and benefits: extended array printing
■ Risks: module technology/system engineering/product-application
■ Concept and feasibility targets
■ Progress to date
■ Timing of 50/35 nm insertion to manufacturing
■ Conclusion/Recommendations
A few assertions that influence the best path to MEBDW

- Acceptable throughput is that which will obtain sufficient sales for the required ROI
  - not necessarily set only by comparison to wafer stepper throughput
  - such comparisons set unrealistic throughput targets/expectations which can lead to incorrect technology choices

- Cost-of-ownership will determine minimum acceptable throughput as set by the
  - price/complexity/existence of the wafer stepper
  - price/complexity/existence of the mask
  - number of wafers to be printed with that mask.
System architecture considerations

- Multi-ebeam is the only path to achieve acceptable throughput
  - Single beam technology will not do better than $<\frac{1}{4}$ wph (at 100nm)

- Vector-scan multi-ebeam is not feasible for direct write
  - Insufficient control of multibeam brush printing or multiple datapaths required

- Raster multi-ebeam architecture provides
  - lower positional errors via repetitive scanning
  - necessary bandwidth and channel capacity of data handling
  - digital resolution extension through gray printing
Technical attributes: Microcolumns for MEBDW

<table>
<thead>
<tr>
<th>Feature</th>
<th>Benefit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uses gray level, multipass, Gaussian beam print strategy</td>
<td>Extends existing writing / calibration strategies</td>
</tr>
<tr>
<td>Extended array of beamlets</td>
<td>Throughput-resolution extendibility by # beamlets and density. Lowers stage velocity</td>
</tr>
<tr>
<td>No crossover in brush</td>
<td>Resolution without throughput penalty</td>
</tr>
<tr>
<td>Low voltage printing</td>
<td>Simpler datapath: no proximity or heating corrections Enhanced resist sensitivity</td>
</tr>
<tr>
<td>Thin layer imaging process/lithography</td>
<td>EUV addressing similar Process, etch, defect issues</td>
</tr>
<tr>
<td>TFE-cathodes/gun</td>
<td>Dose stability, commercially available</td>
</tr>
</tbody>
</table>
Risks

■ Module technology
  – array stability: position, dose, lifetime
  – TLI process: immunity to contamination and drift
    • Resist/etch selectivity limits of pattern transfer

■ System engineering
  – printing/calibration/diagnostic complexity;
  – datapath implementation
  – mark finding/alignment

■ Product timing for 50/35 nm

■ Product configuration
  – application development
  – requirements, implementation and use/ beta partnership
Concept and feasibility targets for 50/35 nm

- Reduce module risks
  - 320 MHz electronics, interconnect integrity
  - Robust, long-lived source and immunity to contamination and drift

- Demonstrate 50 nm array lithography capability on small 100 µm fields
  - 4-beam patterning and control
  - CD and placement accuracy with thin layer imaging and etch
  - Mark alignment capability

- Achieve full 50 nm mask patterning capability with 16 beams

- Address MEBDW system complexity concerns
  - Throughput at <<10 hr
  - Datapath capacity and bandwidth
  - Lithography quality using extended array printing

- Establish market requirement specifications
Progress to date

- System concept
- A key subsystem: the raster bit-mapped datapath
- Module-level
  - microcolumn optics
  - packaging-interconnect
- Test stand
- Lithography results
MEBDW System Concept 50/35 nm

MFS 50 nm (half pitch)  Fixed Pixel Rate 300 MHz  (Variable wafers per hour)
MIFS 30 nm (gates)

Design assumptions: Parallel calibration of columns on master plate in tool
- 40-second calibration done once per wafer
- Blaneker amplifier rise times ~ 200 ps
- 36-second load/unload and registration time

<table>
<thead>
<tr>
<th>Column footprint, mm</th>
<th>20 × 20</th>
<th>10 × 10</th>
<th>5 × 5</th>
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<tbody>
<tr>
<td>Number of inscribed columns</td>
<td>148</td>
<td>624</td>
<td>2632</td>
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<table>
<thead>
<tr>
<th>Shaped Beam (1 pass)</th>
<th></th>
<th></th>
<th></th>
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</thead>
<tbody>
<tr>
<td>Max flash size (pixels/scan)</td>
<td>50 (1024)</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>Scan length, µm</td>
<td>51.2</td>
<td>51.2</td>
<td>51.2</td>
</tr>
<tr>
<td>Pixel rate, MHz</td>
<td>300</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>Amps/col, nA (1 µC/cm²)</td>
<td>8.9</td>
<td>6.2</td>
<td>2.8</td>
</tr>
<tr>
<td>Stage speed, mm/sec</td>
<td>14.7</td>
<td>10.2</td>
<td>4.6</td>
</tr>
<tr>
<td>Write time (cycle time), min</td>
<td>9 (10.2)</td>
<td>2.4 (3.5)</td>
<td>0.6 (1.8)</td>
</tr>
<tr>
<td>Wafers per hour</td>
<td>6</td>
<td>17</td>
<td>33</td>
</tr>
</tbody>
</table>
A Key Subsystem: The Raster Bit-mapped Data Path

Variables | Store | Raster bandwidth | Memory size | Buffer size | Number of channels
--- | --- | --- | --- | --- | ---
Large memory | Low bandwidth | | | | |
Small memory | High bandwidth | | | | |
MEBDW Data Path Feasibility Study

- With commercially available parts, data delivery to the direct write tool has a throughput capacity of 10 wafers/hr under the following conditions
  - 300 mm wafer, ~600 columns
  - 25 nm printing pixel
  - Four data pixels per 50 nm beam flash at 125 MHz
  - No real-time corrections applied to the data
  - 25 × 44 mm maximum chip size
Test stand lithography with single microcolumn

- 100µm exposure field
- 25nm thick PMMA
- Blanker errors observable
- ~250 nm (2 pixel) MFS
70 nm Resolution / 1 kV exposure

- Infineon’s CARL bilayer resist
  - Established manufacturing technology
    - Since 1995, with >80,000 wafer starts for 0.5 mm lithography using i-line
  - Process
    - Image and wet silylate top imaging layer
    - Dry develop bottom hardened novolac layer

- Preliminary 1 kV e-beam CARL results
  - Sensitivity ~2 μC/cm²
  - Contrast >10
  - High resolution: 70 nm features in 35/250 nm resist
  - With ~5 nm beam, ΔCD/Δdose <0.5 nm/%dose
  - Linearity: range 7 nm
  - No proximity effects
1 kV CARL: No Proximity Effect

- 85 nm linewidth: Tower Pattern

Linewidth @ 2.6 $\mu$C/cm$^2$
40 nm resolution: HSQ

1 kV exposure. Dose ~20 µC/cm². Courtesy A. Jamison/ U. Texas
Timing risk: MEBDW

<table>
<thead>
<tr>
<th>CY</th>
<th>2001</th>
<th>2002</th>
<th>2003</th>
<th>2004</th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
</tr>
</thead>
<tbody>
<tr>
<td>SIA 3/99 Generation (nm)</td>
<td>130</td>
<td></td>
<td>100</td>
<td></td>
<td>70</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Accelerated Two-year Cycle</td>
<td></td>
<td></td>
<td>100</td>
<td></td>
<td>70</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Technology Development**
- 16 multi-e-beams
- 100–70 nm capability
- 64 beam
- 70 nm capable
- 256 beam
- 70 nm capable

**Product Development**
- MEBDW
  - 50 nm
  - 256 beam

**Commercialization**
- First beta
- 10 units/year
- 100 units/year

**Identify key technical hurdles**
- Throughput (extendibility)
- Alignment
  - Stitching
- Mark detection
- Column-column stability
- Reliability
Risk: Product configuration

- Partnership with integrated device manufacturer is needed for
  - Successful insertion into manufacturing
  - Risk reduction and R&D leverage

- $\Omega$-partner needs data and understanding of issues
  - Lengthy adoption of technology and market penetration
  - Joint tasks are complementary to those needed for advanced mask patterning
  - Helps us understand multibeam patterning technology

- What can be done now by the $\Omega$-partner?
  - Pattern transfer technology (process development)
  - Definition of requirements and experiments
Conclusions/Summary

- **Progress to date**
  - System concept/datapath developed
  - Unit microcolumn characterized: optics, package, interconnect
  - TLI process data: 40~70 nm resolution w/ no proximity effect

- **Challenges ahead**
  - Array system complexity: calibrations/diagnostics/writing
  - Applications development and impact on system requirements

- **Milestones to manufacturing implementation**
  - Existence as a mask pattern generator
  - Partnership between tool supplier and device manufacturer

- **What can SRC/ISMT do?**
  - Promote/support TLI process development
    - Resist, Etch, Defect characterization
Acknowledgements

- DARPA/NAVAIR/SPAWARS support of microcolumn technology development
- Microcolumn development team
- Andrew Jamison, Univ. Texas (HSQ development)
The present status of Canon’s ML2 technology

Nobuyoshi Deguchi
of Canon Inc.
1. Canon’s strategy of NGL Development
2. Canon’s approach to ML2
   - Background
   - Aberration Correction technology (CLA System)
   - Key Technologies / Multi EBDW
   - ML2 Tool Development Schedule
3. ML2 development status report
   - CLA development status
   - Air-guided wafer stage development status
4. Conclusion
Canon’s strategy of NGL Development

- I-line
- KrF
- ArF
- F₂
- EUV

Current = 130nm

Final Goal

Mask-less system

70nm ~

MEBDW (ML2)

SoC Market QTAT

~ 300nm ~ 150nm ~ 100nm ~ 70nm

50nm ~
Mask-Less is alternative solution

Mask crisis:
Accuracy, MEF, OPC -> impact to mask manufacturing -> Cost
Rising mask cost gives serious damage to devices of SoC (Many products/Low volume)

Features
- Multi-EB direct write system → Mask-less
- Large field size and High NA → High-Throughput
- New correction technique → High Resolution

Semiconductor Production Equipment Development Center
1. Canon’s strategy of NGL Development
   - Background
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   - ML2 Tool Development Schedule

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3. ML2 development status report
   - CLA development status
   - Air-guided wafer stage development status

4. Conclusion
### Parameters of the MEBDW system

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Accelerating voltage (kV)</td>
<td>50</td>
</tr>
<tr>
<td>Energy spread (eV)</td>
<td>2</td>
</tr>
<tr>
<td>Demagnification ratio</td>
<td>50</td>
</tr>
<tr>
<td>Convergence angle (mrad)</td>
<td>10</td>
</tr>
<tr>
<td>Individual beam size (nm)</td>
<td>$\Phi \ 17.5$</td>
</tr>
<tr>
<td>Number of beams</td>
<td>4096 (64x64)</td>
</tr>
<tr>
<td>Main-field size (um x um)</td>
<td>4.096 x 0.256</td>
</tr>
<tr>
<td>Sub-field size (um x um)</td>
<td>256 x 256</td>
</tr>
<tr>
<td>m-field size (um x um)</td>
<td>4 x 4</td>
</tr>
<tr>
<td>Focal length of the final lens [Lens D] (mm)</td>
<td>20</td>
</tr>
<tr>
<td>Focal length of the correction lens (mm)</td>
<td>100</td>
</tr>
</tbody>
</table>

2001.08.28  
Semiconductor Production Equipment Development Center
### Key Technologies / Large Field MEBDW

<table>
<thead>
<tr>
<th>Category</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>EB Source</strong></td>
<td>LaB6 (Uniformity of radiation angle, emission stability)</td>
</tr>
<tr>
<td><strong>Lens Design</strong></td>
<td>Low distortion Magnetic Lens</td>
</tr>
<tr>
<td><strong>Lens Device</strong></td>
<td>Blanking Aperture Array, Correction Lens Array, Multi Deflector</td>
</tr>
<tr>
<td><strong>Manufacturing</strong></td>
<td>Charge Up measures, In-Situ Cleaning</td>
</tr>
<tr>
<td><strong>Stage Environment</strong></td>
<td>High accuracy Air-guided wafer stage in HV</td>
</tr>
<tr>
<td><strong>Alignment</strong></td>
<td>Stitch and Alignment, Multi Beam drift control</td>
</tr>
<tr>
<td><strong>Virtual Mask</strong></td>
<td>Giga-scale Mask data handling</td>
</tr>
<tr>
<td><strong>Resist</strong></td>
<td>High sensitive Resist for higher Throughput</td>
</tr>
</tbody>
</table>
### Simulated Throughputs

<table>
<thead>
<tr>
<th>Image blur components (nm)</th>
<th>CLA system</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lens aberrations blur $s_{ab}$</td>
<td>13.7</td>
</tr>
<tr>
<td>Optical assembly tolerance blur $s_{tol}$</td>
<td>10.0</td>
</tr>
<tr>
<td>Depth of focus blur $s_{foc}$ (DZ=+/-1um)</td>
<td>5.8</td>
</tr>
</tbody>
</table>

| Resolution 100nm | Allowable image blur $s_{total}$ for 70% contrast (nm) | 33.8 |
| Resolution 70nm | Allowable image blur $s_{total}$ for 50% contrast (nm) | 29.9 |

<table>
<thead>
<tr>
<th>Components</th>
<th>100nm</th>
<th>70nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coulomb Interaction blur (nm)</td>
<td>28.7</td>
<td>23.9</td>
</tr>
<tr>
<td>Total current (mA)</td>
<td>11.8</td>
<td>9.1</td>
</tr>
<tr>
<td>Total current (mA)</td>
<td>11.8</td>
<td>9.1</td>
</tr>
<tr>
<td>Throughput (8&quot; wafers/ hour)</td>
<td><strong>59</strong></td>
<td><strong>52</strong></td>
</tr>
</tbody>
</table>

- Overhead time: 30 sec/8” wafer
- Resist sensitivity: 3 uC/cm²
- Pattern density: 50%
- Exposed area of a wafer: 240 cm²
- Lens aberration blur $s_{ab}$: standard deviation of aberration disk
EB lithography tools: **Throughput** is limited by the **Coulomb interaction effect**

Maximize the throughput for a given resolution

Minimize the Coulomb interaction effect

A much larger field size
A much larger convergence angle (NA)

Increasing lens aberrations

New corrections is required
Aberration Correction

Distortion
Intermediate Image Field
Final Image Field

Electron source
Collimator Lens
CLA
Field Curvature
BAA
Projection Optics

Electron source
Collimator lens
Aperture Deflector
Lens 1
Principal Plane
Lens 2
Fc
Image of source
Correction lens
Correction lens
Correction lens

2001.08.28

Semiconductor Production Equipment Development Center
MEBDW Tool Development Schedule

System research & Design
EB Optics Design
Assembly/DBG
Fabrication
β tool (1st Version)
Production Tool (2nd Version)
Evaluation

Basic elements
- CLA device
- EB gun
- Vacuum Stage in HV
1. Canon’s strategy of NGL Development
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4. Conclusion
Principle of CLA

- Three Electrodes
  - Voltages applied

1st electrode
2nd electrode
3rd electrode

Electron Beam

Equipotential line
Photo of the lens array

Pin
Lens holder
2nd substrate
2nd electrode
1st electrode with shield membrane
1st substrate
Base substrate
50mm
Experimental setup for Hartmann`s test

(estimation of the focal length)

gun

CL

OL

UD

Hartman aperture

Lens array

LD

Screen1

FC

Screen2

Electron beam

Vc

2001.08.28

Semiconductor Production Equipment Development Center
Details of Hartmann’s test

Electron Beam

Hartmann’s aperture

Lens

SC1

SC2

Lens OFF (30μm-pencil)

Lens ON (30μm-pencil)
Result of Hartmann’s test
(focal length of pencils)

Acceleration Voltage: 10kV

- 15μm
- 30μm

2nd electrode voltage [V] (absolute value)

focal length [mm]
Prototype Vacuum Stage

Prototype Wafer stage for High Vacuum Circumstance
Conclusion

“Mask-less Lithography” is a key word for small volume production.
- CLA can solve the aberration problems of high throughput EB optics.

CLA device development status
- Small sized lens array has been fabricated.
- Lens array is under evaluation.

Wafer stage development status
- The first trial wafer stage for the vacuum circumstance have been fabricated.
- We are developing the improved wafer stage.
The Maskless Stepper
- a Flashy New Tool

Tor Sandstrom
MICRONIC Laser Systems
The Maskless Stepper (MLS)  
- Maskless Lithography with a Difference

- Not aiming to solve the NGL quandary
- An opportunity to build  
  a maskless lithography system  
  which
  - prints identically to an optical stepper  
  - uses files on a hard-disks instead of reticles  
  - has close to perfect process compatibility with the steppers
- Current status:  
  - an ongoing joint design and market study  
    by
    - pattern generators  
    - stepper technology
Micronic’s maskwriter development

- OMEGA laser-scanning reticle writer
- New SIGMA SLM-based reticle writer
  - resolution: 180 nm
  - registration: 25 nm
  - CD uniformity: 10 nm
  - Voting: 4 pass
  - write time: 2-3 hours
**SLM-based pattern-writing**

- New deep-UV SLM-based technology for writing reticles
  - uses a micromirror chip as a computer-controlled reflective reticle
  - imaging physics is identical to a DUV stepper
  - can use 248, 193, 157, ... nm
  - throughput is only bounded by practical limitations of SLM technology and data processing

*SLM = Spatial Light Modulator*
Principle of operation

The optics of a stepper, but...

- much higher demagnification
- a reflective SLM chip in the place of the reticle
- the SLM diffracts light away from the lens aperture where non-zero data is loaded

Flash-on-the-fly:

- a continuously moving stage
- a 20 ns long excimer laser pulse illuminates the SLM and prints an image of the SLM on the workpiece
- the SLM data is reloaded in time for the next flash, 1000 times per second or more
The excimer-based flash-on-the-fly pattern generator was invented by Dr. Heinz Kück at the Fraunhofer Institute for Microelectronic Circuits and Systems in Duisburg.
Using diffraction to create contrast with < 0.1 µm of mirror movement

- When the SLM surface is flat all light is reflected in the specular direction
- A very small surface perturbation causes the light to be diffracted and the specular reflection is attenuated or extinguished
- Variable attenuation by variable non-flatness enables analog addressing for gray scale
The micromirror SLM chip

- Torsional 16 x 16 micron mirrors
- The mirrors are actuated by electrostatic force
- A matrix-addressed CMOS chip similar to a TFT screen below the mirrors

Matrix addressing of analog array
The SLM is designed to work exactly as a binary mask, but with 64-level gray.

- robust imaging with no phase effects in the image
- stability through focus
- X-Y symmetry

Mirror height map

400 nm feature through focus

- +/- 0.00 µm
- +0.17 µm
- +0.34 µm defocus
1 Mpixel Analog Spatial Light Modulator

Developed by the Fraunhofer Institute of Microelectronic Circuits and Systems, Dresden. Ackn: Hubert Lakner, Peter Dürr
Micromirror Details
Mask Clear - Dark Isolated Lines

SLM imaging
248 nm wavelength

200 nm (208)
300 nm (296)
400 nm (401)
500 nm (510)
600 nm (591)

February 2001
Starburst with 0.3 µm spokes
- data and SEM picture

- Blue: deflected = dark
- White: relaxed = bright
- Other colours = intermediate analog deflections
Hey, I am a stepper!

All my friends print on silicon...
Why can’t I print on wafers like the big guys?

Nobody would notice the difference!

Nobody would notice the difference!
Stepper/Scanner

- Wavelength: 248 nm
- NA: 0.75
- Sigma: 0.3-0.8
- Annular, quadrupole, dipole illumination
- Attenuated PSM
- Strong PSM
- Resist

SLM-based Maskless Tool

- same
- same
- same
- same
- same
- same
- option
- same
Wait a minute!

The delay times are not the same.
Identical process
- except for the delay times

- The maskless tool is one-two orders of magnitude slower than a stepper/scanner
- Writing time is 5-30 minutes, not 30 seconds
- Manual handling of wafers in low volume adds issues with contamination and varying delays
- CD control could be affected

Therefore:
- the MLS must be interfaced to a track
- workflow and delay times must be actively managed
- the AMB contamination must be well under control
- it may not be optimal to write full wafers

If this issue is kept under control you have a perfect match between reticle stepper/scanner and maskless stepper
Throughput

- The throughput of a modern stepper with 120 WPH @ 300 mm and 110 nm L/S corresponds to 1000 billion gray-scale pixels per second, or 1000 Gpel/s
- Micronic’s current SLM engine prints 1 Gpel/s
- Does a slow tool have a market?
- Yes, even a slow tool that produces expensive wafers can save time and money!
How can a slow and expensive tool save time and money?

Because wafers have two types of value:

**Use value**
- Value per wafer: based on selling price
- Proportional to production volume
- Memories, MPUs, ASICs, etc.

**Intellectual value**
- Value per wafer: based on knowledge and timing, can be very high
- Independent of volume
- Customer samples, engineering prototypes, redesign confirmations, design iterations, parameter mapping, process development experiments
Half of all reticles print only one wafer lot
Economy of replacing reticles

- If you only need one state-of-the-art wafer to confirm a design, that wafer may cost 500,000 $ in reticle cost.
- Writing it in a maskless tool for 100,000 $ would be a bargain.
- At 10,000 $ per wafer you are in the realm of profitable small-volume production.
- For best economy only some layers are maskless, since non-critical reticles are inexpensive, quick to get and are used late in the process.
- Optimizing within the maskset extends the economic use of maskless lithography to more products, but with fewer substituted reticles in each maskset.
The cost is doubly high for the critical layers.

- Performance
- Cost
- Time to market

Critical layers dominate the cost, with a particular emphasis on reticle lead time.
At some limit maskless becomes desirable

- ML better
- Reticles better
- Cost of reticle lead time
- Critical
- Subcritical
- Non-critical
- 2 WPH
- 10 WPH

MICRONIC LASER SYSTEMS
A mix of masksets

Reticle cost per wafer

Cost of reticle lead time

ML better

Reticles better
Design study - basics

- 300 mm wafers per hour: 2
- Lines: 130 nm
- L/S: 130 nm
- NA: 0.75
- Wavelength: 248 nm
- Sigma: 0.3 – 0.9 variable pattern
- Projected pixel size: 50 x 50 nm
- Address grid: < 1 nm
- Pixels per second: 30 Gpel/s, double-pass
Focus on CD control

- CD control is paramount. No tool is good enough on CD control.
- For maskless lithography we are implementing:
  - 2-pass voting
  - field blending
  - flash energy correction
  - analog calibration of every mirror’s transfer function
- Data integrity and rasterizing accuracy is an absolute requirement
Individual mirror correction

- All mirrors are characterized optically. Their transfer function is measured and stored in a large look-up table, LUT.
- The LUT is applied in real time during writing.
- Calibration removes errors and drift in:
  - transistor parameters
  - hinge stiffness
  - mirror reflectivity
  - illumination uniformity
  - analog electronics hardware
Pixel calibration hardware

- The geometry is converted to a bitmap
- The bitmap is fed to DACs driving the SLM
- But first it is converted by means of the large look-up table containing the transfer functions of the individual mirrors

**Diagram:**
- Geometry data
- 6 bit deep bitmap
- Map of pixel transfer functions
- Gray value
- DAC value
- DAC
- Mirror voltage
- SLM
Rasterizing precision

- The maskless stepper will write from a reticle pattern file including
  - serifs
  - scatter bars
  - other OPC features

- Some OPC features are the size of one pixel or less. The rasterizing algorithms must represent them accurately.

- Current algorithm inaccuracy:
  - line edge position: < 0.5 nm
  - corner position: < 1.0 nm

- Very small features are represented by a larger gray area. The gray must represent the small feature optically. This is currently the subject of a special study.
Can the data flow be managed?

- 30 Gpel/s means 30 Gbyte/s bitmap data into the SLM (sustained average over 24 hours).
- Although challenging, this can be met by Micronic’s current rasterizing architecture.
- Bottlenecks are anticipated in input data transfer and conversion, and in the analog feeding of data to the mirrors.
- An engineering effort is undertaken to alleviate the anticipated bottlenecks.
- There is also room for the further improvements as required by Moore’s Law and industry roadmaps.
Can 30 Gb/s be compared to something?

- 30 000 Ethernet cables @ 10 Mb/s
- 600 000 ADSL lines
- 6 000 000 V90 modem connections
- 600 computer-generated TV screens
- 0.5 WDM fiber-optical link

= 30 Gbyte/s
The Maskless Stepper - Outlook

- Uses for maskless lithography
- Bonus effects
- Vision
Where could the maskless stepper be used?

<table>
<thead>
<tr>
<th>Type of application</th>
<th>Technology level</th>
<th>Driving force:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology development</td>
<td>Bleeding edge</td>
<td>Enablement</td>
</tr>
<tr>
<td>• before steppers are available</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• in lack of good reticles</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Process development</td>
<td>Leading edge</td>
<td>Time to market</td>
</tr>
<tr>
<td>• parameter space mapping</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Product development</td>
<td>Mainstream</td>
<td>Time to market</td>
</tr>
<tr>
<td>• Quick-turn prototypes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Confirmation runs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Shrinks and design tweaks</td>
<td>Leading to trailing</td>
<td>Production economy</td>
</tr>
<tr>
<td>• Parameter tryout, e.g. analog or OPC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low-volume production</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• replacement of low-run reticles</td>
<td></td>
<td>Opportunity</td>
</tr>
<tr>
<td>Niche applications</td>
<td>Leading to trailing</td>
<td></td>
</tr>
<tr>
<td>• individual chip codes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• semi-custom personalisation</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Time to production – time to market

- A strong trend is faster ramp-up of equipment, fabs and products
- The maskless stepper can help by short-cutting lead times and increase the number of learning cycles

Proposed ITRS Fab Ramp Model

100 wafers/week = 10K-25K Die/week
(©170mm² die size)

Time to Reach 100% Capacity
Bonus 1 – Reduced uncertainty

- If an ASIC design is anticipated to need one or two redesigns, the high cost of reticles leads to economic uncertainty
- Maskless prototyping can act as an insurance
- The risk of excessive reticle cost is reduced
- The cost of the insurance is that the final reticles are produced only when the design correctness has been verified
Bonus 2 – More design evolution

- Maskless lithography makes process experiments, design iterations, and redesigns less expensive.
- One more process experiment may give a higher-yielding, more capable process.
- One more design iteration may improve the product, increase customer value and increase yield
- One more redesign during the lifetime of a product may prolong its economic lifetime and improve the product economy
**Bonus 3 – Faster learning cycles**

- When a mask set costs 500,000 $ the number of learning cycles has to be reduced.
- Relaxing the economic restrictions on engineering prototypes lead to faster learning
- Faster learning is a stimulus for the entire technology, leading to better processes, faster ramp-up, higher quality and better performance
- The end result is better product economy
Bonus 4 – Improved mask technology

- The maskless stepper shares its technology base with Micronic’s mask writers.
- A larger combined machine base leverages the SLM and datapath development efforts and improves quality, performance and throughput also for mask writers and guarantees the development of the necessary basic technology.
- More maskless steppers means better and faster reticles as well.
Why will the maskless stepper not fail like many direct-writing efforts have done in the past?

- The cost structure is different: the 1 M$ mask set is a reality
- The semiconductor world is larger and more segmented than it has been
- Control of production cost and lead times is more important than ever before
- Process compatibility has never before been possible
- The SLM technology is optically identical to the stepper
- The SLM technology gives higher throughput than other technologies
Summary

- The Maskless Stepper may change the rules of semiconductor development and production
- This could be a stimulus to the industry as a whole
- To the fabs it would bring a whole new freedom leading to:
  - faster and more efficient engineering
  - better productivity
  - new capabilities
- And it appears to be perfectly feasible
The future: Simulated 40 nm semi-dense lines using 157 nm and a micromirror SLM
A thought experiment!

- Time is 2004. You are building a fab for the next technology level.
- In “The Big Fab-builder’s Mail-order Catalog” there are:
  - steppers running 100 WPH
  - maskless steppers running 2 WPH
  - everything else needed for the fab
- The maskless steppers are at the same level as the steppers in terms of
  - process capability
  - reliability
  - user-interface, factory integration, etc
- What would be your mix: 10 to 1, 1 to 1, 1 to 10?
- What would you use maskless lithography for?
- Mail me your comments: <sandstrom@micronic.se>
Massively Parallel Direct Write E-Beam System

H.F. Lockwood*
Emission Systems, LLC

W.B. Feller, P.L. White, P.B. White
Nova Scientific, Inc.

*hlockwood@emissionsystems.com
Conclusions

• Massively parallel system appears feasible

• Multi-generation technology

• Attractive cost of ownership
  – Low initial cost
  – Relatively small footprint
  – Simple maintenance

• Virtual Mask - new paradigm for Semicon industry
Integrated Electron-Beam Source Cartridge

- Maskless, Direct-Write E-Beam Tool
- Thousands of micro-beams
- Field Emission Array combined with Microchannel Amplifier Array for stable, low-current operation and long-term reliability
- Integrated Micro-Column electrostatic lens array
- Patterning to 70 nm and below
- Short excursion (< 500 µm) stage travel for large area patterning
- Compact 25 mm high assembly
- Scalable to any wafer diameter
- High throughput potential
Microchannel Amplifier Operation
MCA Transfer Characteristic

![Graph showing transfer characteristic of MCA with linear, saturated, and operating points labeled.](image-url)
MCA Schematic

Issues

- Angular Distribution (ADOE)
- Energy Distribution (EDOE)
- Thermal Dissipation
- Modeling/Design
Si MCA Gain Comparison with Glass MCP
Effective L/D = 10:1

- **Si MCA (measured)**
- **Lead glass MCP (typical)**

- e- input: 300 eV
Einzel#4 Alignment:
EBLA#2, 1, 3 & CLA#2

Wafer 1-2 Translational Offset
Translation Uncertainty
Maximum Rotation Error

Wafer 1-3 Translational Offset
Translation Uncertainty
Maximum Rotation Error

Wafer 1-4 Translational Offset
Translation Uncertainty
Maximum Rotation Error

Wafer Order
"EBLA#2": bottom (1)
"EBLA#1": middle (2)
"EBLA#3": middle (3)
"CLA#2": top (4)

Wafer Offsets (µm)
"EBLA#2": \( x = 0.0 \ y = 0.0 \ \theta = 0 \ \text{µradians} \)
"EBLA#1": \( \Delta x = 0.2 \ \Delta y = -0.4 \ \Delta \theta = 16 \ \text{µradians} \)
"EBLA#3": \( \Delta x = -0.4 \ \Delta y = 0.1 \ \Delta \theta = 6 \ \text{µradians} \)
"CLA#2": \( \Delta x = 0.1 \ \Delta y = 0.4 \ \Delta \theta = 11 \ \text{µradians} \)

EMISSION SYSTEMS, LLC
ML2 Workshop, 28 August 2001
Proof of Principle Completed

• Design and build new generation Si MCA
  – All CMOS-type processing.
  – Gain, noise, brightness.

• Design and build EBLA
  – Manufacturability

• Integrate components into Source Cartridge

• Pattern features at < 100 nm
Proof of Lithography

Issues

- Optimize MCA design
- Incorporate deflection in EBLA
- Demonstrate wafer throughput > 100 wph for 300 mm wafers
- Writing strategy (Key: redundancy)
Wafer Throughput
Without Deflection

With $S = 1 \mu\text{C/cm}^2$ and $i = 80 \text{ pA}$, $t = 0.25 \mu\text{s}$

Table speed $= 200 \text{ mm/s}$, $a = 1 \text{g}$

Wafer throughput $\approx 10 \text{ wph}$
Wafer Throughput
With Deflection

Orthogonal displacement = ± 2.5 µm (± 50 pixels)

Table speed = 2 mm/s, a = 1g

Wafer throughput > 140 wph

Deflection frequency = 40 kHz

(Preliminary EBLA design complete)
Writing Strategy

• K6-2 poly Si gate-level file is 800 MB corresponding to total information rate of 800 MB/25 s = 32 MB/s. Redundancy is key.

• To write single line across 300 mm wafer (6 Mp) requires only 600 bits.

• Writing strategy should look to global change of state with each clock cycle rather than change in every pixel.
Conclusions

• Massively parallel system appears feasible
• Multi-generation technology
• Attractive cost of ownership
  – Low initial cost
  – Relatively small footprint
  – Simple maintenance
• Virtual Mask - new paradigm for Semicon industry
Massively Parallel Digital Electrostatic E-Beam Array Lithography (DEAL)


(1) Solid State Division
(2) Fusion Energy Division
(3) Instrumentation and Controls Division
(4) Engineering Technology Division

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OUTLINE

• Overview: DEAL Concept and Capabilities

• System Design
  – Digitally Addressable Field Emitter Array (DAFEA) concept
  – On-chip electrostatic lens concept

• Key Research Objective for DEAL and Approach

• Recent Accomplishments in Field Emitter Array Development
  – Deterministic growth of individual vertically aligned carbon nanofibers (VACNFs) in arrays
  – VACNF field emission (FE) properties and modeling (Part 1)
  – Fabrication of gated electrode (diode and triode) structures
  – Growth of single VACNFs centered in electrode wells
  – First demonstration of gated control of FE from VACNF emitters
  – Shape control for VACNF emitters

• Plans for Future Development
Digital Electrostatic E-Beam Array Lithography (DEAL)

DEAL CONCEPT

• Based upon massively parallel electron beamlets emitted by a digitally addressable field emission array (DAFEA)

• Internally funded research initially focused on e-beam transport and emitter materials studies, resulting in an enhanced concept without the need for magnetic lenses, enabled by the high density of emitters

• Current research (supported primarily by DARPA) focuses on development of the DAFEA structure using carbon nanofiber emitters
DEAL Highlights

- [1] **Maskless technology:** A fully digitally programmable “virtual mask”
- [2] **High wafer throughput with minimal wafer motion**
- [3] **Reliable:** Every pixel redundantly illuminated by multiple e-beams
- [4] **Ultimately scalable to 10 nm feature size** (5 nm pixels)
  - High density of emitter cathodes, integrated with on-chip electrostatic focusing
    - No need for beam deflectors or separate beam blankers
- **Optional additional functionality possible:** An integrated high-speed SEM
  - Absolute reliability in writing and verifying pixels
  - Independent use for massively parallel wafer metrology and inspection
System Design Solves Many Lithography Problems

- *Completely maskless* lithography: Low cost of ownership and operation

- *No space–charge limitations* at lithography currents because *no magnetic lens* is required -- *entirely electrostatic focusing*

- *On-chip* electrostatic lens system *integrated* with the DAFEA focuses electron beamlets individually (1 nA writing current)
  - Design calculations: *Pixel sizes of 20 nm to 5 nm (WD = 100 μm)*
    *Feature sizes of 40 nm to 10 nm* (WD = working distance from emitter array to wafer)

- *Great depth of focus*: ± 10 μm at assumed WD = 100 μm
  (but other design points possible)

- The DAFEA provides *great redundancy* of resist illumination, with 8 to 10 emitters illuminating every 10-nm pixel on the wafer

- *High throughput*: A 460–chip (1-cm² chips) DAFEA array could write an entire 300-mm wafer in 45 seconds with 30-nm pixels and redundant illumination (up to 80 WPH)
Massively Parallel Electrostatic DAFEA / SEM Array

- One optical fiber per DAFEA
  Data rate ~ 1 Gbyte/s/fiber

- 30 buttable DAFEAs / row
  10 rows per system

- DAFEA Array
  Two Beamlets out of $10^6$/Chip
  Tilt angle ~ 0.4°
  Stage movement

- Wafer stage is ~100 µm from the DAFEA array

- Because of their slight offset (resulting from the tilt angle), these beams can redundantly write die immediately upstream as the wafer is translated by the linear stage

- This redundancy can compensate for multiple bad emitters and opens the possibility of grey-scale illumination
The LMCD circuitry beneath each emitter is not shown, nor is the split-ring detector at the top of each focusing stack (to implement the in situ SEM function).

Proposed CNF point-source emitter looks entirely feasible.
Important Features: Design Calculations for Electrostatic Optics (Electron Beamlet Extraction, Acceleration, and Focusing)

- **No space charge limitation** because of small current (~1 nA)
  - Emitter beams do not “blow up” over 100-μm length
  - On average *less than one electron* in beam path at any time

- **Lots of “overhead”** for modifying exposure conditions
  - Assumed operating conditions:
    1 μsec / illumination @ 10 KHz (only 1% duty cycle) and 1 nA

- **Time-avg current** ~ 30 μA per 1-cm² DAFEA chip (~ 3 x 10⁶ emitters)
  - 460-chip array produces ~14 mA (time-average)
  - ~100X SCALPEL ⇒ *comparable increase* in throughput (?)

- **Design Calculations**
  - Electric field strength limited by dielectric breakdown to 100 V/μm
  - Focused electron beamlet *spot sizes of 20 nm to 5 nm* at WD = 100 μm
    (40 nm to 10 nm feature sizes)

- **Write with nominal electron beamlet energy of 200–300 eV**, eliminating the proximity effect
Recent Accomplishments in Field Emitter Array Development

Key Research Objective for the DEAL Concept

A reliable, stable solid-state emitter, lithographically placed at each site of a massively parallel array

- Deterministic growth of individual vertically aligned carbon nanofibers (VACNFs) in arrays
- VACNF field emission (FE) measurements and modeling (Part 1)
- Fabrication of gated electrode (diode and triode) structures
- Growth of single VACNFs centered in electrode wells
- First demonstration of gated control of FE from VACNF emitters
- Shape control of VACNF emitters to tailor FE characteristics
Highly Deterministic Growth of Individual VACNFs Has Been Achieved and Used for Array Fabrication

VACNF Growth Is Deterministic

- Catalyst dot pattern: VACNF location
- Nanodroplet size: VACNF tip diam
- Growth time: VACNF height
Two Critical Tests

• Amount of misalignment between EBL and PL steps
• RIE must uncover Ni dots, to catalyze VACNF growth

Results

• Measurements made after calibrating SEM to 300-nm periodic grating
• Typical misalignment < 50 nm (< 5% of aperture diameter) averaged over ~ 50 devices
• Misalignment of EBL and PL steps is no longer an issue
• A self-aligned process is not needed
Proof that

- Two lithography steps placed Ni catalyst dot near center of the aperture
- RIE released Ni dot from PECVD oxide, to catalyze growth of a single, isolated carbon nanofiber
  \[ h \approx 950 \text{ nm} \]
  \[ r \leq 17 \text{ nm} \]

Both critical tests are met
Post-Etch Image of Triode Structure

Best-case alignment shown, overlay < 50 nm
Worst case observed ~ 100 nm

Ni catalyst dot
Lower gate
Upper gate
Three SMUs: Independently monitor gate and anode currents

Anode: 700 µm from gate and at +100 volts (collect FE current)

Gate grounded, cathode swept 0 to –100 volts (control FE current)

VACNF in 2-µm diam x 1.5-µm deep electrode well:
- Turn-on electric field (1 nA current) = 80 V/µm (–85 V_{cathode})

Reproducible, gated control of field emission from a vertically aligned carbon nanofiber emitter
Reduced FE Turn-On Field and Fowler-Nordheim Behavior After Initial Operation

- Measure FE I-V after 20 minutes constant-bias testing, with 22 MΩ series ballast resistor
- Turn-on field (1 nA emission) decreases to 60 V/µm
- Fowler-Nordheim plot shows straight-line behavior expected for field-emitted electrons
- More than 99% of field-emitted current goes to anode, less than 1% to gate
Controlling the Shape of Nanostructures in a Large-Scale Synthesis Process

• Dynamically change growth conditions to produce cylinder-on-cone geometry

• Cone: Mechanically robust base

• Cylinder: Narrow tip for field emission

• Permits controlling aspect ratio (height / tip radius), to optimize shape for field emission

Growth of Cylinder-on-Cone VACNFs
Current and Near–Future R&D

- *Electrical* (turn-on field, stability, lifetime) / structural / compositional characterization to determine and optimize FE from VACNFs. Determine optimum growth conditions for FE.

- Reduce height \( h \) and tip radius \( r \) of VACNFs while maintaining or increasing aspect ratio \( h / r \).

- Develop experimental facilities: (1) wafer-scale growth; (2) rapid, simultaneous FE measurements for VACNF arrays.

- Continue developing lithography and processing to fabricate higher aspect ratio and more complex electrode structures.

- Seek industrial partners
  - Leverage ORNL research capabilities
  - Move toward prototype DAFEA chips and a tool
Summary
Field Emitter Array Development

- Highly deterministic (catalytically controlled) growth of large arrays of individual vertically aligned carbon nanofibers (VACNFs)
- FE measurements for VACNFs are in reasonable agreement with Fowler-Nordheim modeling
- Fabrication of gated electrode (diode and triode) structures
- VACNFs centered in electrode wells
- Reproducible, controlled FE from gated arrays of VACNF emitters
- VACNF emitters’ shape can be controlled and tailored for FE
- VACNFs are robust to processing steps and promising as field emitters
DEAL Summary

- A massively parallel, maskless, direct-write Digital E-beam Array Lithography (DEAL) system appears feasible.

- Large areas may be written on wafers with multiple Digitally Addressable Field Emitter Array (DAFEA) chips.

- Design tradeoffs permit scaling at 60 WPH from 40-nm features/linewidths down to 10-nm features/linewidths.

- Industrial partners (a DAFEA chip fabrication partner and a tool partner) are needed now to transform this R&D effort into a prototype tool.
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- Cornell Nanofabrication Facility
- Professor David Joy (U. Of Tennessee / ORNL)
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Electron Source Technology and Massively Parallel Digital Electrostatic E-Beam Array Lithography (DEAL)


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(4) Engineering Technology Division

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OUTLINE

• Electron source technologies
• DEAL Concept and Capabilities
  – Digitally Addressable Field Emitter Array (DAFEA) concept
  – On-chip electrostatic lens concept
• Current Research Objectives and Approach
• Recent Accomplishments in Field Emitter Array Development
  – Deterministic growth of individual vertically aligned carbon nanofibers (VACNFs) in arrays
  – VACNF field emission (FE) properties and modeling
  – Fabrication of gated electrode (diode and triode) structures
  – Growth of single VACNFs centered in electrode wells
  – Shape control for VACNF emitters
  – Advantages and feasibility of growing the VACNF array first
• Plans for Future Development
Electron Beam Source Requirements for Maskless Lithography

- **Brightness** - high brightness needed (> $2 \times 10^6$ A/cm$^2$/sr @ 50kV) dose of 1-10 μC/cm$^2$ required

- **Low energy spread** – to minimize source divergence need < 1eV

- **Stability** – 3% variation over a 12 hr period desirable

- **Lifetime** - ~ 1 yr for an economic lithography tool

- **Uniformity** - variations of a few % in brightness between multiaxis sources

- **Modulation** – switching times of 10-100 μs needed for high throughput capability
Electron Beam Sources for Maskless Lithography

- NEA Photocathode
- Amorphous Diamond (aD, DLC) Field Emitters ($\Phi \sim 4\text{eV}$)
- Carbon Nanotube/fiber (CNT,CNF) Field Emitters
- Schottky W Zr
- Thermionic LaB$_6$ W
- Spindt tips Mo Si

- Cold-Cathode Field Emitters

- A variety of electron source technologies have been examined for maskless lithography
Photocathode Sources

• **Principle of operation** –
  - Photons from a laser are incident on a thin film causing electrons to be emitted with $E_m = h\nu - \Phi$

• **Properties** -
  - Materials: GaAs, GaAsP, GaN, Au (Cs+O activation used for negative electron affinity (NEA))
  - Quantum efficiency determines brightness (cesiated GaN for instance can be ~50%).
  - Low energy spread $< 1$ eV

• **Current research** –
  - Overcome Cs depletion and trapped electrons

• **Research groups**: Stanford Univ., Intevac, OGI, Etec, ...

• **Other applications**: intensifiers (night vision), accelerator sources, astrophysics detectors

• **Enough parallel sources for high throughput maskless EBL?**
Schottky Field Emitters

- Principle of operation –
  - Electrons are emitted from the tip due to both thermal excitation and the electric field from an extractor electrode
- Properties -
  - Predominant electron source technology
  - Materials: Tungsten wire heated to 1800 K
  - High brightness (> $1 \times 10^8$ A/cm$^2$/sr)
  - Low energy spread $< 1$ eV
  - ~1% RMS current stability
  - Service life > 1 year
- Suppliers and users: FEI, YEO, Etec, ...
- Other applications: SEM, TEM, etc.
- Enough parallel sources for high throughput maskless EBL?
Thermionic Emitters

- Principle of operation –
  - Electrons are “boiled off” of heated emitter
- Properties -
  - Mature electron source technology
  - Materials: Tungsten, LaB$_6$, > 1500K
  - High stability and low thermal noise
  - ~1% RMS current stability
  - Moderate brightness (~ 1x10$^5$ A/cm$^2$/sr/kV)
  - Service life ~ 1000 h
- Other applications: Vacuum tubes, CRTs, ...
- Enough parallel sources for high throughput maskless EBL?
  - ~1000 times larger than Schottky emitters or cold cathodes
Spindt Tip Field Emitters

- Cold-cathode principle of operation –
  - Electrons tunnel through surface potential barrier with strong applied electric field

- Spindt tip emitters developed for miniature parallel arrays

- Properties:
  - Materials: Mo, Si
  - Good performance in UHV
  - Large-scale fabrication is possible

- Poor environmental stability
  - Recent example: short lifetime of Motorola’s field-emission display based on Mo field emitters
Silicon Field Emitters (Fabrication & Performance)

- Variation of Spindt tip using Si
  - Utilizes standard semiconductor processing

- Good performance in UHV

P ~ 10^{-9} Torr

Spindt Tip Field Emitters (Summary)

- High level of integration
- High current densities
- Low power consumption
- Poor environmental stability of Si and Mo tips due to ion bombardment and surface chemistry (oxide formation, adsorbates)

Si tip exposure to O
Carbon Fiber Field Emitters

- Carbon fibers have been examined for cold cathode FE applications for more than 20 yrs.
- Excellent environmental stability and lifetime!

\[ P \approx 1 \times 10^{-6} \text{ Torr} \]

\[ RT \quad 1100 \text{ K} \]

\[ RT \quad 100 \text{ MOhm} \]

(F S Baker, A R Osborn and J Williams)

Figure 2. Diagram of ‘corona etching’ apparatus.

Figure 11. Lifetime–pressure curves for carbon-fibre and tungsten field emitters.
Carbon Nanotube (CNT) Field Emitters

- More recently carbon nanotubes and nanofibers have been examined for cold cathode FE applications.
- Very promising FE properties
Field Emission Display with CNT-based Cathodes (Samsung)

- Resistance to sputtering and chemical inertness of carbon: Excellent environmental stability
- High aspect ratio of CNTs: Low FE turn-on field
- Problem: multiple emitting sites in each cathode => difficult to produce a well-focused electron beam
Vertically Aligned Carbon Nanofibers (VACNFs)

- VACNFs have been developed in an attempt to produce the ideal field emitter
  - Resemble multi-walled CNTs, but smaller grain sizes due to lower temperature growth
- Deterministic growth of VACNFs: fabrication of highly integrated gated cathode structures is possible
- Single VACNF tip per cathode: a well-focused electron beam can be produced
- High aspect ratio of VACNFs: low FE turn-on field
- Resistance to sputtering and chemical inertness of carbon: long lifetime

Field Emission as a Function of Carbon Nanofiber Aspect Ratio \((h/r)\)

- The electric field at a sharp tip on a shank is given by
  \[ E_{\text{local}} \sim \left( \frac{h}{r} \right) E_{\text{applied}} \sim \beta E_{\text{applied}} \]
  where
  \(E_{\text{local}} = \text{tip electric field}\)
  \(h = \text{height of the shank}\)
  \(E_{\text{applied}} = \text{applied voltage / distance}\)
  \(r = \text{tip radius}\)

- For 10-nm tip diameter CNFs this implies emission at \(\sim 8\ \text{V/}\mu\text{m}\) (scaling from 25 V/\(\mu\text{m}\) for 30-nm tip diameter) \(\text{if } h = \text{constant}\)

- A 5 volt grid potential at 500 nm separation, driven by CMOS circuitry, would control such a VACNF emitter
Field Emission Measurements of Isolated VACNFs Reveal Expected Emission Characteristics

- Analyses of I–V characteristics imply a Fowler-Nordheim like tunneling emission mechanism
- Emission turn-on fields \( \sim 10\text{-}60 \text{ V} / \mu\text{m} \) \( \propto r/h \) as expected
  - Slightly higher than expected from Fowler-Nordheim theory assuming emission from entire tip radius
  - VACNFs exposed to reactive ion etch (RIE) have lowered emission threshold
Lifetime of Field Emission from Isolated VACNFs

- **Lifetime:** Stable CW field emission operation at 10 nA measured for > 175 hours for isolated ORNL VACNFs
  - Threshold changes shown in plot for 20 hrs
  - Japanese group [ APL 76, 1776 (2000) ]: 7500 hours CW with MWCNTs

- **Intrinsic** environmental stability of FE from carbon (nanotube) emitters
  - SWNTs much less sensitive to environment than metallic emitters
  - No current runaway / arcing: Unballasted operation
  - Stability: Low sputter yield; low C-atom mobility; strong bonding
Electron Sources - Summary

• Conventional source technologies have promising characteristics for maskless lithography applications.
  – In particular photocathodes and Schottky emitters look attractive
  – Can these sources be configured to produce enough parallel beams to make maskless lithography attractive?

• Newer carbon nanotube based field emitters are starting to look attractive for massive parallel applications
  – Stay tuned as this technology develops
Maskless Lithography Data Issues:

What’s in a Mask?
The Mask is a Data Storage Device

- Storage capacity
- Transfer rate
- Physical representation transformation
- Physical size constraints
- Reliability (Data Integrity)
What is the pixel size?

- The pixel size is NOT the MFS
- It is also probably not a “rule” based on MFS
- A rule based on CD control required
**Mask Storage Capacity**

Assume:

- 6.25 square cm chips
- AU = 1/2 CD control tolerance

*We need Data Compression!*
What Does Gray Scaling Do?

Assume:

2 gray pixels/MFS  
16 levels (5 bits)/pixel

This we can probably do!

Gray Scale Tera-Bits per Chip

Keith Standiford, Consulting Services
Transfer Rate – Throughput Requirements

Assume:

300 mm wafers  30 seconds “beam-on” time

We (still) need Data Compression!
Try Gray Scaling Again

Assume:
2 gray pixels/MFS 16 levels (5 bits)/pixel

This begins to make me nervous!
Can We Get 5 Tb/sec of Data?

• **Current B/W**
  - 25 Gb/sec (Rambus)
  - 20 “systems”/Tb/sec — 100 “systems” for 5 Tb/sec
  - *May be do-able*

• **Data compression**
  - Loss-less methods
  - 10 – 100 fold compression reported
  - 2 – 20 systems for 5 Tb/sec
  - *This we could do*

• **Data transmission**
  - 5 – 50 channels at 10 Gb/sec
  - *This we could also do*
Clock Rate – an aside ...

Gray Pixel Rate = number of beams $\times$ beam clock rate
Physical Representation Transformation

What?!?

- Data must be transformed from its form of physical storage to some representation which will alter the physical properties of the wafer in order to affect the pattern transfer for lithography.

- **Masks:**
  - Data stored as clear/opaque spots (or scattering, phase shifting, reflecting, etc.)
  - Transformed to presence or absence (or interference) of radiation at the wafer

- **Mask-less:**
  - Electronic data storage and transmission
  - Transformed to (insert method here) at “print head”
Physical Size Constraints

- Masks are “about the same size” as wafers
  - Imaging physics
  - Fabrication practicalities

- Mask-less size varies with printing physics
  - Chip Scale methods – 1X printers
    - Ink jets
    - Nano-probes
  - Wafer scale methods
    - Stripe, sub-field or chip printing reduction methods
    - Micro-columns
    - Hybrids – multiple “chip scale” copies
**Required Functionality**

- Receive compressed data
- Expand compressed data
- Implement gray scales  
  - DAC, pulse width modulation, etc.
- Implement the “actuator”
- “Drive” the “actuator”  
  - Blanker, mechanical deflector, etc.
  - Deflection drives, source power, etc.
- Connect to the “actuator”  
  - N wires per channel

⇒ It all has to fit in the available space!
Wafer Scale Space Budget

In a 300 mm diameter, how much space can we afford?

Remember: EVERYTHING has to fit. This is actually hard!
Chip Scale Space Budget

In a square 25 on a side, how much space can we afford?

![Graph showing Square mm/Function/second vs. Node]

Remember: EVERYTHING still has to fit. This is even harder!
Reliability (Data Integrity) for Masks

Masks are not really very accurate!

• **Characterize data storage accuracy**
  - CD measurements
  - Overlay measurements
  - Defect inspection/repair
  - Yield characterization

• **Monitor and preserve integrity**
  - Pellicles
  - Periodic re-inspection

⇒ Masks are quite “non-volatile” storage!
Mask-less Accuracy and Integrity

Mostly thought of as “actuator” issues:

- Variations in:
  - placement
  - delivered “dose”
  - etc.

- Functionality
  - do they all actually work?

- Usual solution is redundancy
  - Average out the errors
  - A strategy for “dead pixels”
    - Average them out
    - Overlap to write them with a good one
    - Note: Stuck “ON” is harder to overcome!
What About DATA Integrity?

This question hasn’t been asked much!

- We have Tera-bits of data transmitted and processed for every wafer.
- We have thousands up to millions of data channels at the “print head”.
- Data integrity is no longer guaranteed by just preserving a physical structure.
- Data handling faults can destroy weeks worth of WIP before discovered at final probe.
- Why hasn’t this come up with masks?
  - Number of probes is small enough that intermittent faults still make lots and lots of errors
  - Mask inspection finds most of the errors, eventually!
Mask-less Lithography Needs Fault Tolerance!

MORE than just fault detection...

• Manufacturing yield will demand fault detection

• Reliability, maintainability, serviceability demands fault tolerance
  - Uptime requirements
  - Overall system complexity

• How far down into the system?
  - Data transmission
  - Data expansion
  - Actuator function

• It still has to fit in the available space!

⇒ This is hard, but without it we have a showstopper
Summary

We have examined replacing the mask as a data storage device:

- Storage capacity: probably OK
- Transfer rate: probably OK
- Physical representation transformation: technology dependent
- Physical size constraints: looks difficult
- Reliability (Data Integrity): difficult, largely unexplored
Your Job Today...

• **Listen critically!**
  – Are the programs tracking the needs of the industry?
  – Are the program timing and requirements meeting your expectations?

• **Develop opinions**

• **Constructively feedback in afternoon sessions**
  – Provide feedback on technology progress
  – Provide areas of further work (Critical Issues) that need to be addressed
Now our job....

• We thank you for participating!

• We will:
  – Post presentations to SRC/ISMT web
  – Roll up results and distribute to participants
  – Develop action plan that responds to your feedback
  – Continue to monitor programs & determine how/where we can affect technology development
  – Continue to include world-wide programs
  – ISMT/SRC will work together to continue industry involvement

• Reception @ 6:00 in the Horseshoe Garden Terrace
The rest of your job....

- If you have not already given us a soft copy of your presentation, please do so by the end of this week.

- Send it in either PowerPoint or Acrobat .pdf format to: judy.behr@sematech.org
2001 Maskless Lithography Critical Issues

- Economic analysis including: CoO, Cycle time, Market segment and application
- Data path/flow issues including compression/decompression and redundancy
- Simultaneous calibration and control of many beams
- Demonstration of working scalable system
- Define verification and inspection steps unique to ML2
- Thin resist development (low kV)
- Overlay and alignment strategy