SEPTEMBER 2022

CONNECTIONS

LATEST NEWS AND UPDATES FROM SEMICONDUCTOR RESEARCH CORPORATION

TECHCON 2022 Keynote: "The Future of Semiconductor Innovation" by Intel's Jack Kavalieros

Image credit: Intel

Jack T. Kavalieros is an Intel Fellow and Vice President directing the novel device and process integration teams in Intel's Components Research Group. He leads a team of device, process integration, and design engineers responsible for conducting exploratory research into advanced transistors, interconnects, memory technologies, novel materials, and architectures. His role requires that he keep a close eye on external research at universities and consortia while staying aligned with the needs of Intel's internal development partners.

Born in Greece, he immigrated to the US in 1980 and completed his PhD in Electrical Engineering at the University of Florida in 1995 with an emphasis in semiconductor device physics and gate oxide reliability under Professor **C.T. Sah.** Upon graduating, he joined Intel's Portland Technology Development group and initially focused on the future of gate dielectric scaling. In 1998 he helped launch the front-end novel device, transistor & process integration team in Components Research which he has been a part of for the last 25 years. Jack played an integral part leading the research and development teams that invented strained silicon channels, High-k dielectrics with dual metal gates, and the 3-D architecture known as Tri-Gate. In 2018 he was appointed as an Intel Fellow and in 2022 promoted to Vice president in Components Research.

He and his team were recognized in the Smithsonian Museum of American History under the exhibition for American Enterprise in the Global Era of R&D, by the 2012 SEMI Award for North America in 2012 for their pioneering work and successful introduction of High-k/Metal Gate in the 45nm CMOS IC production, and by the VLSI Symposium with the "Test of Time Award" for their 2006 paper on the Tri-Gate Transistor Architecture.

As a member of the Institute of Electrical and Electronics Engineers (IEEE), Jack Kavalieros has authored more than 40 publications in IEEE technical journals throughout his career. He also holds over 500 issued patents related to novel transistor & memory devices, materials, architectures, and process breakthroughs.

Register for TECHCON 2022 to attend his keynote address.

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TECHCON2022

SRC Semiconductor Research Corporation

Register for TECHCON 2022

September 18 - 20, 2022
Austin, Texas

Register Here*

**SRC.org website account is required*

SRC Scholar Alum, U-Mich JUMP Student's Dissertation Recognized by SIGARCH/TCCA

Image credit: U-Mich

University of Michigan CSE alum **Akshitha Sriraman** has been awarded an Outstanding Dissertation Award Honorable Mention by the Association for Computing Machinery's Special Interest Group on Computer Architecture (SIGARCH) and Technical Committee on Computer Architecture (TCCA) for her dissertation, "Enabling Hyperscale Web Services." The JUMP ADA tasks she was working on were focused on architecture and technologies for reconfigurable, scalable, energy-efficient accelerators to support the explosive growth in data and compute (Decadal Plan Energy Efficiency Seismic Shift). The SIGARCH recognition of her work is strong validation of the ADA/JUMP vision from the architecture community. Read more >>>

ADA Director Valeria Bertacco has been named the Mary Lou Dorf Collegiate Professor of Computer Science and Engineering

Image credit: LinkedIn

Prof. **Valeria Bertacco** has been named the Mary Lou Dorf Collegiate Professor of Computer Science and Engineering in recognition of her contributions in advancing the field of computer architecture, broadening participation in the field, and in contributing innovations in teaching. Her research focuses on computer design, emphasizing specialized architecture solutions, and design viability with reliability, validation, and hardware-security assurance. Read more >>>

Building Your Elevator Pitch by Emily Rhode of Storied Science, LLC

Image credit: LinkedIn

Last month, **Emily Rhode** of Storied Science LLC shared insights with scholars from the SRC Research Scholars Program about using good science communication to build their career foundations. She touched on the technical aspects of presentations and networking, but most importantly, she empowered scholars with the knowledge that they are the experts on their research; therefore, their confidence and passion should directly correlate. Since many young researchers feel the need to hide their true personalities when meeting someone new or speaking in professional circles, Rhode emphasized the importance of building authentic and meaningful connections with one another. Those connections are desperately needed to make sure that the incredible science being done is understood, believed, and remembered beyond the doors of the lab. To learn more, connect with Storied Science on LinkedIn.

CBRIC Prof. Panda a DARPA Riser

Image credit: Yale

C-BRIC faculty researcher **Priya Panda** was selected as a member of the DARPA Risers program as part of the DARPA Forward series for her work on "Energy-aware and Robust Distributed Learning for Extreme Edge Efficiency." The Risers program recognizes "up-and-coming standouts in their fields," and gives them the opportunity to share their ideas with DARPA representatives. Selected researchers perform work "related to national security and [which] demonstrates the potential to lead to technological surprise." Read more >>>

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Highly-Efficient New Neuromorphic Chip for AI on the Edge

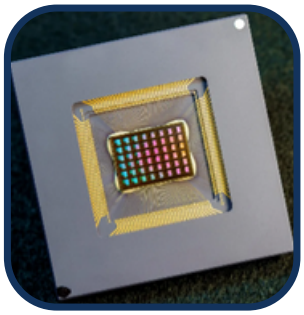
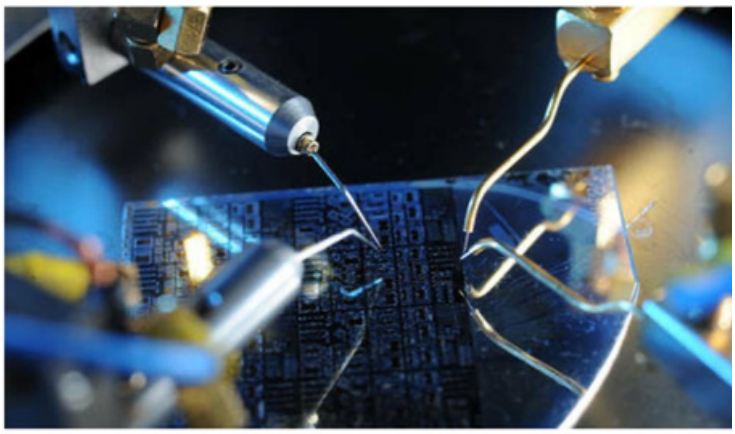


Image credit: SciTech Daily

An international team of researchers led by UC/San Diego has designed and built NeuRRAM, a new chip that runs computations directly in memory and can run a wide variety of AI applications. Notre Dame's Prof. **Siddharth Joshi**, from JUMP ASCENT task #2776.074 on Neuromorphic Design Flow, says "this chip now provides us with a platform to address problems across the stack from devices and circuits to algorithms." Joshi, who started working on the project as a Ph.D. student in the Cauwenberghs Lab at UCSD was added to the ASCENT Center during JUMP's mid-program realignment in 2020. Read more >>>

Midwest Network to Advance Domestic Semiconductors



After years of massive SRC investments in materials, processes, devices, chipmaking, and advanced packaging in Indiana, SRC is thrilled to see Notre Dame and Purdue join 10 other universities in a Midwest Regional Network. The network has a common goal of advancing semiconductor research, innovation, and production. Members can use the SRC Research Catalog to learn about the 14 Notre Dame tasks and 29 Purdue tasks that are actively supported by SRC's members. Read more >>>

SRC Invites Cardea to be Part of Defining how to Integrate Biology with Electronics

Image credit: Cardea

As part of the Semiconductor Research Corporation (SRC) being selected by NIST's Advanced Manufacturing Office to define the future of Microelectronics and Advanced Packaging Technology (MAPT), Cardea Bio has been invited as a commercial semiconductor company to share their experience with integrating biology and electronics. Learn more about Cardea Bio's push to integrate electronic systems and streams of biosignals to create the Internet of Biology with their BPU (Biosignal Processing Unit) platform. Read more >>>

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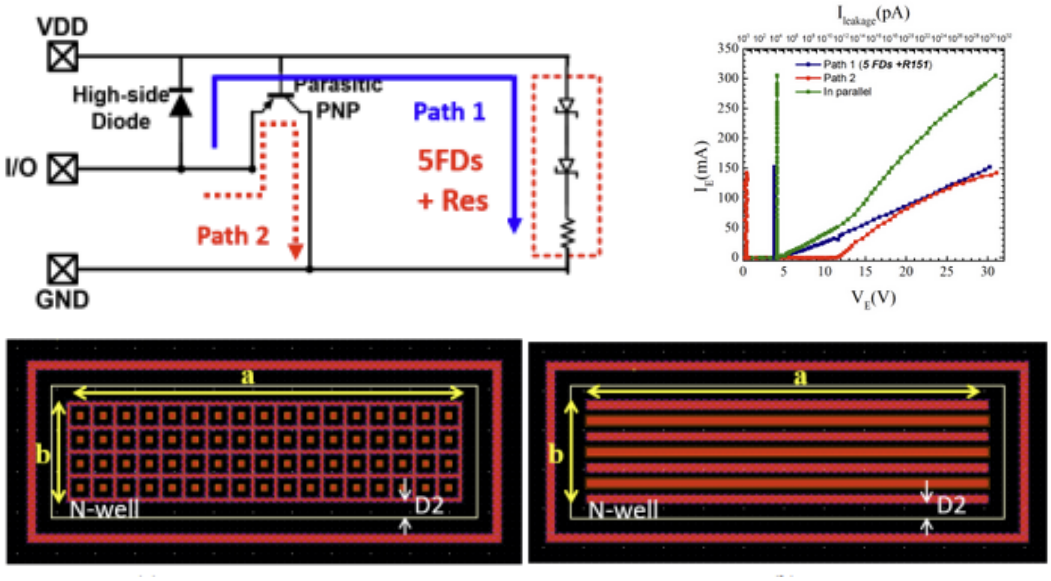
Tech Transfer Series



Electrostatic discharge (ESD) is a major reliability issue in the electronics industry. TxACE researcher, **Zhong Chen**, from University of Arkansas/Fayetteville, has been working with Industry Liaison, **Farzan Barbiz,** from TI, to come up with an innovative way to protect on-chip system level IEC for high-speed interface Integrated circuits (ICs) in an area efficient way. (https://www.src.org/library/research-catalog/2712.015/).

In their research work, also the joint invention disclosure, a novel area-efficient rail-based ESD protection structure was proposed and validated, by utilizing the parasitic bipolar structure (i.e., substrate PNP structure formed between the high-side ESD diode and the chip substrate). The proposed structure saves >10X chip area and passed System-level ESD tests including IEC 61000-4-2 and ISO106051. This collaborative effort has led to patent filing (https://www.src.org/library/patent/p1849/) and will also shape the future of ESD protection research. In terms of market size, ESD Market size is up to 3.2 billion USD; Integrated circuit market size is up to 391.5 billion USD last year.

Top 5 SRC Publications Viewed Across All Programs

Don't miss the papers that received the most views on the SRC website over the last six weeks. Members of the associated programs have early access to the pre-publications.

- Charging Li Ions with Voltage Regulators (Publication P107727)
- Energy Efficient Computing with High-Density STT-Assisted SOT-MRAM (Publication P107773)
- In-Memory Computing: from Devices to Applications - A Cross-Layer Perspective (Publication P107462)
- Regenerative Breaking: Recycling Energy from Duty-Cycled SoC Domains for Energy Minimization (Publication P107253)
- Higher-order Masking of Post-quantum Cryptography (Publication P107150)