

SRC Presenters at GOMACTech 2021 Read more here





Stacked Memory (Synapse) BEOL Peripheral CMOS under Array (CUA)

IEDM 2020 Paper Highlighted in Semiconductor Engineering for Analog Memory, Neuromorphic Applications, and Other Emerging Innovations

Today, billions of connected edge devices produce zettabytes of data that must be transformed into actionable information. This has created an unprecedented demand for data-centric computing with compute-in-memory (CIM) a leading approach to bring compute closer to the data residing in the memory. At IEDM2020, a team of researchers at Notre Dame led by Dr. Sourav Dutta from Prof. Suman Datta's group was first to demonstrate a monolithic 3D integration solution that can greatly accelerate CIM. They demonstrated a fully back-end-of-line (BEOL) compatible ferroelectric field-effect transistor (Fe-FET) with low temperature processing, ultra-scaled channel length, ultra-fast write speed, high endurance cycle and multi-bit programming capability. With such a monolithic 3D architecture, the researchers exhibit a significant advantage in area, energy, and latency compared over conventional 2D architectures. Read more here and here »



SRC Packaging Science Director Gives Keynote at IEEE Heterogeneous Integration Roadmap

John Oakley gave the keynote talk at the IEEE Heterogeneous Integration Roadmap meeting on February 26, 2021. In this talk, he discussed SRC, our Packaging research focus, and key topics of the Decadal Plan with their implications on Packaging research. Packaging research at SRC has been growing and will be instrumental to driving the industry beyond 2D-scaling. See video here.



IEEE Solid-State Circuits Society Establishes Educational Fund in Honor of Prof. James Meindl

The IEEE Solid State Circuits Society has established an educational fund to honor Prof. James Meindl, a long-time SRC-supported faculty and recipient of the 2004 SRC Aristotle Award. This fund will provide long-term support to enable SSCS to nurture, encourage, and celebrate students and early career innovators in the field of solid-state circuits and financially support the awardees to engage high school and undergraduate students through research projects related to integrated circuits technology. Read more »



ADA Wins Best Paper at the International Symposium on Code Generation and Optimization (CGO)

CGO provides a premier venue to bring together researchers and practitioners working at the interface of hardware and software on a wide range of optimization and code generation techniques and issues. The conference spans the spectrum from purely static to fully dynamic approaches, and from pure software-based methods to specific architectural features and support for code generation and optimization. ADA researchers Ajay Brahmakshatriya, Yunming Zhang, Changwan Hong, Julian Shun, Saman Amarasinghe, and their collaborator Shoaib Kamil received the Pest Paper Award for their publication, "Compiler Graph Applications for GPUs with GraphIt." Learn more starting here.



JUMP PI Receives IEEE Computer Society Technical Achievement Award

Professor Vijay Narayanan, Penn State, has received the 2021 Edward J. McCluskey Technical Achievement Award for his contributions to "cross-layer power-aware architectures leveraging post-CMOS technology." This award is given by IEEE for outstanding and innovative contributions to the fields of computer and information science and engineering or computer technology. Read more »



SRC Researcher Joins Podcast "Nanomatters" to Discuss how Nano-tech can Support Next-generation Communication Advancements

Rhonda R. Franklin, Abbott Professor for Innovative Education at the University of Minnesota and NMP program researcher, shares her opinion with Lisa Friedersdorf, the director of the National Nanotechnology Coordination Office, on her podcast, Nanomatters. In NMP, Prof. Franklin works on characterizing nanowire array vias from 30 to 325 GHz for both DC and AC applications. See video here



SRC Researcher Hosting IEEE Solid-State Circuits Society Directions Workshop

SRC researcher, Prof. Boris Murmann (Stanford) is hosting an IEEE Solid-State Circuits Society Directions Workshop titled "Democratizing IC Design" on April 7th. The event is open to all and will look at the new movement toward an open-source ecosystem for integrated circuit design. Last year, Google, SkyWater, and efabless have partnered to launch a shuttle program based on SkyWater's SKY130 open-source process (130 nm CMOS). This technology is offered to the open community along with a complete design flow to enable designers to implement their ideas. This workshop will provide an overview of this program and highlight upcoming opportunities to benefit from it. Finally, it will showcase specific design work delivered by the community members and articulate a call to action for volunteers to design, teach and mentor. Read more »

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