2012-2016 SRC-GRC Strategic Plan

Draft II 6/2011

2012 – 2016 SRC-GRC Strategic Plan

Table of Contents

I. EXECUTIVE SUMMARY

I. EXECUTIVE SUMMARY

OVERVIEW

During the spring of each year, SRC business planning includes development of an SRC-GRC Strategic Plan, covering the ensuing five years (2012-2016). The planning process continues in the fall of each year with the development of an Operations Plan for the next calendar year. The GRC Strategic Plan is developed by various Technical Advisory Committees/Boards in conjunction with SRC Directors and managers of corresponding functional areas. The plan is reviewed by the appropriate representatives of member companies, the OCE and finally, the SRC Board. The plan becomes a plan of record after the SRC Board approves it in 2Q/3Q of the year.

STRATEGIC PLANNING PROCESS

The development of these plans utilizes outputs from various forums and analyses. SRC has periodically continued to conduct a Research Gap analysis to assess the amount of research investment necessary to address the ITRS challenges as compared with the actual investment occurring worldwide. This analysis highlights the criticality of research needs and respective shortfalls in funding, thereby providing a backdrop for the Strategic Plan. Additionally, the SRC community conducts a biennial GRC ETAB Summer Study and an SRC Annual Board Retreat to derive long-term strategic technical and business directions. Based on the outputs of these two forums, the ETAB develops an annual list of top-down, strategic technical priorities. The SACCs and T-TABs develop the Strategic Plans of the various science areas using the inputs from the forum and analyses described above. All of the information from these sources is then incorporated into the strategic technical priorities that are decided at the end of the annual ETAB strategic planning meeting. These priorities are the starting point for the plans shown in **Section III**. The ETAB strategic planning strategic priorities resulting from the 2010 ETAB Strategic Planning meeting are reproduced here and are the same for 2011:

- Scaling to Ultimate CMOS: Processes, Materials, Devices, Packages, and Systems
- Analog/Mixed Signal: Processes, Materials, Devices, Packages, and Systems
- Memories: Materials, Devices, Circuits, and Subsystems
- Low Power Architecting: Devices, Circuits, and Systems
- Power, Thermal, and Energy Management
- Design Productivity for Circuits and Systems
- Application-specific Integration of Diverse Technologies
- 3D IC Architecting: Technology, Design, Test, and CAD
- Multicore Homogeneous/Heterogeneous Systems
- Reliable, Resilient and Robust Technology, Circuits, and Systems
- ESH Stewardship for Materials, Processes and Energy

The specific strategic directions for each science area and thrust are outlined here. Each of these thrust level areas of emphasis are determined by the SACCs and T-TABs after the ETAB strategic priorities are set.

COMPUTER-AIDED DESIGN AND TEST SCIENCES (CADTS)

CADTS will continue to have an overarching emphasis on power and energy, design for manufacturability, productivity, reliability and resilient robust systems. For digital technologies, the emphasis is on variability, low power, multiple domains (voltage, clock, frequency, etc.) while analog topics include low voltage, synthesis, automated layout, test, and verification. System-level design issues include verification and test, software, multicore, 3D, reliability, memory subsystems, and multicore homogeneous/heterogeneous systems. Test issues include statistical test methods, more on chip self-test, mixed-signal, and 3D. Verification at all levels continues in importance.

INTEGRATED CIRCUIT AND SYSTEMS SCIENCES (ICSS)

The ICSS area continues to maintain only two thrusts: Circuit Design and Integrated System Design. Emphasis on working across science areas continues as the division between design and manufacturing becomes less defined. In the Circuit Design thrust, the emphasis will be on developing design innovations to enhance the robustness, performance, power-efficiency and application space of logic, memory, mixed-signal, RF and mm-wave circuits. In the Integrated System Design thrust, the emphasis will be on developing novel techniques and design methodologies for the integration robust, high-performance, power-efficient systems comprised of silicon, software and an infrastructure to support their thermal/power management and communications.

DEVICE SCIENCES (DS)

For logics, the overall priority is to track and push ITRS-driven CMOS scaling towards limits. Advanced materials, structures. and processes are studied for this purpose. Some important areas to be enhanced are strain to improve mobility, high-K gate dielectrics and metal gate, source/drain junction and contact, and alternate channel material III-V. Analog technologies, active and passive devices, are becoming increasingly important and common for mixed-signal applications as well as functional diversification. Research in this thrust has been growing. In memory, the priority is to develop novel non-volatile memories of non-charge-based cells, such as ReRAM, FeRAM, and MRAM, to replace the floating-gate and charge-trapping types, and selection devices for 2-terminal cross-point arrays. Apart from technology development, DS maintains a balance in modeling effort which includes process and device simulation, and compact modeling of the aforementioned technologies.

NANOMANUFACTURING SCIENCES (NMS)

The mission of NMS is to deliver value by developing and providing early access to evolutionary, breakthrough, and high impact material, process, and metrology technologies for scaled CMOS, targeting a half pitch of ≤10 nm, and analog/mixed signal technologies, including: 1) low variability, centered, and cost effective nanofabrication options that enable extensible scaling [≤16 nm]; 2) functional diversification of charge-based technologies, which may be in addition to scaling options that increase performance and functionality; and 3) high-performance and sustainable options that enable 3-D applications. An additional goal is to develop and provide our members with well-educated students, who are prepared for innovation driven careers in nanofabrication technology.

INTERCONNECT AND PACKAGING SCIENCES (IPS)

The current strategy for IPS is to continue to focus the BEP and Packaging Thrust portfolios on the 16 nm CMOS technology node and beyond, while at the same time addressing the cross-Thrust issues with our well-defined 'interface' research. BEP emphasis continues to be aimed at ensuring the viability and reliability of scaled Cu / low-k interconnects. There is an increased emphasis on predictive modeling and nano-metrology capability development. Packaging research continues to drive thermal management alternatives, wafer level and thinned-die packaging solutions, reduced chip-package spacing, and optimized power delivery, as well as now an increased emphasis on developing viable optical global interconnect options. There is also a need to explore the interactions between biological systems and electronic packages, as well as integration options for passive components and sensors to address the functional diversity needs of the industry at the system level. The Interface research portfolio continues to increase the focus on 3D integration, while also driving solutions for critical die-package thermo-mechanical reliability issues.

CROSS-DISCIPLINARY SEMICONDUCTOR RESEARCH (CSR)

One of SRC's missions is to provide a strategic vision for the possible scenarios of both technologies and their applications in the longer term (e.g. 15 years from now). As a part of this effort, SRC-GRC launches exploratory research targeting long-term applications through CSR. Specific areas to target this year are to support development of a Research Center in Abu Dhabi, to support efforts to develop new initiative in bioelectronics and to conduct a forum in Abu Dhabi on advanced photovoltaics. Other fundamental studies on on the scaling limits of memory select device, biocomputing and others will be pursued.

VALUE INFRASTRUCTURE MANAGEMENT (VIM)

The mission of SRC's Value Infrastructure Management (VIM) group is to provide the people, processes and infrastructure necessary to proactively support and promote all aspects of SRC's value proposition. In essence, the primary strategic role of the VIM group is to position SRC's core value-based business services to adapt and evolve in support of SRC's strategic direction in a timely, efficient and effective manner.

II. SRC STRATEGIC PLANNING

II. SRC- GRC STRATEGIC OVERVIEW

SRC business planning process, depicted in **Figure 1**, results in two documents that provide the basis of long-term directions and annual operations of SRC. Each year during the first two quarters, the SRC community develops a Strategic Plan covering the time horizon of the following five years. In the fall of each year SRC develops an Operations Plan for the next year. These plans are based on a number of inputs resulting from a variety of formal interactions among the SRC member representatives on advisory boards and the Board of Directors. In order to develop a foundation for the Strategic Plan, the OCE team conducts an annual assessment of long-term environmental trends in our industry and resulting challenges. Based on this assessment, the team also develops strategic directions. This strategic vision is reviewed with the Board to receive their inputs and ratification.

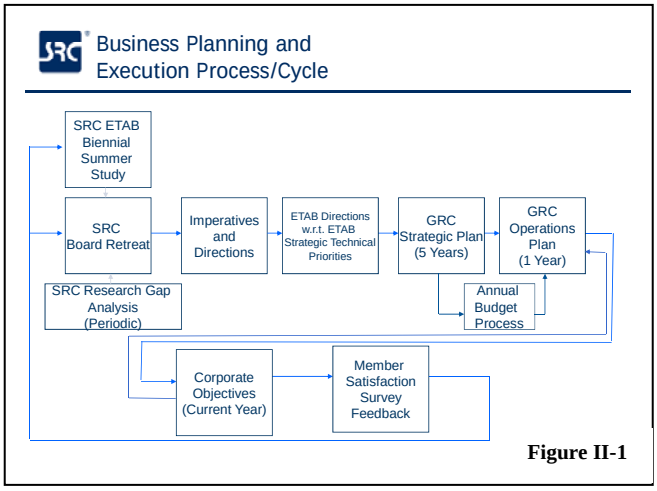


Figure II-1

As we did last year, the SRC strategic planning and the GRC strategic planning will be separated into two separate documents. The GRC strategic plan is the subject of this document and deals with the SRC-GRC strategy. The SRC Strategic Directions document will be done separately and will be developed directly with the SRC Board of Directors.

SRC-GRC STRATEGIES

The SRC Science Area Structure has proven to be responsive to the research needs of member companies and aligns well with the Focus Center themes. We expect that this structure will be sustained during the 2012-2016 timeframe of this Strategic Plan. However, there is a continuing need for Cross-Science-Area thrusts (Cross-thrusts) of which there are nine.

The nine managed Cross-thrusts that are currently operative are (1) 3D (Candelaria) (2) Mixed-Signal Technologies (Yeh), (3) Metrology and Characterization (Herr), (4) Modeling and Simulation (Candelaria), (5) Reliability (Candelaria), (6) Memories (Ng), (7) Multicore (Joyner), (8) Interconnect (Candelaria), and (9) Design for Manufacturability (Joyner). SRC also participates in an annual reliability symposium with SEMATECH and other agencies. SRC will continue its membership in the Nano Computational Network sponsored by NSF at Purdue that is developing computational tools for the atomistic level modeling of semiconductor devices.

A concerted effort to coordinate the SRC-GRC research with the research supported within the Focus Center Research Program (FCRP) is managed through the Science Area Directors and Program Managers. Each Director has responsibilities for a Focus Center that is most closely aligned to his respective area (see **Table 1**). The role of SRC-GRC Research Management for the FCRP includes review and coordination of FCRP and GRC research

portfolios, organization of the industry feedback to FCRP Center Directors following the Center Annual Reviews, and assisting in the generation of reports for DARPA and FCRP sponsors.

Focus Center	MSD	IFC	FENA	GSRC	C2S2	MuSyC
GRC- Manager	Kwok Ng	Jon Candelaria	Dan Herr	Bill Joyner	Dale Edwards	David Yeh

Table II-1

In addition to the coordination responsibilities as detailed above, an extra step in the solicitation process was instituted at the GRC proposal review stage for researchers engaged in a Focus Center. This step requires the researchers to describe the differences and potential overlaps of their FCRP efforts with the proposed GRC research project to enable informed funding decisions in order to benefit both programs.

There is also an active effort to keep the NRI projects and results coordinated with the GRC research portfolio. Particular attention is paid to the results of CSR projects that would be relevant to the NRI program.

SRC-GRC PARTNERSHIPS

SIA

SRC expects to continue to support SIA initiatives to call to the attention of Congress and the Administration the vital importance of the semiconductor industry to the economic health of the United States, and, in particular, to the importance of federal support for basic research in Physical Science and Engineering.

NSF

SRC expects to continue its productive partnership with NSF over the planning period.
The NSF and SRC-GRC collaborate under an umbrella MOU that provides for SRC (and hence industry) involvement in the planning, selection, and review of NSF-sponsored programs. The MOU was renewed in 2010 to explicitly include integration of NSF projects that are of interest to our members into the SRC research dissemination processes for faculty who choose to participate.

This is the second year of a 3-year joint program between NSF and SRC that supports multicore research. Similar joint program is under consideration in the area of optoelectronics. In addition, SRC is engaged in the NSF process—and may elect to partner on a proposal—for establishing new Engineering Research Centers focusing on research directions that are of interest to the semiconductor industry.

STATE GOVERNMENTS

SRC-GRC and the State of New York are jointly supporting the Center for Advanced Interconnect Science and Technology (CAIST) that is headquartered at the State University of

New York at Albany and involves a substantial number of New York and university participants from other regions. We have joint programs with Texas (TxACE and CEMPI), with Georgia (IPC), and Arizona (ESH). These programs provide substantial leverage for member funds and serve as a model for other SRC/State research initiatives.

NIST

SRC-GRC has also worked closely with NIST and we will seek ways to expand our domain of cooperation. The area of metrology and characterization will assume ever-increasing importance as the industry moves into the far-sub-nanometer regime. We have begun interaction and cooperation in the areas of device reliability and bioelectronics.

III. SRC GRC RESEARCH PROGRAM

OVERVIEW

Science Area: Computer-Aided Design and Test Sciences
Director: William H. Joyner, Jr.

MISSION

The Computer-Aided Design and Test science area has as its mission:

Promote excellent and relevant university research to strengthen member leadership in computer-aided design and test:

- through tools and techniques that:
    - reduce cost and time-to-market through productivity improvement and correctness assurance
    - enable high level/high value design
    - take full advantage of technology advances through linkages to manufacturing
    - anticipate future CMOS and post-CMOS CAD challenges
- through highly qualified graduate students who can fill key positions in member companies
- through strategic partnerships that leverage other funding sources

Member companies who employ SRC-supported students on summer internships, as postdocs, or as permanent employees are able to better extract the value of research in design tools and test techniques. Students can apply the results of their research, often immediately, in the industrial research and development environments of SRC members, giving them an advantage over those without the opportunity to guide and take early advantage of this work.

Design and test tools also can and must address cost pressures:

- by reducing time-to-market through the speedup of the logic and physical design process and the migration of this process to higher levels,
- by reducing product field failures by pre-manufacturing verification and efficient and effective manufacturing test, and
- by coupling with the manufacturing process to control cost and improve yield as feature sizes shrink.

CADTS aims to provide:

- research for highly productive digital/analog/RF design flows
- key research directions for design-based performance gains
- tools critical in reducing cost by reducing/eliminating re-spins
- smoother, efficient interfaces between design and manufacturing
- tools to benefit application-driven design

ENVIRONMENT AND TRENDS

Highlights of the changing environment facing computer-aided design and test include:

The CADTS Ecosystem

- CAD vendors depend on industry as a whole, and need multiple sources for research
- Design and CAD must extract the highest performance from each technology node
    - CAD needed on "cutting edge" to leverage new technologies (3D, etc)
    - CAD needed to squeeze more out of current technologies
- Design productivity needs to keep pace with design complexity
- Pre- and post-silicon validation an increasing focus due to time-to-market, lower average selling price, complexity factors
- 3D CAD challenges increase with finer-grained 3D integration

The digital design environment

- Several billion transistors on a chip with power constraints
- Multi-core, 3D, systems-on-chip, mixed analog/digital
- Lower supply voltages → decreasing noise margins
- Opposite pulls:
    - Higher-level design to improve productivity
    - Lower-level awareness to assure manufacturability
- DFM/DFV/DFT/DFR critical as variability increases – provide support for multiple operating modes and power management techniques.
- Emerging devices and new technologies –
  Longer lifetimes for older technologies

The analog/mixed-signal/RF design environment

- Analog presents additional challenges: fully integrated on chip, within package, 3D, or stand-alone
- Automation needed for synthesis, optimization, physical design, verification – lags digital
- Slower scaling than digital
    - Harder to get to work with advanced processes
    - May need special processes and devices
    - Can drive 3D IC design tool development
- Applications in safety, health and energy require highly robust and fail-safe designs
- Test becomes more difficult with increasing analog content
- Concerns remain about noise from digital circuits in SoCs with increased analog content

The system design environment

- Opportunity to exploit high level design and verification for increased productivity
- Homogeneous, heterogeneous multi-core designs demand additional CAD efforts
- Software a major component of system design and affects CAD focus
- System testing/verification an increasing challenge
- Power/thermal issues at multiple levels
- Resilience/resistance to failure at system level
- Parallel CAD algorithm development essential for productivity
- Increased focus on cyber-physical systems, cyber security

CAD and Test Challenges

- Increased focus on reliability and resistance to failure with reduced ASP, higher volume, lower margins, test challenges
- Design productivity still key
- Time-to-market critical
- "Correct-the-first-time" important to reduce re-spins
- Need to reduce size/cost of design teams
- Optimization and system-level design are key
- Post-silicon bring-up, validation, test
- Mixed-signal/heterogeneous systems make test and verification more difficult
- Technology scaling and the resulting design rule explosion
- Observability obscured by complexity

PRIORITIES

The SRC Executive Technical Advisory Board highlighted these design-related priorities in 2011:

- Scaling to Ultimate CMOS:
  Processes, Materials, Devices, Packages, and Systems
- Analog/Mixed Signal:
  Processes, Materials, Devices, Packages, and Systems
- Memories: Materials, Devices, Circuits, and Subsystems
- Low Power Architecting: Devices, Circuits, and Systems
- Power, Thermal, and Energy Management
- Design Productivity for Circuits and Systems
- Application-specific Integration of Diverse Technologies
- 3D IC Architecting: Technology, Design, Test, and CAD
- Multicore Homogeneous/Heterogeneous Systems
- Reliable, Resilient and Robust Technology, Circuits, and Systems

Design priorities emphasized in the 2010 International Technology Roadmap for Semiconductors include:

- Design productivity
- Power consumption
- Manufacturability
- Reliability
- Interference

Other 2010 ITRS emphases included SiP planning and implementation flows, heterogeneous component integration, A/MS/RF, design for reliability, 3D/TSV

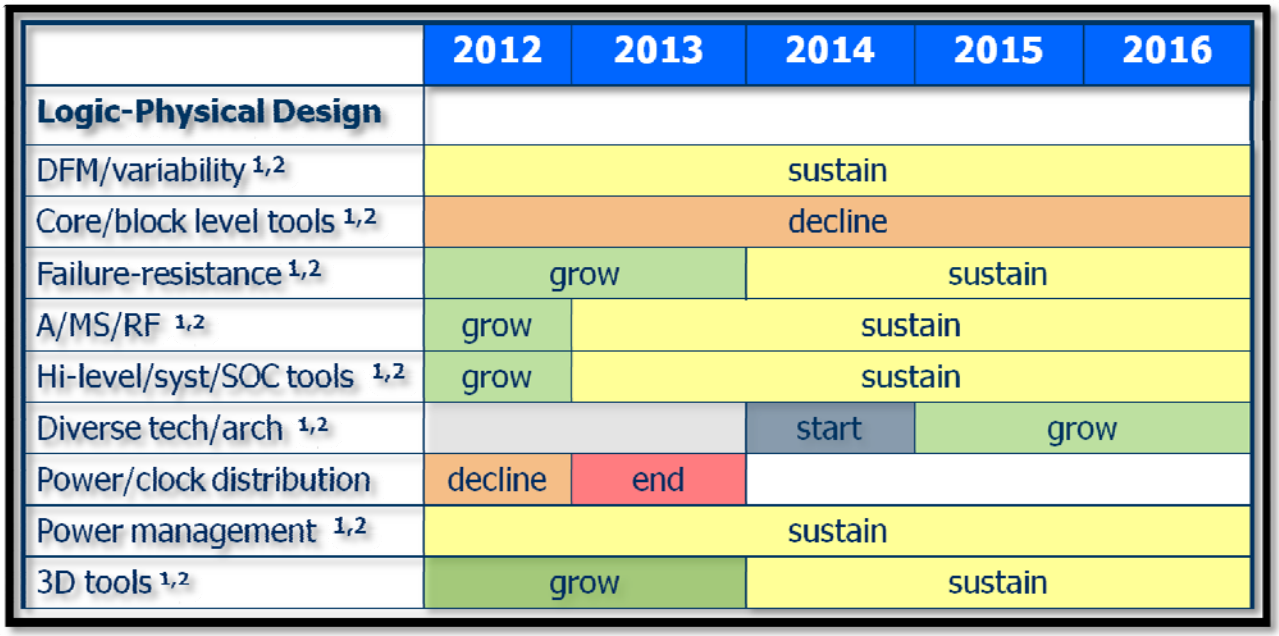
A 2010 Design Automation Conference workshop on a design automation roadmap stressed:

- End product roadmaps
- System level
- Design space exploration
- Software synthesis and verification

- Post silicon
- EDA scaling
- Power management
- 3D
- Variability
- Analog / mixed-signal
- Interoperability

STRATEGIC ACTION PLAN

- Classical challenges expected to remain difficult: power and energy, design for manufacturability, productivity, reliability, hardware/software co-design, . . .
- Continue exploration of leading/future technologies for CAD
  - Digital: variability, low power, multiple domains (voltage, clock, frequency, etc.)
  - AMS: low voltage, synthesis, verification
  - System-level design: verification and test, software, multicore, 3D, reliability
- Thrusts and emphases:
  - Design issues (low power/voltage, variability, resilience, high-level, productivity)
  - Test issues (statistical test methods, more on-chip self-test, mixed-signal)
  - Verification issues (mixed-signal, coverage, post silicon validation)
- Link with other science areas as traditional boundaries blur
- Continue leveraging initiatives and cooperation with NSF, DARPA, States, FCRP, GRC SAs, . . .



	2012	2013	2014	2015	2016
Logic-Physical Design					
DFM/variability [1,2]	sustain				
Core/block level tools [1,2]	decline				
Failure-resistance [1,2]	grow		sustain		
A/MS/RF [1,2]	grow	sustain			
Hi-level/syst/SOC tools [1,2]	grow	sustain			
Diverse tech/arch [1,2]			start	grow	
Power/clock distribution	decline	end			
Power management [1,2]	sustain				
3D tools [1,2]	grow		sustain		

	2012	2013	2014	2015	2016
Verification					
Core technologies [1,2]	sustain	decline			
RTL/Coverage [1,2]	sustain		decline		end
System-level [1,2]	grow		sustain		
Software/microcode [1,2]	start	grow	sustain		
A/MS/RF [1,2]	grow	sustain			
Test					
System/SoC [1,2]	grow	sustain			
Delay-based, stuck fault [1,2]	decline	end			
Test for mfg and yield [1,2]	sustain				
Post-silicon validation [1,2]	grow	sustain			
A/MS/RF [1,2]	grow	sustain			
Test for 3D, adv tech [1,2]	start	grow	sustain		

(1)=ETAB priority (2)=ITRS

OVERVIEW

Science Area: Integrated Circuits and Systems Sciences
Director: David C. Yeh

MISSION

To conduct research in advanced integrated circuits and systems design that will

- Exploit advances in IC technology while overcoming associated barriers and challenging conventional notions of the circuits and systems design space
- Develop a circuits and systems research portfolio that will provide exceptional value to our Members – with a focus on design-based performance gains
- Facilitate the training of highly-skilled graduates to help fill design engineering needs of Members

In the Circuit Design thrust, the emphasis will be on developing design innovations to enhance the robustness, performance, power-efficiency and application space of logic, memory, mixed-signal, RF and mm-wave circuits. In the Integrated System Design thrust, the emphasis will be on developing novel techniques and design methodologies for the integration robust, high-performance, power-efficient systems comprised of silicon, software and an infrastructure to support their thermal/power management and communications.

ENVIRONMENT AND TRENDS

- Technology-driven constraints and increased transistor count impact all circuits and systems
    - Process variability, leakage, low-Vdd, new devices (eg. FinFETs)
    - Increased probability of reliability-induced failure: SEU/aging
    - Resilient circuits and architectures will be essential
    - Design complexity increases faster than transistor count
    - POWER will always be an issue – even beyond CMOS
- Design research on the CMOS scaling path continues
    - Adaptive systems: reconfigurable, self-adaptation, self-test
- High fab cost and restricted access constrains research outcome
    - Need is to focus on areas where universities add value
    - Critical to address above trends
- Emphasis on multi-core, 3D, SoC/SiP: integration and reliability
    - Software concurrency, tools, debug, verification, programming model
- Integration of multiple functional blocks + software
    - Long and difficult new product development and launch cycles, including software development and debug
    - Challenging to optimize digital and analog circuits…
- Diverse applications drive architecture/ IP/circuits/ software
    - Design constraints cover power, performance, cost, safety

- The spectrum of research is broad and interdisciplinary
    - Digital, analog, mixed-signal, RF, memory & I/O
    - Novel structures: multi-gate, 3D integration, devices
    - Reliability impact: cause-effect and solutions
    - Covers frequencies of interest from Hz to hundreds of GHz
    - Sensors, actuators, cyber-physical systems

Of special note this year is the emphasis on safety. As application spaces for integrated electronics expand beyond the PC and mobile internet platforms to others include automotive and medical, reliability requirements may become much more stringent as a result of the end-product requirements. As such, research that extends reliable/fault-free operation to harsh environments such as extreme temperatures and electrical interference is an area of interest by the members. In addition to the harsh environment, long product lifecycles, operating time, and long product lifetime further add design challenges. Some of the techniques being considered include robustification, sense and adapt.

Challenges highlighted by the ICSS SACC include

- Economy is better but funding challenges remain
- Broadening research needs
    - Multiple application and integration domains
    - Digital – Memory – Mixed/Signal – RF – Analog
    - Technology nodes of interest
        - AMS/RF → 65 nm – 28 nm
        - Digital → 15 nm and beyond
    - Diverse research lead times
- PIs lag Members in access to process technology and simulation models
- Maintaining interest and relevance

PRIORITIES

The GRC Executive Technical Advisor Board highlighted these design-related priorities in 2011:

- Scaling to Ultimate CMOS: Processes, Materials, Devices, Packages, and Systems
- Analog/Mixed Signal: Processes, Materials, Devices, Packages, and Systems
- Memories: Materials, Devices, Circuits, and Subsystems
- Low Power Architecting: Devices, Circuits, and Systems
- Power, Thermal, and Energy Management
- Design Productivity for Circuits and Systems
- Application-specific Integration of Diverse Technologies
- 3D IC Architecting: Technology, Design, Test, and CAD
- Multicore Homogeneous/Heterogeneous Systems
- Reliable, Resilient and Robust Technology, Circuits, and Systems

The 2010 International Technology Roadmap for Semiconductors includes these priorities:

- Silicon Complexity
    - Non-ideal scaling of device parasitics and supply/threshold voltages
    - Coupled high-frequency devices and interconnects

    - Manufacturing variability
    - Complexity of manufacturing handoff
    - Scaling of global interconnect performance relative to device performance
    - Decreased reliability
- System Complexity
    - Reuse
    - Verification and Test
    - Cost-driven Design Optimization
    - Embedded Software design
    - Reliable Implementation Platforms
    - Design Process Management
- Cross-cutting challenges
    - Design Productivity; Power Management; Design for Manufacturability; Interference; Reliability
- Expansion of analog in revision of RF/Wireless Chapter
    - Revision of RF/Wireless chapter
    - mm-wave; Power management; Short-distance transceivers/transducers; High speed links (40 Gbps) ; Automotive controls; ….

STRATEGIC ACTION PLAN

- Addressing a demanding research agenda
    - Improve design-to-fab infrastructure for PIs
        - MOSIS special pricing/GRC fab $ match program
        - Investigate other opportunities for fabrication and simulation
        - Hold another design challenge?
    - Work across science areas where appropriate
        - CADTS – system tools; DS – predictive CMs; IPS – packaging;
    - Partnering with other entities for leveraging
        - 2012 joint solicitation with NSF on failure-resistant system
        - Support the renewal of the State of Texas funding for TxACE
        - Monitor long-range research – FCRP, NRI, etc., engage when ready
- Continue to increase value to member companies
    - ICSS e-Workshops, including monthly from TxACE
    - e-Kickoffs for new programs where appropriate
    - Help members identify/hire excellent students
        - Invite final year students to reviews, present posters/previews
    - Remote access to reviews; RCP fund travel assistance
    - File IP where there is value
    - ICSS newsletter
    - Stronger emphasis on new member recruiting

Circuits	2012	2013	2014	2015	2016
Memory	sustain				
Functional Diversification – (mmWave/bio/….)	sustain	grow			
Analog/MS/RF Design	sustain				
Homogeneous/ heterogeneous multicore[1]	sustain	decline			
Coping with variability and reliability	sustain	grow			
Design solutions for thermal/power[1]	sustain				

(1) These research topics will be pursued in the Systems area.

Systems	2012	2013	2014	2015	2016
Memory	sustain				
Functional Diversification - Applications	sustain				
Homogeneous/ heterogeneous multicore	sustain				
Coping with variability and reliability	sustain	grow			
Design solutions for thermal/power	sustain				
Embedded systems and software	sustain				

OVERVIEW

Science Area: Nanomanufacturing Sciences (NMS)
Director: Daniel Herr

MISSION

The mission of NMS is to deliver value by developing and providing early access to evolutionary, breakthrough, and high impact material, process, and metrology technologies for scaled CMOS, targeting a half pitch of ≤10 nm, and analog/mixed signal technologies, including: 1) low variability, centered, and cost effective nanofabrication options that enable extensible scaling [≤16 nm]; 2) functional diversification of charge-based technologies, which may be in addition to scaling options that increase performance and functionality; and 3) high-performance and sustainable options that enable 3-D applications. An additional goal is to develop and provide our members with well-educated students, who are prepared for innovation driven careers in nanofabrication technology.

ENVIRONMENT AND TRENDS

The semiconductor industry's growth rate relies on continuously enhanced functional density to provide increasing value. However, it is becoming increasingly **DIFFICULT** to manage variability, cost, reliability, yield, sustainability, and factory operations with conventional scaled subtractive/damascene processing alone. This trend implies an increasing number of potential insertion opportunities for breakthrough innovations in materials and nanofabrication technologies that address these emerging digital and analog/mixed signal challenges.

PRIORITIES

The following high level strategic research priorities are aligned with the NMS mission and driven by the 2010 ETAB identified critical research needs:

- **Centered, low variability fabrication technologies:** Demonstrate that the percent of manufacturing variability need not increase with functional density, i.e. with respect to dimension, overlay, placement, composition, architecture, etc. This includes the development of predictive models that provide insight into key nanomanufacturing tool-material-process trade-offs and their synergistic impact on reducing material, process, structural and property variability;

- **New cost curves for scalable nanoelectronics fabrication:** Develop novel materials, modeling, process and equipment options that:
  - Enable extensible nanoelectronics fabrication, defect detection, and yield management into the sub-10 nm domain;
  - Strengthen the predictive capabilities of the computational lithography infrastructure;
  - Leverage the existing fabrication infrastructure;

- **Sustainable, high performance fabrication:** Extend sustainable, benign, high performance nanomanufacturing technologies into the sub-10 nm domain.

- **Functional diversification:** Design, identify, and enable the integration of customized materials with electronically useful functionality for high value application opportunities, which includes an emerging emphasis on predictive materials by design and quantitative material structure-property correlations;

- This set of challenges provides a framework for assessing the potential of proposed and continuing research to achieve critical science area objectives.

STRATEGIC ACTION PLAN

Nanomanufacturing Sciences Research [NMS], Overall: NMS' 2012-2016 research strategy is designed to:

- Identify and address strategic member/ETAB and ITRS identified needs;
- Maintain a strong and leveraged relationship with SEMATECH/ISMI, with respect to relevant strategic initiatives, such as the Center for Environmentally Benign Semiconductor Manufacturing [CEBSM].
- Develop, engage, leverage and influence targeted government and regional initiatives; For example, in the ESH thrust area, consider opportunities that leverage strategic and relevant nanoengineered materials related aspects of the EPA's nanomaterials research centers. Also, encourage well positioned proposals that offer leveraged support.
- Engage tool suppliers early in the research cycle;
- Enhance GRC/NMS-FCRP-NRI synergy, coordination, and networking;
- Evolve thrusts to anticipate and reflect emerging non-traditional drivers.

- [Note: In the following Thrust Research priority tables, the super scripts '[1]' and '[2]' correspond to ETAB priorities and ITRS challenges, respectively.]

Patterning Research [PAT]: This thrust creates and enables high-impact potential patterning options, centered at 16 nm and beyond, which address member-identified and projected ITRS difficult patterning challenges.

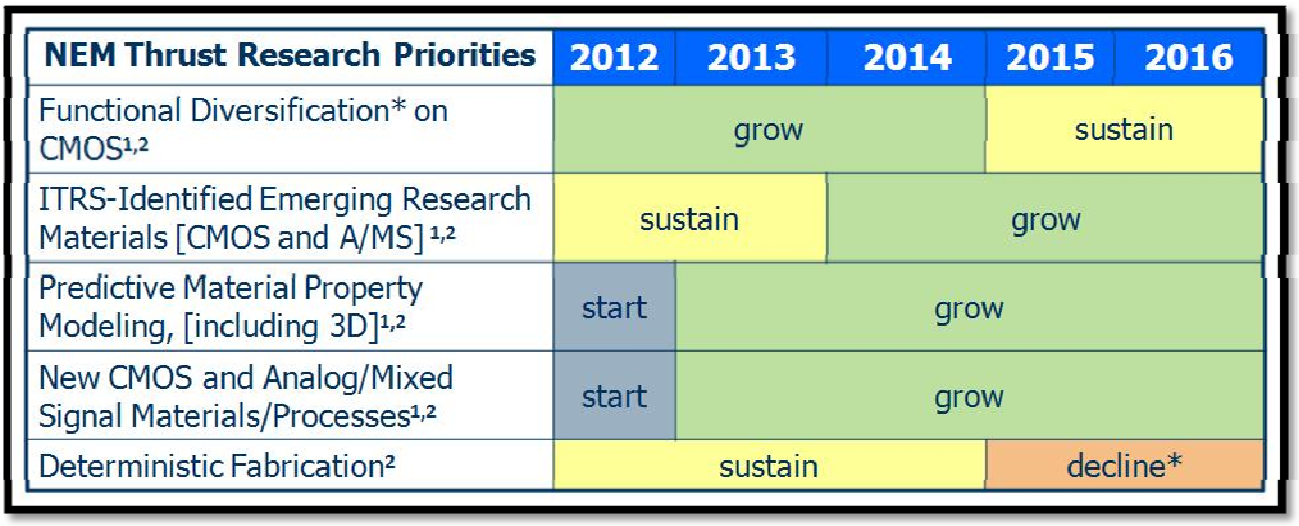
- 2012-2013: Assess potential of directed self-assembly for insertion in 2018-2019.
- 2012-2016:
  - Address the patterning variability challenge, such as through an increased emphasis on predictive computational lithography and process aware compact models;
  - Develop critical knowledge-base of post-NGL patterning options, e.g. maskless patterning;
  - Identify and address strategic member-identified patterning needs.

- **Nanoengineered Materials [NEM] (Currently Positioned Under the Patterning Thrust):** This thrust seeds and explores emerging research material and process options that address strategic member scaling and analog/mixed signal needs.

- 2012-2016: Launch targeted seed projects that explore prioritized needs and uncover emerging opportunities;

- 2012-2016: Increase the emphasis on developing predictive material and synthesis modeling to enable a functional and structural materials-by-design capability.

- 2012-2014: Ensure rapid communication of breakthrough results to thrusts and science areas.



NEM Thrust Research Priorities	2012	2013	2014	2015	2016
Functional Diversification* on CMOS[1,2]	grow			sustain	
ITRS-Identified Emerging Research Materials [CMOS and A/MS] [1,2]	sustain		grow		
Predictive Material Property Modeling, [including 3D][1,2]	start	grow			
New CMOS and Analog/Mixed Signal Materials/Processes[1,2]	start	grow			
Deterministic Fabrication[2]	sustain			decline*	

- [Note: * Will evolve with strategic SACC-ETAB alignment and ITRS consensus.]

  Metrology and Nano-Characterization Research [MET] (Currently Positioned Under the Patterning Thrust): This cross-thrust addresses strategic member company and ITRS-identified nano-characterization and metrology knowledge gaps. It explores emerging and enabling ≤ 10 nm measurement options.

  - 2012-2013: Secure and leverage resources, such as with SEMATECH, to address GRC/FCRP/NRI nano-characterization gaps.

  - 2012-2016:
    - Ensure that the metrology portfolio continues to anticipate emerging nanomaterial and device measurement needs.
    - Increase and maintain visibility of metrology results across thrusts and science areas.
    - Update assessment of GRC/FCRP/NRI nano-characterization gaps.
    - Leverage and engage strategic relevant metrology initiatives.

- **Environment, Safety, and Health Research [ESH]:** This thrust explores sustainable, high-performance semiconductor materials and processes for future technologies, which reduce consumables, energy, and water use and enable new material screening options.

  - 2012-2016:
    - Maintain current SRC processes for selecting, assessing, and managing strategic and relevant ESH related research.

- Ensure the re-competed research portfolio aligns with the joint SRC-SEMATECH/ ISMI research needs document and addresses strategic high priority ESH research needs, especially with respect to understanding the ESH impact of new and nanomaterials and sustainable processes;
- Sustain and grow the Center's culture;
- Continue to secure strategic SEMATECH/ISMI support
- Secure new and additional leveraged resources for sustaining future relevant ESH research.
- Develop multi-regional initiatives.
- Increase and maintain visibility of ESH research in other GRC thrusts.

ESH Thrust Research Priorities [Near term growth through leverage]	2012	2013	2014	2015	2016
ESH Impact of New and Nanomaterials					
▪New Materials and Associated Processes[2] - Includes packaging materials and processes	grow	sustain			
▪ESH for Nanotechnology[2]	grow	sustain			
▪New Technologies for Detection, Hazard Assessment, and Toxicity Screening[1,2] - Includes dose definition, hierarchical assessment, and data mining	grow	sustain			
ESH/Process Improvement					
▪Reduction in "Net" Water Use[1,2]	sustain				
▪Energy: Utilization, Management, and Sources[1,2]	start	grow			
▪Chemical Utilization and Waste Reduction[2]	sustain				
▪Hazardous Chemicals Use Reduction[2] -Includes sustainable chemical substitution	sustain				
▪Reduction of Hazardous Emissions, e.g. PFCs[2]	grow [phase II]			sustain	
▪Design for ESH/Life-Cycle Analysis[2]	start		grow		

Factory Systems Research [FAC]: This research thrust is formally sunsetted.

- 2012-2016:
  - **Transitioning to a sub-thrust priority under ESH, with an emphasis on energy utilization and management within a relevant manufacturing facility.**
  - Member companies interested in this research area are exploring alternate funding scenarios

Appendix: NMS Thrust Priorities

- **Summary of Potential Strategic NMS Thrust Changes, i.e. by 2016**
- **Patterning Thrust:**

  - Increase:
    - Dimensional control:
      - Reduce Variability
      - Enhance CD, Placement, and Process Control
    - Resist: Pattern collapse, LER, materials and polymer composition

  - Decrease: Nanoimprint Patterning

Nanoengineered Materials Thrust:

- Increase: Predictive Material Property and Synthesis Modeling
- Decrease: No decrease planned at this time.

Metrology Cross-Thrust:

- Increase:
  - Nanoscale Characterization and Defect Detection: Visual and Non-visual, especially for local characterization of surfaces and buried interfaces at the near atomic scale.
  - Patterning Metrology: Immersion, EUV, mask, maskless
  - Correlate Nanostructure to Macro-Scale Properties
- Decrease: No decrease planned at this time.

Environment, Safety, and Health Thrust:

- Increase:
  - Hazardous Emissions Reduction
  - ESH for Nanotechnology
  - Energy Utilization and Management
- Decrease: No decrease planned at this time.

OVERVIEW

Science Area: Device Sciences
Director: Kwok Ng

MISSION

Device Sciences (DS), through sponsoring university research world-wide, acquires scientific knowledge and innovation in all aspects of semiconductor devices, and meanwhile training highly skilled graduates in pertinent areas for the industry need, to enable member companies to successful commercialization of differentiating semiconductor-related products.

The areas of interest, aiming at evolutionary and revolutionary technologies for 14-nm generation and beyond to 9-nm, include the design, process technology, modeling, characterization, and reliability of semiconductor devices.

DS is organized into six thrusts:

- Digital CMOS Technologies (DCMOS)
- Non-Classical CMOS Research (NCR)
- Analog and Mixed-Signal Devices (AMS)
- Memory Technologies (MT)
- Device Sciences Modeling and Simulation (DSMS)
- Compact Modeling (CM)

ETAB had asked DS to consider merging of thrusts because DS has the most among five science areas (others have 2-3 thrusts). Our SACC went through rounds of discussions, going through different combinations of merging, and weighting the pros and cons of many thrusts. It was finally decided to remain unchanged since there is no obvious advantage for changing and they are there already.

ENVIRONMENT AND TRENDS

In CMOS scaling, according to the ITRS, it is expected to sustain for the next 15 years. The bulk process will proceed to SOI and eventually the ultimate structure will be multi-gate FinFET. Continuing improvement in the areas of high-K gate dielectrics, strain, and source/drain junction and contact will be necessary. In current technologies, the series resistance degrades about 1/3 of the idealized current, and that fraction is expected to go up with smaller dimensions. At the R/D stage, III-V and Ge semiconductors as alternate channel materials are being studied vigorously. These technologies are forecasted to be in production in year 2018. These equivalent scaling techniques are necessary to yield some relief to geometric scaling to keep up with the overall Moore's Law in performance, or to be able to deliver the same performance with reduced power (supply voltage).

In recent years, the circuit operating clock frequency in percentage increase per year has slowed down. It has been observed that it is now at about 4% increase per year. This is due to the design enhancement such as multi-core, and that power is becoming a limiting factor.

In non-volatile memory, the current floating-gate type is becoming harder to maintain the coupling ratio, and the charge-trapping type (SONOS) is foreseen as the dominant structure in the near future. This charge-trapping structure also has the added advantage of 3-D scaling as vertical NAND string to yield the smallest foot-print. However, both of these charge-based devices are facing limit in scaling the tunnel oxide, due to the fixed requirement of long retention time. To overcome the limitation, novel non-charge-based device options are being actively pursued. Examples are ReRAM, FeRAM, and MRAM. However, these newer cells are all 2-terminal cells, and a selection device in series is needed for the cross-point array. For DRAM cell, it is also expected to go to vertical channel structure in production in two years.

In parallel to scaling, one can also gain performance through functional diversification– performance gain without depending on scaling. This can be application-specific chips that involve integration of existing technologies. Examples are embedded flash, mixed-signal technologies and SoC, integrated optics, sensors, MEMS, energy harvesting, etc. In particular, due to the increasing demand of performance in wireless communication, analog and mixed-signal technologies are increasingly important. Another area is improvement in reliability and variability. One can certainly improve performance and cost through both. In memory devices, controlling variability will yield multi-bit cells. Yet another area is new functional devices– devices that can perform a function which usually requires a circuit block to do. Examples are SRAM and DRAM replacements.

Another industry trend is using multi-core design. In terms of technology requirement, examples are embedded memories and isolation. This trend also implies larger systems and more components in a chip. So naturally the issues are reliability and variability, and the requirement of low standby power or low off current. In particular, devices beating the fundamental subthreshold slope of kT/q are interesting options for research.

Multi-layer 3-D integration is a trend in the industry. The influence on and requirements from DS are stress, increased temperature, parasitics, noise/interference, and isolation. Optical interconnect is another trend. The requirements from DS in the long term are light sources, modulators, and detectors.

PRIORITIES

The main overall priorities for DS are listed as follows:

- Track and push ITRS-driven CMOS scaling towards limits.
- Ensure the success of III-V program in NCRC (Non-Classical CMOS Research Center).
- Manage the growth in analog and mixed-signal portfolio.
- Develop novel non-volatile memories of non-charge-based type.
- Maintain balance of technology and modeling which includes TCAD modeling and compact modeling.
- Ensure synergy and maximize transfer between DS and FCRP, in particular MSD and FENA.

Specific priorities per thrust are listed in the following.

Digital CMOS Technologies:

- Push scaling for the 16-nm node and beyond, to the end of Roadmap. New materials and processes are sought after.
- More focus on thin-body MOSFET structures, especially FinFET.
- Continue to increase strain to improve mobility.
- Continue to enhance high-K dielectric and metal-gate technologies.
- Optimize junction and contact to minimize source/drain series resistance.
- Develop low-power technologies with ultra-low off current or/and low supply voltage.

Non-Classical CMOS Research:

The goal is to develop MOSFETs of higher performance with alternate channel materials.

- Develop high-K gate dielectrics on III-V and Ge with good interfacial properties.
- Optimize source/drain series resistance.
- Study and plan for complementary *n*-channel and *p*-channel solution.
- Develop epitaxial growth of III-V and Ge materials on Si substrate.
- Develop more advanced structures of multi-gate FinFETs.
- Research on nano-scale materials and devices of carbon nanotube, graphene, and nanowire.

Analog and Mixed-Signal Devices:

- Optimize active and passive devices in analog metrics.
- Develop high-frequency power devices for analog applications with low on-resistance.
- Develop key processes and components for functional diversification (sensors, MEMS, energy harvesting…).
- Address I/O device needs for high speed or/and high voltage.

Memory Technologies:

- Develop novel non-charge-based non-volatile memory cells (ReRAM, FeRAM, MRAM…).
- Study selection devices required for 2-terminal cells.
- Develop 3-D NAND flash with vertical string.
- Explore self-assembly materials and processes.
- Research SRAM and DRAM replacement solutions.

Modeling and Simulation:

- Develop advanced process and device modeling tools and techniques for CMOS integration and devices.
- Develop advanced modeling tools and techniques for nano-scale materials, processes, and structures for memories.

Compact Modeling:

- Develop compact models for beyond-16-nm CMOS devices, including alternate device architectures.
- Develop compact models for analog devices, active and passive.
- Develop compact models for components of functional diversification.

STRATEGIC ACTION PLAN

Digital CMOS Technologies

- There is no core task currently. It is expected to get some core funding and low-level core activity for 2012.
- All four on-going tasks are Custom programs.

	2012	2013	2014	2015	2016
Advanced structure (FinFET) integration[1,2]	sustain				
High-K dielectrics[1,2]	sustain				
Contact and junction technology[1,2]	grow	sustain			
Reliability, variability, metrology[1,2]	sustain				

1,2 = ETAB,ITRS priority.

Non-Classical CMOS Research

- All core funding is put to support NCRC. The 2-year 2nd phase is completing June 2011. SACC had decided to continue onto the 3rd phase which will be 3-year.
- Ge FET is the p-channel solution for CMOS, to be started in following phase.
- Novel structures such as FinFET started in far years.

	2012	2013	2014	2015	2016
III-V MOSFET, n-channel: Integration[1,2]	sustain				
,, : High-K oxide[1,2]	Sustain		decline	sustain	
,, : Contact[1,2]	sustain				
Ge MOSFET, p-channel[1,2]			start	sustain	
Novel CMOS-like devices (multi-gate, nanowire, graphene…)[1,2]					start

Analog and Mixed-Signal Devices

- New cycle starts July 2011. This thrust has grown to be the biggest in DS.
- Currently there is no task on I/O devices.

	2012	2013	2014	2015	2016
Noise and isolation[1,2]	sustain				
RF/Power[1,2]	sustain				
Passives[1,2]	sustain				
I/O devices[1,2]	start	sustain			
Functional-diversification components (sensors, MEMS…)[1,2]	sustain				

Memory Technologies

- Due to decrease of thrust budget, new cycle is delayed from Aug. 2011 to Feb. 2012.
- Planar charge-trapping type of cells is sun-setting.
- Self-assembly processes and devices are longer-term and starting in far years.
- High proportion of Custom programs in this thrust.

	2012	2013	2014	2015	2016
(Planar) Charge-based NVM (FG and CT)[1,2]	decline	end			
3-D vertical gate NVM structures[1,2]	start	sustain			
Non-charge based NVM (ReRAM, FeRAM, MRAM…)[1,2]	sustain				
Selection device[1,2]	start	sustain			
Self-assembly processes and devices[1,2]					start
DRAM/SRAM[1,2]	sustain				

Modeling and Simulation

- Funding roughly equal for device and process modeling.
- New cycle starts March 2012.

	2012	2013	2014	2015	2016
Process simulations for CMOS & Memories[1,2]	sustain				
Device simulations for CMOS[1,2]	sustain				

Compact Modeling

- New research cycle starts January 2013. No solicitation in near future.
- Modeling for novel devices to be started in far years.

	2012	2013	2014	2015	2016
Advanced CMOS (FinFET, multi-gate…)[1,2]	sustain				
Other analog devices (power, bipolar)[1,2]	sustain				
Reliability & variability[1,2]	sustain				
Novel CMOS structures (III-V, nanowire…)[1,2]				start	
Functional-diversification components (sensor, energy…) [1,2]				start	

OVERVIEW

Science Area: Interconnect and Packaging Sciences
Director: Jon Candelaria

MISSION

The IPS has three components of its mission:

1) To create and explore advanced evolutionary, revolutionary, and transformative technologies for connecting elemental devices (transistors, capacitors, nanodevices, etc.) to each other and to the macro world targeting the 16nm node and beyond, including 3D and heterogeneous integration;

2) To facilitate strong bridges and foster new ideas between the packaging and interconnnect communities and develop closer ties to the system and design communities in universities;

3) To educate talented professional staff in the areas of Interconnect and Packaging Science through sponsored, innovative University research.

ENVIRONMENT AND TRENDS

In general the progress on Cu/low-k replacements such as CNTs, graphene, optical interconnects, air gaps, etc. has not yet been sufficient to warrant the integration of these options into mainstream manufacturing processes. Over the past few years, research on these "alternate interconnect systems" has shown that it will be harder to replace Cu-low-k than anticipated. CNTs still have significant challenges concerning controlled growth, high density, chirality control, contact resistance and kinetic inductance. Optical interconnects have up to now required too much power and area for nearly all chip-level interconnects, and molecular interconnects are still way too slow to be beneficial. In addition, any new choices for local interconnects as well as alternative backend dielectric insulator materials must be chosen to interface well with other materials, processes, and manufacturing equipment which will remain in existence for many years to come. Therefore Cu/low-k replacement options continue to require much more research and development before viable alternatives can be chosen for incorporation within advanced CMOS manufacturing processes.

However, because of significant breakthroughs over the past year or so in the area of optical technology for global interconnects, some of our member companies now see these alternatives appearing on their technology roadmaps within the next 4-to-7 years or so. Therefore, it is our belief that such options are viable research topic candidates for ramping up within the IPS portfolio, and direct dialogs with the FCRP-IFC research Center have been conducted to determine which of the options they have investigated may be most ready for migration to the IPS research portfolio over the next year or so.

There has been an increasing trend towards more system-level integration to deliver more functionally diverse solutions to the market. This diversification has manifested itself differently within our various member companies, however a few specific emerging application drivers include sensors, energy harvesting, bioelectronics, etc.

In addition, the continued drive towards increasing the functional density of computing platforms as well as their performance-to-power ratios on fixed and mobile platforms, has resulted in ever more serious challenges to deliver solutions that address intra-system data communication between multiple processing cores, processors-to/from-memories, etc. This data communication has not been able to keep pace with the rapid improvement in processing speeds. This issue, which has then in turn limited overall system performance improvements, has been referred to as 'the memory wall', and while it has been a problem to be addressed for almost twenty years or so, fewer and fewer options have been developed recently to address it adequately. At the same time the challenge itself has been getting worse because of the continually increasing gap between processor performance and memory technology and packaged communication improvements.

These challenges for increased system-level functional diversification, and for higher levels of integration densities and system performance, have driven the need to seriously explore 3D packaging and interconnect technology options, as well as improved chip/package co-designs, and novel system-level architectures.

We will be addressing these serious challenges with an increased emphasis on 3D technology research as well as with improved collaboration across all of the SRC Science Areas and Focus Centers in order to take more advantage of synergistic research and better align the overall sets of targets for our collective research portfolios.

The continued push for integrating new materials into smaller dimensions has generated an increased need for improved metrology and predictive reliability modeling for both the BEP and PKG thrusts. With current metrologies, structures and interfaces are no longer clearly resolved and there is an increasing need to image in three dimensions with atomic resolution for buried interface studies, defect void detection, nano-scale low-k pore investigation, etc. As structures become even smaller and more complex, current models are both more difficult to converge as well as validate. In addition, these metrology solutions ideally should be eventually capable of cost-effective incorporation into the manufacturing lines themselves.

In addition to the technological trends described above, there have been two major environmental factors affecting the IPS area which have had a substantial impact on the formulation and execution of the 2010 strategic plan. These factors are the potential instability in sources of matching state funding and a shift in funding from the BEP to the PKG thrust.

Given the very difficult budgetary constraints of many state governments during the economic downturn of the last three years, commitments of continued state funding are increasingly difficult to secure. In particular, we experienced a substantial reduction in our state matching funding commitments for 2010 and which has continued in to 2011/2012 which has a profound impact on our ability to maintain if not grow our research portfolio.

In response to these challenges, we are proactively identifying specific sources of new, and broader-based matching funding to offset these reductions. In 2011, we will be reviewing our overall Research Center strategy including their diminishing sources of leveraged funding, along

with these potential new sources of matching funds with the goal of creating a more stable resource platform upon which we will build our research portfolio for many years to come.

Lastly, due to the evolutionary business priorities of several of our members, there has been a continuous shift in the relative priority between funding for BEP and PKG tasks. This has resulted in a substantial, greater than 20%, relative reduction in the BEP budget and a proportionate increase in the PKG budget over the last two years. Coupled with an overall budget reduction for the IPS Science Area, the BEP Thrust has had to significantly streamline their research portfolio to focus on Cu / low-k extendibility issues including metrology, reliability, and predictive modeling. At the same time however, this shift has enabled the PKG Thrust to increase exploration of the emerging system-level packaging alternatives, 3D integration, advanced package level cooling options, and now potentially, global optical interconnect technologies.

PRIORITIES

The current strategy for IPS is to continue to focus the BEP and Packaging Thrust portfolios on the most critical needs of our members, while at the same time address the cross-Thrust issues through the clearly defined 'interface' area. The IPS portfolio is targeting the 16 nm node and beyond.

BEP emphasis continues to be aimed at ensuring the viability and reliability of scaled Cu / low-k interconnects. There is a need for increased interactions with circuit and system-level design researchers to better define the needs and potential for different interconnect as well as packaging solutions. There is an increased emphasis on predictive modeling and nano-metrology capability development.

Packaging research continues to drive thermal management alternatives, wafer level and thinned die packaging solutions, reduced chip-package spacing, and optimized power delivery, as well as an increased emphasis on viable optical global interconnect options. There is also a need to explore interactions between biological systems and electronic packages, as well as integration options for sensors to accommodate the functional diversification needs of the industry.

The Interface area focuses on 3D integration, die/package mechanical interactions, passive device integration, thermal management and functional diversification.

In general, the overall IPS research portfolio is currently aimed at addressing the twelve ETAB research priorities described below, listed in descending order of collective prioritization:

1) Development of novel 3D IC processes and architectures

2) Thermal, mechanical and electrical metrology / modeling for nanoscale materials and structures

3) Reliable interconnects to 16nm and beyond

4) Manufacturing options for reducing variability and enhancing reliability

5) New materials and processes for interconnects and packaging

6) Novel interconnect structures (including optical)

7) Ideas to increase bandwidth and I/O

8) Novel approaches for heat removal including novel packaging materials and advanced thermoelectric cooling structures

9) Integration of passives and sensors in die or on package

10) Compact modeling for interconnect system modeling, package modeling, chip-package power modeling and design

11) Emerging materials and passives for analog and mixed signal applications

12) ESH: Processes for interconnect technologies, consumables use and disposal, new material screening

STRATEGIC ACTION PLAN SUMMARY

IPS

- Identify additional and more stable sources of matching funding for both BEP and PKG research
- Expand 3D and heterogeneous system-in-a-package integration research
- Increase interaction with design researchers to better define the needs and potential for different interconnect and system-level packaging solutions
- Explore interactions between biological systems and electronic packages
- Interact with IFC technical programs and management through workshops and reviews to insure portfolio rationalization
- Continue to explore opportunities for collaborative interaction with other Science Areas, particularly with ICSS and NMS.

BEP

- Drive new research for reliability, metrology, and predictive modeling to address processing variability issues to enable the continued scaling of Cu / low-k interconnects to beyond 16 nm
- Explore new dielectric and conductive materials and novel methods of deposition
- Continue to explore interconnect-centric memory alternatives, such as cross-point memories, etc.

PKG

- Continue driving 3D and passive device integration
- Explore potential bio-compatible, sensor and board level applications
- Ensure adequate emphasis on simulation and characterization of overall system performance
- Continue to push near term focus on thermal management and control, and more efficient and effective I/O and power delivery solutions

BEP Strategic Portfolio Evolution

(Start, Grow, Sustain, Decline, or End)

BEP	***2012***	***2013***	***2014***	***2015***	***2016***
Cu Metal					
Reduce Resistance[1,2]	***sustain***				
Plating[1,2] and Electrochemical Deposition	***sustain***				***decline***
CMP[1,2]	***sustain***				
Cu Barriers and Caping Layers					
Process Advances[1,2]	***sustain***				
Minimal thickness Alternatives[1,2]	***sustain***				

BEP	2012	2013	2014	2015	2016
Etch and Low k					
Dielectric Materials[1,2]	sustain				
Plasma Etch and Damage[1,2]	sustain				
Reliability					
Dielectrics[1,2]	grow			sustain	
Cu[1,2]	grow	sustain			

BEP	2012	2013	2014	2015	2016
Modeling and Simulation					
Thermal, Mechanical[1,2]	sustain				
Variability Effects[1,2]	grow			sustain	
Emerging Technologies[1] (3D, optical, graphene, nanowires)		start	grow		
Advanced Metrology					
Interfaces[1,2]	sustain				
Reliability Failure Analysis[1]	grow	sustain			

BEP	*2012*	*2013*	*2014*	*2015*	*2016*
Emerging Technologies					
3D[1,2]	*grow*		*sustain*		
Optical interconnect & I/O	*grow*				*sustain*
Graphene, nanowires			*start*	*grow*	
Functional Diversification					
Interconnect Centric Memory[1,2]	*grow*			*sustain*	

PKG Strategic Portfolio Evolution

(Start, Grow, Sustain, Decline, or End)

PKG	*2012*	*2013*	*2014*	*2015*	*2016*
Thermal Management					
Hot Spot Solutions[1,2]	*sustain*			*decline*	
(Conventional) Thermal Interface Materials[1,2]	*sustain*	*decline*		*end*	
Advanced Solid State Refrigeration[1,2]	*grow*	*sustain*			
Thermal Metrology[1]	*grow*	*sustain*			
Board level and 3D package[1]	*grow*		*sustain*		

PKG	2012	2013	2014	2015	2016
Innovative Materials / Interfaces					
Adhesion and debonding models[1,2]	sustain	decline			end
Next generation Pb free solders[1,2]	decline	end			
Next generation active/passive integration on package[1,2]	grow	sustain			
Biocompatibility[2]	grow			sustain	

PKG	2012	2013	2014	2015	2016
Global Interconnects					
Novel global interconnect packaging[1,2] (incl. optical)	grow		sustain		
RF / analog / MS packaging[1,2]	sustain				
Chip package interactions[1,2]	sustain		decline		
Power delivery modeling[1]	sustain		decline		
Predictive performance modeling[1,2]	sustain				
3D SIP packaging[1,2]	grow		sustain		

PKG	*2012*	*2013*	*2014*	*2015*	*2016*
New Concepts					
Radical low cost packaging and thermal solutions[1,2]	*grow*		*sustain*		
Integration of package / die architecture with system and design inputs[1]	*grow*		*sustain*		
Nano-materials and metrologies applied to packaging[1,2]	*grow*	*sustain*			
Chip in board packaging	*grow*	*sustain*			

[1]*Etab priority* [2]*ITRS*

OVERVIEW

Science Area: Cross-Disciplinary Semiconductor Research
Director: Victor Zhirnov

MISSION

The GRC must continually review various scenarios of technologies and their applications. CSR looks for high risk or cross-disciplinary ideas, which may develop into unique research that may have a different, perhaps even shorter path to implementation than the FCRP or NRI. CSR is a seed grant program to encourage out-of-the-box proposals to address technology and application challenges in semiconductor research. Also CSR supports Forums, the development of new SRC initiatives, reviews the FCRP and NRI programs, as well as fund small projects to better define research programs of interest to the GRC.

ENVIRONMENT AND TRENDS

The semiconductor industry appears to be trifurcating into three business models; IDM's, fabless, and foundries. CSR programs must address the interdisciplinary needs of each of these sectors by creating research initiatives that encourage out-of-the-box ideas that would radically advance semiconductor technology and its applications.

PRIORITIES

- New memory technologies
- Semiconductor/Energy technology convergence
- Prospective chip architectures for low power
- Biocomputing
- Bioelectronics

STRATEGIC ACTION PLAN

- Support Development of a Research Center in Abu Dhabi
- Conduct a forum in Abu Dhabi on advanced photovoltaics
- Support Special Issue of Nanotechnology on emerging memories
- Support efforts to develop a bioelectronic research agenda
- Conduct fundamental study on the scaling limits of memory select device
- Support the biocomputing study group
- Launch study on fundamental physics of energy conversion
- Support the 2011 edition of ITRS Emerging Research Device Chapter
- Support technology assessment activities

IV: SRC SUPPORTING OPERATIONS

OVERVIEW

Area: Value Infrastructure Management
Director: Michael D. Connelly

MISSION

SRC's Value Infrastructure Management (VIM) group provides the people, processes and infrastructure necessary to proactively support and promote all aspects of SRC's value proposition. VIM's primary strategic role is to enable SRC's core value-based business services to adapt and evolve in support of SRC's strategic direction in a timely, efficient and effective manner. To address this challenge, the VIM group focuses on coordinated operations across all SRC programs addressing information collection, management and delivery methodologies and the myriad of office, communication, information, technology and security systems and infrastructure necessary for success. The premise behind VIM's mission is to enable SRC to optimally serve and collaborate with the global SRC community of researchers, students, participants, sponsors and member company personnel.

ENVIRONMENT AND TRENDS

In today's world, value management and the Web are integrally tied in the dual roles of managing and delivering value. Business must be web centric: for value delivery, for supplier integration into the value chain, and to meet continuously evolving expectations. Information and communication technologies evolve, business requirements expand and new opportunities are continuously presented. But so too are the associated costs, time, and complexity to assess, implement, deploy and support.

Successful value delivery, electronic or otherwise, demands both an efficient and quality-centric focus on all aspects of value management along the value chain. The information produced and submitted by researchers, managed and utilized by SRC staff and residents, and delivered to member company personnel is of optimal value only when effectively captured, managed and made available in a timely, coordinated and intuitive manner. SRC excels at delivering this value by sustaining a cost-effective and extensible infrastructure integrating robust business processes with relational database and web-centric technology solutions to best serve the SRC community.

Balancing timely delivery of information of the highest quality against the cost of continuous growth and increasing complexity of the supporting information architecture and technology infrastructure requires constant diligence. While innovative technological opportunities hold great potential, the operational resources required to develop, integrate, maintain and support them are challenging and must be continuously prioritized and assessed.

CURRENT PROGRAMS

The current Value Infrastructure Management group is organized in two programmatic areas:

- Value Management Programs
- Information Systems Architecture & Technology

The strategic focus of VIM efforts align across five critical components of the value chain:

- ***Business Operations*** focuses on integrating and supporting new and changing business needs as they impact value management and delivery and assessed in terms of supporting processes, information systems and technology infrastructure required.
- ***Information Management*** establishes the information architecture, collection and management methodologies and support processes necessary to ensure timely and accurate capture, embodiment and utilization of information necessary to support SRC's value proposition.
- ***Information & Technology Infrastructure*** efforts establish sustainable and scalable technology applications that serve the needs of the wide and diverse SRC community with emphasis on ensuring efficient and effective SRC operations.
- ***Communications & Value Delivery*** strives to provide the right information to the right minds at the right time to ensure that knowledge and awareness is transferred as effectively as possible. These efforts encompass not only SRC's robust web presence but all forms of coordinated communications and awareness efforts from branding, brochures and press releases to the SRC Corporate Annual report.
- ***Member Company Participation*** is a key leading indicator of the active engagement necessary to ensure a high degree of awareness and benefit from SRC. VIM continues to be highly engaged and proactive with the Value Chain, Student Relations and Executive TABs.

A key component of SRC's value proposition lies in its ability to manage efforts across all of these areas in a coordinated fashion.

In 2004, SRC initiated a multi-year strategic plan to enable a comprehensive redesign of its information management architecture that, once complete, would provide the basis for better supporting SRC's programmatic growth while enabling substantial improvements and expansion of the SRC web presence. Completed in 2006, SRC's next step was to launch a comprehensive review and assessment of web-based technologies, Assisted by an industry steering committee, these efforts culminated in the 2010 release of a top-to-bottom re-architecture and design of SRC's web presence supporting all aspects of SRC research and programmatic efforts in a highly scalable, sustainable and adaptable manner.

Today, SRC operates a highly robust web presence and supporting infrastructure covering all aspects of SRC and its multiple programs – GRC, FCRP, NRI, ERI and the SRC Education Alliance as well as new and emerging research initiatives.

STRATEGIC CHALLENGES AND ISSUES

As SRC evolves its value management infrastructure, so too must it address the myriad of challenges associated with promoting awareness of and access to all aspects of SRC's research and programmatic efforts. While the operational intricacies and scope of these programs may be complex, SRC's branding and communication must clear, coordinated and concise to ensure a highly involved and aware SRC Community. This is not only a challenge of value delivery

technologies, but more importantly, of how SRC must leverage opportunities for communication and awareness in a timely, coordinated and coherent manner.

As SRC's programs expand and evolve, so to must its ability to best serve a global community with diverse interests and inherent geographic and time barriers.

SRC must also seek, leverage and serve a common value proposition across all research programs. A near-term challenge is to do so by leveraging the Value Chain and Student Relations Advisory Boards to address the same challenges and opportunities across all SRC members and participants.

SRC will continue to embrace new technologies and methodologies to enhance SRC's value proposition but do so in a cost-effective manner. The advancement of unified information and communication technologies provide a myriad of new opportunities for consideration, yet SRC must prioritize and choose wisely, cognizant of cost, risk and operational complexity.

STRATEGIC ACTION PLAN

The following key strategic actions are deemed critical to the success of the Value Infrastructure Management efforts over the next five years:

- Continue to evolve SRC's new website presence and underlying infrastructure in support of all SRC programs
- Adapt to evolving business requirements using enabling infrastructure and process improvements
- Proactively engage the SRC Value Chain Advisory Board to enable and expand member interests and involvement across all SRC programs
- Leverage common SRC value management, communication and student program efforts across all SRC programs
- Increase awareness of the effectiveness of SRC industry liaison and associate programs and strive to expand the footprint of involvement
- Advocate for coordination and consistency in value management and delivery efforts across all SRC programs
- Leverage the new SRC website to improve information management efforts online and in real-time enabling more streamlined processes
- Assess and embrace opportunities to improve electronic communications and office technologies to seek a long-term unified strategy that will better serve the SRC and its community in a cost-effective and scalable manner.

OVERVIEW

Program Entity/Area: Student Relations
Manager: MaryLisabeth Rich

MISSION

The mission for SRC Student Relations is to work in a strategic partnership with all SRC research program members, sponsors, faculty and students to improve the quality and facilitate the flow of relevantly-educated students for careers with SRC member companies and the basic research community.

ENVIRONMENT AND TRENDS

In October of 2010, Student Relations was moved under the management of SRC Education Alliance. The opportunity exists to leverage the Education Alliance's status as a private foundation to expand funding sources for student initiatives while maintaining a strong connection to SRC research programs.

The downturn in hiring prevalent over the last few years is beginning to mitigate as the need for relevantly educated graduates begins to trend upward. Concern continues over immigration issues and the difficulty in hiring many of the international graduates. Diversity of the student population, both ethnicity and gender, is also a concern. A critical step to diversifying SRC's graduate student population and the future hiring pool for members is to grow the pipeline of students with permanent right to work in the US through the Undergraduate Research Opportunities Program, the Master's Scholarship Program and the Graduate Fellowship Program.

CURRENT PROGRAM

The current student programs include: 1) cost-effective access to student information via the website, 2) student/industry interaction through a series of events, 3) programs to attract academically qualified students (Master's Scholarship and Graduate Fellowship Programs and Undergraduate Research Opportunities), 4) collaboration with member company staffing organizations, including international members, through the SR TAB, and 5) proactive discussion of broader issues, e.g., immigration, diversity, and outsourcing.

STRATEGIC CHALLENGES AND ISSUES

The primary strategic challenges of Student Relations are to accomplish the mission in light of SRC's evolving research programs and Education Alliance's capacity to fundraise. Assisting member organizations in recruiting more SRC-funded students by finding a close technical match between company needs and addressing the permanent right to work status of potential hires remains a priority. Student Relations, in collaboration with the Value and Information Management team, continues to enhance member access to student information by improving the availability, integrity, and reporting of student data.

STRATEGIES/ACTION PLAN

- Implement an integrated SRC Student Programs management plan across all SRC research programs and the Education Alliance.

- Continue to provide easy, cost-effective access to students and student information for all SRC members by restructuring networking events to meet changing member needs, continuing to enhance the availability of student information through the Student Center on the SRC website and identifying and implementing processes to meet specific needs of international companies and US-based companies in offshore facilities.
- Expand programs to attract an academically qualified and diverse student population by expanding the Master's Scholarships and Graduate Fellowships to include all research programs. Eligibility requirements will continue to focus on PRTW status, academic qualification, and connection to SRC-funded research, with the Master's Scholarships focused on women and underrepresented populations. To provide a pipeline of diverse, academically qualified students for SRC research programs, Student Relations will work in conjunction with the Education Alliance to grow the Undergraduate Research Opportunities program and develop other programs to positively impact the academic qualification and demographics of the SRC student population.
- Enhance collaboration with member companies and company staffing organizations, including international members by expanding the current SR TAB to have representation from all SRC research programs. Through the SR TAB, Student Relations initiates efforts to understand and meet the specific needs of international companies and US-based companies hiring offshore and involves staffing organizations and hiring managers so that SRC students become their first choice for hire.
- Proactively participate in discussions of broader hiring issues by supporting the efforts of SIA in lobbying the federal agencies with regard to workforce issues.
- Leverage the SRC Education Alliance's status as a private foundation to increase funding from outside sources. These efforts may open doors for engaging potential new SRC members. Additional funds would allow Student Relations to broaden the scope of existing student programs, to grow and further develop the SRC Alumni Association, and initiate of new programs.

OVERVIEW

Area: Contracts and Intellectual Property
Director: Michael C. Phillips

MISSION

- Counsel and legal support for SRC, MARCO, NERC, TERC, Emerging Research Initiatives, and Education Alliance contract and intellectual property matters
- Contract Administration
    - Sponsored Research Agreements
    - Member License Agreements
    - Member and Participation Agreements
    - Operation Agreements
- IP Asset Management
    - Discovering, evaluating, mining, procuring IP
    - Protection of Members' rights and interests

ENVIRONMENT AND TRENDS

- Obtaining patent peace for Members
- New strategic alliances between Members and non-Members are being forged through the Emerging Research Initiative programs, TERC, and research consortia
- University research foundations are required to exist as self-supporting entities with revenues obtained from IP licensing
- Patent prosecution costs are steadily escalating
- Research at global universities is attractive to GRC Members

CURRENT PROGRAM

- Provide Sponsored Research Agreement ("SRA") support across all entities
- Process invention disclosures
    - Evaluate for value to Members
    - Determine likelihood of success as a patent application
    - Predict probable high prosecution costs
- Patent cost management and quality maintenance
    - Discontinue low probability of success applications
    - Expand qualification and selection of patent law firms
    - Rigorous invoice review and approval process

STRATEGIC CHALLENGES AND ISSUES

- Maintaining relationships with universities while resisting changes to SRA terms and conditions
- Managing an increasing number of blocking intellectual property ("BIP") issues
- Implementing changes to SRC business processes to adapt to the current business environment
- Supporting new business initiatives, collaborations, and research management objectives

STRATEGIC ACTION PLAN

- Continue to improve value provided to Members and transform relationships with universities from an adversarial to a partnership model
- Aggressively seek to resolve potential BIP issues as early as possible
- Make disclosures for qualified inventions promptly available to the IP Advisory Board for review and input, as appropriate
- Communicate with the IP Advisory Board, as necessary, on issues of importance or interest to members
- Monitor and, if necessary, revise newly implemented Export Compliance procedures
- Provide annual training to SRC employees in connection with Export Compliance
- Support the legal requirements of SRC's new business initiatives, specifically Emerging Research Initiatives
- Proactively identify legal requirements of SRC's growing Global Business Model
- Manage SRC equity participation and royalty revenues from various licensing arrangements