Semiconductor Research Corporation

# 2011-2015 SRC-GRC Strategic Plan

# 2011 – 2015 SRC-GRC Strategic Plan
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# I. Executive Summary

# I. Executive Summary

## Overview

During the spring of each year, SRC business planning includes development of an SRC-GRC Strategic Plan, covering the ensuing five years (2011-2015). The planning process continues in the fall of each year with the development of an Operations Plan for the next calendar year. The GRC Strategic Plan is developed by various Technical Advisory Committees/Boards in conjunction with SRC Directors and managers of corresponding functional areas. The plan is reviewed by the appropriate representatives of member companies, the OCE and finally, the SRC Board. The plan becomes a plan of record after the SRC Board approves it in 2Q/3Q of the year.

## Strategic Planning Process

The development of these plans utilizes outputs from various forums and analyses. SRC has periodically continued to conduct a Research Gap analysis to assess the amount of research investment necessary to address the ITRS challenges as compared with the actual investment occurring worldwide. This analysis highlights the criticality of research needs and respective shortfalls in funding, thereby providing a backdrop for the Strategic Plan. Additionally, the SRC community conducts a biennial GRC ETAB Summer Study and an SRC Annual Board Retreat to derive long-term strategic technical and business directions. Based on the outputs of these two forums, the ETAB develops an annual list of top-down, strategic technical priorities. The SACCs and T-TABs develop the Strategic Plans of the various science areas using the inputs from the forum and analyses described above. All of the information from these sources is then incorporated into the strategic technical priorities that are decided at the end of the annual ETAB strategic planning meeting. These priorities are the starting point for the plans shown in **Section III**. The ETAB strategic planning strategic priorities resulting from the 2010 ETAB Strategic Planning meeting are reproduced here:

- Scaling to Ultimate CMOS: Processes, Materials, Devices, Packages, and Systems
- Analog/Mixed Signal: Processes, Materials, Devices, Packages, and Systems
- Memories: Materials, Devices, Circuits, and Subsystems
- Low Power Architecting: Devices, Circuits, and Systems
- Power, Thermal, and Energy Management
- Design Productivity for Circuits and Systems
- Application-specific Integration of Diverse Technologies
- 3D IC Architecting: Technology, Design, Test, and CAD
- Multicore Homogeneous/Heterogeneous Systems
- Reliable, Resilient and Robust Technology, Circuits, and Systems
- ESH Stewardship for Materials, Processes and Energy

The specific strategic directions for each science area and thrust are outlined here. Each of these thrust level areas of emphasis are determined by the SACCs and T-TABs after the ETAB strategic priorities are set.

## Computer-Aided Design and Test Sciences (CADTS)

The design-related priorities in 2011 will have an overarching emphasis on power and energy, design for manufacturability, productivity, reliability and resilient robust systems. For digital technologies, the

emphasis is on variability, low power, multiple domains (voltage, clock, frequency, etc.) while analog topics include low voltage, synthesis, automated layout, test, and verification. System-level design issues include verification and test, software, multicore, 3D, reliability, memory subsystems, and multicore homogeneous/heterogeneous systems. Test issues include statistical test methods, more on chip self-test, mixed-signal, and 3D. Verification at all levels continues in importance.

## INTEGRATED CIRCUIT AND SYSTEMS SCIENCES (ICSS)

The organization of thrusts into Circuit Design and Integrated System Design is working well and the crosscut themes of Compact Modeling, Mixed-signal, and Memory help segment the research.
As the line between design and manufacturing becomes blurred, there exists increasing need and emphasis on cross science area collaboration. Priority changes from last year include an increased focus on interdisciplinary work (DS, IPS, CADTS). Areas of particular design importance include cost/yield, robustness, emphasis on low power systems, power management, and THz design. System-level focus on hardware/software approaches to satisfy reliability, variability, power, and thermal constraints and a memory emphasis from cache cell/architecture to system level coherency issues.

## DEVICE SCIENCES (DS)

In logics, the overall priority for DS is to track and push ITRS-driven CMOS scaling towards limits. New materials and processes are sought after for this purpose. Some important areas are strain to improve mobility, high-k gate dielectrics and metal gate, source/drain junction and contact, alternate channel materials such as III-V and Ge, etc. In analog technologies, active and passive devices are increasingly important for mixed-signal applications as well as functional diversification. In memory, the priority is to develop novel non-volatile memories of non-charge-based types, such as ReRAM, FeRAM, and MRAM, to replace the floating-gate and charge-trapping types. Apart from technology development, DS maintains a balance in modeling effort which includes process and device modeling, and compact modeling of the aforementioned technologies.

## NANOMANUFACTURING SCIENCES (NMS)

NMS addresses strategic nanofabrication technology challenges in two primary thrust areas: Environment, Safety, and Health (ESH) and Patterning (PAT), with emerging secondary themes of Nanoengineered Materials, Metrology, and reducing variability. NMS's Center for Environmentally Benign Semiconductor manufacturing satisfies the dual challenge of sustainable and high performance fabrication technologies, with low ESH impact. PAT thrust focuses on low variability patterning materials, techniques, and models that enable new cost curves for nanoelectronics fabrication. Additionally, this thrust seeds strategic exploratory work in functional, application specific materials and a predictive materials-by-design capability. It also supports novel metrology concepts that address emerging nanoscopic characterization needs, such as nanoscale defects and embedded local interface structures.

## INTERCONNECT AND PACKAGING SCIENCES (IPS)

The current strategy is to increase the research focus on the interface area between BEP and PKG, which has been clearly defined and includes 3D research. The IPS is targeting the 16 nm node and beyond. BEP's top priority is to ensure the viability and reliability of Cu / low k interconnects. There are increased interactions with design to better define the needs and potential for different interconnect solutions. There is also an increased emphasis on predictive modeling, nanometrology capabilities and interconnect centric memory research. Packaging research continues to push thermal management and control, I/O, power delivery and fundamentals of lead-free solder and fracture. There is also a growing need to explore biologically compatible packages and board level electronic packages among other

applications to accommodate the functional diversifications needs of the industry. The interface area focuses on 3D, die/package mechanical interactions, passive integration, thermal management and functional diversification.

## CROSS-DISCIPLINARY SEMICONDUCTOR RESEARCH (CSR)

One of SRC's missions is to provide a strategic vision for the possible scenarios of both technologies and their applications in the longer term (e.g. 15 years from now). As a part of this effort, SRC-GRC launches exploratory research targeting long-term applications through CSR.
Specific areas to target this year are to support efforts to develop new initiative in bioelectronics and to conduct a forum in Abu Dhabi on minimum energy electronic systems. Other fundamental studies on bio-electronic micro-systems, memory technology analysis and others will be pursued.

## VALUE INFRASTRUCTURE MANAGEMENT (VIM)

The mission of SRC's Value Infrastructure Management (VIM) group is to provide the people, processes and infrastructure necessary to proactively support and promote all aspects of SRC's value proposition. In essence, the primary strategic role of the VIM group is to position SRC's core value-based business services to adapt and evolve in support of SRC's strategic direction in a timely, efficient and effective manner.

# II. SRC Strategic Planning

## II. SRC- GRC STRATEGIC OVERVIEW

SRC business planning process, depicted in **Figure 1**, results in two documents that provide the basis of long-term directions and annual operations of SRC. Each year during the first two quarters, the SRC community develops a Strategic Plan covering the time horizon of the following five years. In the fall of each year SRC develops an Operations Plan for the next year. These plans are based on a number of inputs resulting from a variety of formal interactions among the SRC member representatives on advisory boards and the Board of Directors. In order to develop a foundation for the Strategic Plan, the OCE team conducts an annual assessment of long-term environmental trends in our industry and resulting challenges. Based on this assessment, the team also develops a five-year strategic vision and responses to these challenges. This strategic vision is reviewed with the Board to receive their inputs and ratification.

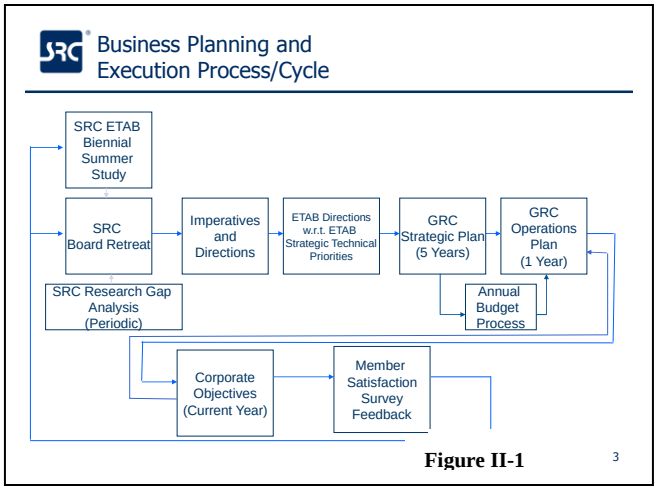


**Figure II-1**

This year, the SRC strategic planning and the SRC-GRC strategic planning will be separated into two separate plans. The SRC-GRC strategic plan is the subject of this document and deals with the SRC-GRC strategy. The SRC strategic planning will be done separately and will be developed directly with the SRC Board of Directors. The result of that plan will be the basis for the strategic imperatives.

## SRC-GRC STRATEGIES

The SRC Science Area Structure has proven to be responsive to the research needs of member companies and aligns well with the Focus Center themes. We expect that this structure will be sustained during the 2011-2015 timeframe of this Strategic Plan. However, there is a continuing need for Cross-Science-Area thrusts (Cross-thrusts) of which there are nine.

The nine managed Cross-thrusts that are currently operative are (1) 3D (List) (2) Mixed-Signal Technologies (Yeh), (3) Metrology and Characterization (Herr), (4) Modeling and Simulation (List), (5) Reliability (List), (6) Memories (Ng), (7) Multicore (Joyner), (8) Interconnect (List), and (9) Design for Manufacturability (Joyner). SRC also participates in an annual reliability symposium with SEMATECH and other agencies. SRC will continue its membership in the Nano Computational Network sponsored by NSF at Purdue that is developing computational tools for the atomistic level modeling of semiconductor devices.

A concerted effort to coordinate the SRC-GRC research with the research of the Focus Center Research Program (FCRP) is managed through the Science Area Directors and program managers. Each Director has responsibilities for a Focus Center that is most closely aligned to his respective area (see **Table 1**). The role of SRC-GRC Research Management in the FCRP includes coordination of FCRP and GRC Research Programs, Organization of the industry feedback to FCRP faculty at the annual reviews, and generation of reports for DARPA and members, and identification of FCRP research highlights for the FCRP Web site.

| Focus Center | MSD | IFC | FENA | GSRC | C2S2 | MuSyC |
|---|---|---|---|---|---|---|
| **GRC- Manager** | Kwok Ng | Scott List | Dan Herr | Bill Joyner | Dale Edwards | David Yeh |

**Table II-1**

In addition to the coordinating responsibilities that are detailed above, an extra step in the solicitation process is in place at the GRC proposal review stage for all researchers who have research interests in a Focus Center. This step requires the researchers to describe the differences and overlaps of the coordinated research to allow optimization of the funding decisions in order to benefit both programs.

There is also an active effort to keep the NRI projects and results coordinated with the GRC research portfolio. Particular attention is paid to the results coming from CSR projects that would be relevant to the NRI program.

## SRC-GRC PARTNERSHIPS

### SIA

SRC expects to continue to support SIA initiatives to call to the attention of Congress and the Administration the vital importance of the semiconductor industry to the economic health of the United States, and, in particular, to the relative decline in federal support for basic research in Physical Science and Engineering.

### NSF

SRC expects to continue its productive partnership with NSF over the planning period. The ten year partnership with NSF to support the Engineering Research Center on Environmentally Benign Semiconductor Manufacturing concluded in 2006. SRC-GRC and SEMATECH are continuing to support a center at the University of Arizona in this area post 2008.

The NSF/SRC-GRC initiative originally entitled 'Silicon Nanoelectronics and Beyond (SNB)' operated under an addendum to an umbrella MOU and provides for SRC (and hence industry) involvement in the planning, selection, and review of NSF-sponsored programs arising from the annual NSF-wide Nano Science and Engineering (NSE) solicitation. We have renewed this MOU to integrate NSF projects that are of interest to our members into the SRC research dissemination processes for faculty who choose to participate. We are also in the second year of a 3 year joint program in multicore research. We are working closely with NSF and individual universities to target new choices for Engineering Research Centers to have research directions that are of interest to the semiconductor industry.

### STATE GOVERNMENTS

SRC-GRC and the State of New York are jointly supporting the Center for Advanced Interconnect Science and Technology (CAIST) that is headquartered at the State University of New York at Albany and involves a substantial number of New York and university participants from other regions. We have joint programs with Texas (TxACE and CEMPI), with Georgia (IPC), and Arizona (ESH). These programs provide substantial leverage for member funds and serve as a model for other SRC/State research initiatives.

## NIST

SRC-GRC has also worked closely with NIST and we will seek ways to expand our domain of cooperation. The area of metrology and characterization will assume ever-increasing importance as the industry moves into the far-sub-nanometer regime. We have begun an interaction and cooperation in the area of device reliability and bioelectronics.

# III. SRC- GRC RESEARCH PROGRAM

## OVERVIEW

Science Area: Computer-Aided Design and Test Sciences
Director: William H. Joyner, Jr.

## MISSION

The Computer-Aided Design and Test science area has as its mission:

To promote diverse university research to strengthen member leadership in computer-aided design and test

- through tools and techniques that:
  - reduce cost and time-to-market through productivity improvement and correctness assurance
  - take full advantage of technology advances through linkages to manufacturing
  - enable high level/high value design
- through highly qualified graduate students who can fill key positions in member companies, and
- through strategic partnerships that leverage other funding sources

Member companies who employ SRC-supported students on summer internships, as postdocs, or as permanent employees are able to better extract the value of research in design tools and test techniques. Students can apply the results of their research, often immediately, in the industrial research and development environments of SRC members, giving them an advantage over those without the opportunity to guide and take early advantage of this work.

Design and test tools also can and must address cost pressures:

- by reducing time-to-market through the speedup of the logic and physical design process and the migration of this process to higher levels,
- by addressing product field failures through pre-manufacturing verification, efficient and effective manufacturing test, post-silicon validation, and cost-effective post-manufacturing in-field testing, and
- by coupling with the manufacturing process to control cost and improve yield as feature sizes shrink.

## ENVIRONMENT AND TRENDS

Highlights of the changing environment facing computer-aided design and test include:

- **The CADTS ecosystem**
  - CAD vendors depend on industry as a whole; need multiple sources for research
  - Design and CAD must do “due diligence” to extract highest performance from each technology node
  - Designer productivity not keeping pace with design complexity
  - Pre- and post-silicon validation an increasing focus due to time-to-market, lower average selling price, complexity factors
  - CAD spans the design/manufacturing boundary; high level decisions must comprehend the effects on manufacturing and post-silicon

- **The digital design environment**
  - 2-3 billion transistors on a chip (and increasing) with power constraints
  - Voltage supplies approaching 0.7 V (possibly lower)
  - Opposite pulls:
    – higher-level design to improve productivity
    – lower-level awareness to assure manufacturability
  - DFV/DFT/DFR critical as variability, diverse operating modes and power management techniques increase
  - Multi-cores, networks, true systems with 1012 ops/sec (challenge and opportunity)
  - Emerging devices and new technologies

- **The analog/mixed-signal/RFdesign environment**
  - Analog is still challenging from hertz to terahertz: fully integrated on chip, within package, or stand-alone.
  - Tools challenges include:
    – reliability assurance and temperature awareness
    – analog/mixed-signal test
    – automation for synthesis, physical design, verification
    – variation-tolerant analog design and optimization tools
    – tools for electromagnetic compatibility analysis
  - Applications in safety, health and energy require highly robust and fail-safe designs
  - Not scaling at the same rate as digital
    – harder to get to work with advanced processes
    – may need special processes and special devices
    – may drive 3-D IC design tools
  - Concerns remain about noise from digital circuits in SoCs with increased analog content

- **The system design environment**
  - Opportunity to exploit higher level design and verification for increased productivity
  - 3D issues pervade all science areas: test, synthesis, power are key
  - Software a major component of system design and affects CAD focus
  - System testing/verification an increasing challenge
  - Power/thermal issues at multiple levels – thermal variability a greater challenge
  - Homogeneous and heterogeneous multi-core designs hold promise (power reduction), challenge (software and applications) – also opportunity to gain CAD productivity
  - Cyber-physical systems an increased focus

- **CAD and test challenges**
  - Increased focus on reliability and resistance to failure with reduced ASP, higher volume, lower margins, test challenges
  - Design productivity still key – time-to-market critical
    – "Correct-the-first-time" important to reduce re-spins
    – Need to reduce size/cost of design teams
    – Optimization and system-level design are key
  - Post-silicon bring-up, validation, test
  - Mixed-signal/heterogeneous systems make test and verification more difficult

- 3D affects all thrusts
- Technology scaling and the resulting design rule explosion
- Observability obscured by complexity

Where do computer-aided design and test fit in the spectrum between fabrication technology and system design? Process technology and device/ process research provide devices and the ability to scale. Circuit/system design provides techniques to use these devices to accomplish a specific purpose. CAD and test provide the only productive interface between the two. Ever increasing design complexity decreases productivity and profitability and increases time to market. Tools and automation are the only viable mechanisms for dealing with this increased complexity of the design/manufacturing interface.

## PRIORITIES

The SRC Executive Technical Advisory Board highlighted these design-related priorities in 2010:

- Analog/Mixed Signal: Processes, Materials, Devices, Packages, and Systems
  - Synthesis, physical design, test and verification
- Memories: Materials, Devices, Circuits, and Subsystems
  - Memory subsystem test and validation
- Power, Thermal, and Energy Management
  - System-level power and thermal estimation and reduction
- Design Productivity for Circuits and Systems
  - High-level languages, real-time simulation and emulation
  - System-level exploration of specs, coverage, mapping, verification, test
- Application-specific Integration of Diverse Technologies
  - Novel architectures for emerging application spaces
- 3D IC Architecting: Technology, Design, Test, and CAD
  - 3D IC enabled applications
  - 3D implications in multicore applications
- Multicore Homogeneous/Heterogeneous Systems
  - 3D implications in multicore applications
  - Memory subsystem test and validation
  - Systematic post-silicon bring-up and debug
- Reliable, Resilient and Robust Technology, Circuits, and Systems
  - DFM through robust and resilient design for both analog and digital
  - Cross-system resiliency
  - Stochastic design techniques and methodologies
  - Process aware synthesis and physical design tools

Design priorities emphasized in the 2009 International Technology Roadmap for Semiconductors include:

- Resilience / reliability
- Power management
- Design productivity
  - System-level design, including analog/mixed-signal
  - Formal verification
  - Optimization/synthesis, including analog/mixed signal
- Design for manufacturability
  - Variability issues
  - Test issues

## STRATEGIC ACTION PLAN

- Classical challenges expected to remain difficult: power and energy, design for manufacturability, productivity, reliability
- Continue exploration of leading technologies for CAD
  - Digital: variability, low power, multiple domains (voltage, clock, frequency, etc.)
  - AMS: low voltage, synthesis, automated layout, verification, test
  - System-level design: verification and test; software, multicore, 3D, reliability
- Thrusts and emphases:
  - Design issues (low power/voltage, variability, resilience, high-level, productivity)
  - Test issues (statistical test methods, more on chip self-test, mixed-signal)
  - Verification issues (mixed-signal, coverage, post silicon validation)
- Link with other science areas as traditional boundaries blur
- Continue leveraging initiatives and cooperation with NSF, DARPA, States, CDADIC, FCRP, GRC SAs, others

| | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| **Logic-Physical Design** | | | | | |
| DFM/variability[1,2] | sustain | | | | |
| Core/block level tools[2] | sustain | decline | | | |
| Failure-resistance[1,2] | grow | | | sustain | |
| A/MS/RF[1,2] | grow | | sustain | | |
| Hi-level/syst/SOC tools[1,2] | grow | | sustain | | |
| Diverse tech/arch[1] | | | | start | grow |
| Power/clock distribution | decline | | end | | |
| 3D tools[1] | grow | | sustain | | |

| | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| **Verification** | | | | | |
| Core technologies[2] | sustain | | decline | | |
| RTL/Coverage [2] | sustain | | | decline | |
| System-level[1,2] | grow | | sustain | | |
| Software/microcode [1] | grow | | | sustain | |
| A/MS/RF [1] | grow | | sustain | | |
| **Test** | | | | | |
| Stuck-at fault | decline | end | | | |
| System/SoC [1] | grow | | sustain | | |
| Delay-based | decline | | end | | |
| Correlation-based [2] | grow | | | | sustain |
| Post-silicon validation [1] | grow | | sustain | | |
| A/MS/RF [1] | grow | | sustain | | |

(1)=ETAB priority (2)=ITRS

## OVERVIEW

Science Area: Integrated Circuits and Systems Sciences
Director: David C. Yeh

## MISSION

To conduct research in advanced integrated circuits and systems design that will

- Exploit advances in IC technology while overcoming associated barriers and challenging conventional notions of the circuits and systems design space
- Develop a circuits and systems research portfolio that will provide exceptional value to our MCs – with a focus on design-based performance gains
- Facilitate the training of highly-skilled graduates to help fill design engineering needs of MCs

In the circuit design space, the emphasis will be on advances for robust high-performance low-power digital logic and memory, analog, RF, and mixed-signal designs. In the integrated system design space, the emphasis will be on advances that enable robust and power efficient designs for both high performance and embedded systems comprised of silicon and software for diverse applications. Additional emphasis will be placed on defining algorithms and methodologies required for critical design activities in diverse application domains.

## ENVIRONMENT AND TRENDS

As the semiconductor fabrication industry approaches the fundamental limits of CMOS device scaling, the device property improvements at each new technology node become harder to achieve. Thus, extracting the expected performance and economic advantages of moving to new process nodes is harder now than in the past. New design techniques are necessary to facilitate and augment the march towards using advanced processing nodes. The push to integrate more functionality on-chip and achieve higher performance to drive down the cost per transistor continues but this also encounters more obstacles with each succeeding process node. Modeling the parasitic effects and process variability that are critical for robust behavior (of both analog and digital components) is getting much more difficult. These factors increase the risk and thus, the uncertainty of recovering costs of doing designs in these advance process nodes. This is driving more companies towards design-based performance gains – extracting more out of existing technologies through the use of more innovative design. This is especially true for analog/mixed-signal applications. Furthermore, members' exploration of new application domains may drive research along possibly different vectors and this will have a critical impact on the portfolio in the future.

Some of the critical topics on the scaling path that impact design techniques include SRAM stability, self-testing and self-repairing systems, and dynamically reconfigurable circuits. This type of research will be targeted towards leading edge process nodes and the types of devices and interconnect that technology will enable. On the functional diversification and design-based performance gains front, work will need to address topics such as higher performance analog/mixed-signal design and efficient multi-core operation. Some of the subtopics include circuit architectures, embedded memory, software, I/O, and communications. As chip transistor counts reach several billion, the additional circuit and system complexity leads to long and difficult new product de-bug and launch cycles. Circuitry for built-in self–testing, self-calibration, and self-repair is needed to help overcome these issues. For many system applications, software as well as hardware has a strong impact on overall system performance. Thus, software is one of the keys to allowing dynamic response and optimization of power,

performance, reliability, and other system metrics. In the multi-core design space, this is especially true. Research on improving compilers and multi-core programming models, supporting programming, debug, and optimization needs of system developers is needed.

Long-term, the emergence of non-classical devices along with new diverse applications will dramatically impact design techniques. While some of these devices have appeared, such as double-gate structures, it is not too early to re-examine the design process to determine how to best take advantage of the new structures. New applications in areas such as medical, energy, and specialized automotive electronics are emerging. Even so, the same design issues of power, reliability, test, manufacturability, and accurate modeling will remain substantial challenges.

- Technology driven constraints impact circuits and memories
    - Process variability, leakage, low-Vdd, new devices (eg. FinFETs)
- Increased transistor count worsens technology constraints
    - POWER will always be an issue – even beyond CMOS
    - Increased statistical variation → analysis requires more "sigmas"
    - Increased probability of reliability-induced failure: SEU and aging
    - Resilient circuits and architectures will be essential
    - Design complexity increases faster than transistor count
- SoC/SiP integration of multiple functional blocks + software
    - Long and difficult new product development and launch cycles, including software development and debug
    - Challenge to optimize digital and analog circuits
- Diverse applications drive architecture/ IP/circuits/ software
    - Design constraints cover power, performance, cost, safety, …
- Emphasis on multi-core and system reliability
    - Software concurrency, tools, debug, verification, programming model
- The spectrum of research is broad and interdisciplinary
    - Digital, analog, mixed-signal, RF, memory & I/O
    - Novel structures: e.g. multi-gate, 3D integration, & carbon-based
    - Reliability impact: cause-effect and solutions
- Design research on the CMOS scaling path continues
    - Adaptive systems: self-test & self-repair
    - Dynamic reconfigurable circuits & systems
    - Covers frequencies of interest from Hz to hundreds of GHz
- Focus on design-based performance gains
    - Supplementing technology-based gains
- High fab cost for PI's constrains research focus
    - Need is to focus on areas where universities add value

## PRIORITIES

In 2009, the International Technology Roadmap for Semiconductors underwent a major update and the Design Chapter still states that the cost of design is the greatest threat to continuation of the semiconductor roadmap. Both hardware and software are included in this cost and are expressed as silicon complexity and system complexity. The revision also highlights five cross-cutting challenges: design productivity, power management, design for manufacturability, interference, and reliability.

- Silicon Complexity

    - Non-ideal scaling of device parasitics and supply/threshold voltages
    - Coupled high-frequency devices and interconnects
    - Manufacturing variability
    - Complexity of manufacturing handoff
    - Scaling of global interconnect performance relative to device performance
    - Decreased reliability

- System Complexity
    - Reuse
    - Verification and Test
    - Cost-driven Design Optimization
    - Embedded Software design
    - Reliable Implementation Platforms
    - Design Process Management

The SRC GRC ETAB also gives guidance on priorities and those have strong overlap with ICSS. The following list of priorities has been extracted from the 2014 ETAB Priorities as those with the highest weighting.

- Analog and Mixed-Signal Design
    - Synthesis, physical design, test and verification
    - Ultra-low powered digital and analog circuits
    - Compact Models: device (active/passive)
    - High performance low power signal I/O
    - RF and mixed-signal circuits for M2M communication
- Homogeneous/Heterogeneous Multi-Core Architectures
    - 3D implications in multicore applications
    - Highly parallel system architectures
    - New explicit programming models for embedded and general purpose multicores
    - Software
    - Methods for systematic post silicon bring-up and debug
    - Memory subsystem test and validation, including coherence assurance
    - System level exploration specification, coverage, mapping
- Memories
    - Non-volatile memory: eg. phase-change
    - Novel cell and system architectures
- Coping with Variability/Reliability Issues
    - Manufacturing options for reducing variability and enhancing reliability
    - Design for manufacturability through robust design for both digital and analog (regularity, statistical optimization, configurable redundancy, etc)
    - Resiliency across the system including process variability, tunable with respect to reliability, and adaptable circuits and architectures
    - Methods to assess system reliability in the face of new failure
    - Stochastic design techniques and methodologies
    - Merging of configurable design, fault diagnosis, and testing
    - Autonomic approaches for variability and aging compensation
    - Deterministic fabrication methods
- Design Solutions for Thermal/Power
    - System-level power and thermal estimation and reduction

    - Active feedback between thermal solutions and processor
- Functional Diversification - Applications
    - 3D IC enabled applications
    - Integration of key components eg. sensors, energy harvesters and storage
    - Systems level: hi-level languages, real-time simulation and emulation
    - Cross-functional integration of semiconductor systems design with human factors and cognitive systems research
    - Novel architectures for emerging application spaces

## STRATEGIC ACTION PLAN

Looking forward, the strategies and actions are still driven by the member companies through various channels, which include inputs at the SACC, ETAB, and BoD levels. The organization of thrusts into Circuit Design and Integrated System Design is working well and the crosscut themes of Compact Modeling, Mixed-signal, and Memory help segment the research. With the new ETAB allocation at the thrust level, the influence of the SACC on the portfolio evolution has been decreased. Even so, there still is a balance between the Circuit Design and Integrated System Design thrusts, with support for a small amount of Compact Modeling. The SACC was also in favor of a small amount of Director's Discretion funding. The portfolio is also influenced by the work proposed in response to our solicitations, which may include ideas not anticipated in the process and our desire to only fund excellent research.

As the line between design and manufacturing becomes blurred, there exists increasing need and emphasis on cross science area collaboration. Leveraged funding dollars are still highly valued and ICSS participates in several activities with NSF, CDADIC and MISCIC. Other new sources of leveraged funding will be considered if any appear beneficial for member companies. Finally, delivering value to the members in the form of relevant research and hirable students skilled in design remain our highest priorities.

- New Changes in Research Priority (since last year)
    - Increased focus on interdisciplinary work (DS, IPS, CADTS)
- Design research for silicon CMOS, reflected in Needs documents
    - Objective functions include power, performance, reliability, thermals, cost/yield and robustness
    - Underlying processes cover leading-edge to mature
    - Areas cover digital, analog, mixed-signal, RF, and memory
    - Abstraction from circuit level to systems architectures
    - Product usage from general purpose to application-specific
    - More diverse systems/applications research; embedded and high performance multicore architectures; 3D exploration; power gating optimization
    - Circuits and systems research for applications in health, medical, and security: emphasis on low power systems, power management, and THz design
    - System-level focus on hardware/software approaches to satisfy reliability, variability, power, and thermal constraints
    - Memory emphasis from cache cell/architecture to system level coherency issues
    - Monitor long-range research – FCRP, NRI, etc., engage when ready
- Continue to increase value to member companies
    - e-Workshops in ICSS, including monthly TxACE e-workshop,
    - e-Kickoffs for new programs
    - Help members identify/hire excellent students
        - Invite final year students to reviews, present posters, and meet Members

- Remote access to reviews; travel assistance through RCP funds
- File IP where there is value
- ICSS newsletter
- Improve design-to-fab infrastructure for PIs
  - MOSIS special pricing/GRC fab $ match program
  - Investigate other opportunities for fabrication
- Work across science areas where appropriate
  - CADTS – system tools; DS – predictive CMs; IPS – packaging;
- Partnering with other entities for leveraging

| Circuits | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| Memory | sustain | | | | |
| Functional Diversification - Applications | grow | sustain | | | |
| Analog & MS Design | grow | sustain | | | |
| Homogeneous/ heterogeneous multicore | sustain | | | | |
| Coping with variability and reliability | grow | sustain | | | |
| Design solutions for thermal/power | sustain | | | | |

| Systems | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| Memory | sustain | | | | |
| Functional Diversification - Applications | grow | sustain | | | |
| Analog & MS Design | sustain | | | | |
| Homogeneous/ heterogeneous multicore | sustain | | | | |
| Coping with variability and reliability | grow | sustain | | | |
| Design solutions for thermal/power | grow | sustain | | | |

## OVERVIEW

Science Area: Nanomanufacturing Sciences (NMS)
Director: Daniel Herr

## MISSION

The mission of NMS is to deliver value by developing and providing early access to evolutionary, breakthrough, and high impact material, process, and metrology technologies for scaled CMOS, targeting a half pitch of ≤16 nm, and analog/mixed signal technologies, including:

- Low variability, centered, and cost effective nanofabrication options that enable extensible scaling [≤16 nm];
- Functional diversification of charge-based technologies, which may be in addition to scaling options that increase performance and functionality; and
- High-performance and sustainable options that enable 3-D applications;

## ENVIRONMENT AND TRENDS

The semiconductor industry's growth rate relies on continuously enhanced functional density to provide increasing value. However, it is becoming increasingly difficult to manage variability, cost, reliability, yield, sustainability, and factory operations with conventional scaled subtractive/damascene processing alone. This trend implies an increasing number of potential insertion opportunities for breakthrough innovations in materials and nanofabrication technologies that address these emerging digital and analog/mixed signal challenges.

## PRIORITIES

The following high level strategic research priorities are aligned with the NMS mission and driven by the 2010 ETAB identified critical research needs:

- **Centered, low variability fabrication technologies:** Demonstrate that the percent of manufacturing variability need not increase with functional density, i.e. with respect to dimension, overlay, placement, composition, architecture, etc. This includes the development of predictive models that provide insight into key nanomanufacturing tool-material-process trade-offs and their synergistic impact on reducing material, process, structural and property variability;

- **New cost curves for nanoelectronics fabrication:** Develop novel materials, modeling, process and equipment options that:
    - Enable extensible nanoelectronics fabrication, defect detection, and yield management into the sub-10 nm domain;
    - Strengthens the predictive capabilities of the computational lithography infrastructure;
    - Leverage the existing fabrication infrastructure;

- **Functional diversification:** Design, identify, and enable the integration of customized materials with electronically useful functionality for high value application opportunities, which includes an emerging emphasis on predictive materials by design and quantitative material structure-property correlations;

- **Sustainable, high performance fabrication:** Extend sustainable, benign, high performance nanomanufacturing technologies into the sub-10 nm domain.

  This set of challenges provides a framework for assessing the potential of proposed and continuing research to achieve critical science area objectives.

## STRATEGIC ACTION PLAN

Note: [[1] ETAB rating of near term/long term critical research challenge; [2] ITRS challenge]

**Nanomanufacturing Sciences Research [NMS], Overall:** NMS' 2011-2015 research strategy is designed to:

- Identify and address strategic member/ETAB and ITRS identified needs;
- Leverage, engage, and influence targeted government and regional initiatives;
- Engage tool suppliers early in the research cycle;
- Enhance GRC/NMS-FCRP-NRI synergy, coordination, and networking;
- Evolve thrusts to anticipate and reflect non-traditional drivers.

**Patterning Research [PAT]:** This thrust creates and enables high-impact potential patterning options for low variability extensible scaling, centered at 16 nm and beyond, and scaling independent technologies, which address member-identified and projected ITRS difficult patterning challenges.

- 2011-2013: Assess potential of directed self-assembly for insertion in 2016.
- 2011-2015:
  - Address the patterning variability challenge, such as through an increased emphasis on predictive computational lithography and process aware compact models;
  - Develop critical knowledge-base of post-NGL patterning options;
  - Identify and address strategic member-identified patterning needs.

| | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| **Patterning Options that Enable Reduced Variability, Extensible Scaling, and Enhanced CD and Process Control**[1(28/28),2] | start | grow | | | |
| Directed Self-Assembly[1(26/23),2] | sustain | | | grow | |
| Process Aware Compact Models, such as Directed Self-Assembly.[1(26/23),2] | start | grow | | | |
| NGL Extensibility / Limits[1(26/23),2] | sustain | | | decline | |
| Alternate/Non-Traditional Patterning[1(26/23),2] | sustain | | grow | | |
| Nanoimprint Patterning[2] | decline | end | | | |

**Nanoengineered Materials [NEM] (Currently Positioned Under the Patterning Thrust):** This thrust explores emerging research material and process options that address strategic member scaling and analog/mixed signal needs.

- 2011-2015: Launch targeted seed projects that explore prioritized needs and uncover emerging opportunities;

- 2011-2015: Increase the emphasis on developing predictive material and process TCAD tools that enable a functional and structural materials-by-design capability.
- 2011-2014: Establish a formal process for efficiently communicating breakthrough results with other thrusts and science areas.

| | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| Functional Diversification on CMOS, including materials for enabling 3D IC applications*[1(28/29),2] | grow | | | sustain | |
| ITRS-Identified Emerging Research Materials [CMOS and A/MS][1(26/25),2] | start | grow | | | |
| Process & Material TCAD[1(25/26),2] | sustain | | grow | | |
| New CMOS and Analog/Mixed Signal Materials/Processes[1(24/26),2] | | start | grow | | |
| Deterministic Fabrication*[1(18/18),2] | sustain | | decline? | | |

**Metrology and Nano-Characterization Research [MET]:** This cross-thrust addresses strategic member company and ITRS-identified nano-characterization and metrology knowledge gaps. It explores emerging and enabling sub-10 nm measurement options.

- 2011-2012: Secure resources to address GRC/FCRP/NRI nano-characterization gaps.
- 2011-2015:
  - Increase and maintain visibility of metrology results across thrusts and science areas.
  - Update assessment of GRC/FCRP/NRI nano-characterization gaps.
  - Leverage and engage strategic relevant metrology initiatives.

| | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| **Nanoscale Characterization and Defect Detection - Visual and Non-visual[1,2]**<br>▪ Atomic and Nanoscale 3D Structure and Defects, including Polymers and other low-Z Materials<br>▪ Nanoscale Probe-Sample Measurement Uncertainty<br>▪ Nanoparticle Monitors for ES&H, which include Size, Dose, and Composition | start | grow | | | |
| Correlate Nanostructure to Macro-scale Properties[1,2]<br>▪ In-Situ, Non-destructive, 3D Imaging of Atomic and Nanoscale Materials<br>▪ In-Situ Measurements that Enable Enhanced Synthetic and Process Control<br>▪ Methods that Resolve and Separate Surface from Bulk Properties<br>▪ Measuring Coupled Nanoscale Phenomena | start | grow | | | |
| Known Characterization Methods Limits[1,2] | | | start | grow | |
| Metrology for MFD and DFM[2]<br>▪ Integrated Measurement and Modeling Tools<br>▪ Uniformity Measurements of Nanoscale Properties of Over Large Areas | | | start | grow | |
| Patterning Metrology[1,2] | sustain | | | | |

**Environment, Safety, and Health Research [ESH]:** This thrust explores sustainable, high-performance semiconductor materials and processes for future technologies. During this strategic period, the ESH strategic action plan is to enable new material screening technologies and demonstrate the feasibility of consumable, energy, and water use reduction.

- 2011-2013: Develop new funding approaches and multi-regional initiatives.
- 2011-2015:
  - Address strategic high priority ESH research needs, especially with respect to understanding the ESH impact of new and nanomaterials and sustainable processes;
  - Increase and maintain visibility of ESH research in other GRC thrusts.

| Near term growth through leverage | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| **ESH Impact of New and Nanomaterials** | | | | | |
| ▪ New Materials and Associated Processes [Includes packaging materials and processes] [2] | grow | | sustain | | |
| ▪ ESH for Nanotechnology[2] | grow | | sustain | | |
| ▪ New Technologies for Detection, Hazard Assessment, and Toxicity Screening [1(20/22),2] [Includes Dose Definition, Hierarchical Assessment, and Data Mining] | grow | | sustain | | |
| **ESH/Process Improvement** | | | | | |
| ▪ **Reduction in "Net" Water Use**[1(20/22),2] | sustain | | | | |
| ▪ **Energy:** Sources/Utilization/Management[1(20/22),2] | | | start | grow | |
| ▪ Chemical Utilization and Waste Reduction[2] | sustain | | | | |
| ▪ Hazardous Chemicals Use Reduction [Includes sustainable chemical substitution] [2] | sustain | | | | |
| ▪ Reduction of Hazardous Emissions[2] | sustain | | decline | | |
| ▪ Design for ESH/Life-Cycle Analysis[2] | | | start | grow | |

**Factory System Research [FAC]:** This research area's mission is to provide enabling technology to improve the effectiveness of factory operations.

- 2010: This GRC thrust is scheduled to conclude in December 2010;
- Member companies interested in this research area are exploring alternate funding scenarios, such as an SRC Emerging Initiative.

## Appendix: NMS Thrust Priorities – Summary of Potential Strategic ETAB/SACC Thrust Changes, i.e. by 2015

**Patterning Thrust:**

- **Increase:** Reduce Variability and Enhance CD, Placement, and Process Control
- **Decrease:** Nanoimprint Patterning?

**Nanoengineered Materials Thrust**

- **Increase:**
  - Materials to Enable 3D Applications*;
  - Process and Material TCAD;
- Decrease: Deterministic Fabrication?*

**Metrology Cross-Thrust:**

- **Increase:**
  - Nanoscale Characterization and Defect Detection - Visual and Non-visual
  - Correlate Nanostructure to Macro-Scale Properties

**Environment, Safety, and Health Thrust:**

- **Increase Through Leverage:** ESH Impact of New and Nanomaterials
- **Decrease:** Hazardous Emissions Reduction?*

* These proposed changes require further clarification to ensure strategic NMS SACC-ETAB alignment.

## OVERVIEW

Science Area: Device Sciences
Director: Kwok Ng

## MISSION

Device Sciences (DS), through sponsoring university research world-wide, acquires scientific knowledge and innovation in all aspects of semiconductor devices, and meanwhile training highly skilled graduates in pertinent areas, to enable member companies to successful commercialization of differentiated semiconductor-related products.

The areas of interest, aiming at 16-nm generation and beyond, include the Design, Process Technology, Modeling, Characterization, and Reliability of semiconductor devices.

DS is organized into six thrusts:

- Digital CMOS Technologies (DCMOS)
- Non-Classical CMOS Research (NCR)
- Analog and Mixed-Signal Devices (AMS)
- Memory Technologies (NT)
- Device Sciences Modeling and Simulation (DSMS)
- Compact Modeling (CM)

## ENVIRONMENT AND TRENDS

In CMOS scaling, according to the ITRS, it is expected to sustain for the next 15 years. The bulk process will proceed to SOI and eventually the ultimate structure will be 3-D, multi-gate FinFET. Continuing improvement in the areas of high-k gate dielectrics, strain, and source/drain junction and contact will be necessary. At the R/D stage, III-V and Ge semiconductors as alternate channel materials are being studied vigorously. These equivalent scaling techniques are necessary to yield some relief to geometric scaling to keep up with the overall Moore's Law in performance.

In non-volatile memory, the current floating-gate type is becoming harder to maintain the coupling ratio, and the charge-trapping type (SONOS) is foreseen as the dominant structure in the near future. This charge-trapping structure also has the added advantage of 3-D stacking as vertical NAND string to yield the smallest footprint. However, both of these charge-based devices are facing limit in scaling the tunnel oxide, due to the fixed requirement of long retention time. To overcome the limitation, novel non-charge-based device options are being actively pursued. Examples are ReRAM, FeRAM, and MRAM.

In parallel to scaling, one can also gain performance through functional diversification, performance gain without depending on scaling. This can be application-specific chips that involve integration of existing technologies. Examples are embedded flash, mixed-signal technologies and SoC, integrated optics, MEMS, etc. Another area is improvement in reliability and variability. One can certainly improve performance and cost through both. In memory devices, controlling variability will yield multi-bit cells. Yet another area is new functional devices–devices that can perform a function which usually requires a circuit block to do. Examples are SRAM and DRAM replacements.

Another industry trend is using multi-core design. In terms of technology requirement, examples are embedded memories, isolation, and 3-D integration. This trend also implies larger systems and more components in a chip. So naturally the issues are reliability and variability, and the requirement of low standby power or low off current. In particular, devices beating the fundamental subthreshold slope of *kT/q* are interesting options for research.

## PRIORITIES

The main overall priorities for DS are listed as follows:

- Track and push ITRS-driven CMOS scaling towards limits.
- Ensure the success of III-V program in NCRC (Non-Classical CMOS Research Center).
- Develop novel non-volatile memories of non-charge-based type.
- Maintain balance of technology and modeling which includes process and device modeling, and compact modeling.
- Ensure synergy, maximize transfer, and avoid overlap between DS and FCRP, in particular MSD and FENA.

Specific priorities per thrust are listed in the following.

**Digital CMOS Technologies:**

- Push scaling for the 16-nm node and beyond, to the end of Roadmap. New materials and processes are sought after for this purpose.
- Continue to increase strain to improve mobility.
- Optimize junction and contact to minimize source/drain series resistance.
- Study thin-body MOSFETs not requiring high channel doping (SOI and FinFET).
- Develop low-power technologies with ultra-low off current or/and low supply voltage.

**NCR:**

The goal is to develop MOSFETs of higher performance with alternate channel materials.

- Develop high-k gate dielectrics on III-V or/and Ge with good interfacial properties.
- Optimize source/drain series resistance.
- Study and plan for complementary n-channel and p-channel solution.
- Develop epitaxial growth of III-V or/and Ge materials on Si substrate.
- Research advanced FETs on nano-scale materials of carbon nanotube, graphene, and nanowire.

**Analog and Mixed-Signal Devices:**

- Develop key processes and components for functional diversification (sensors, MEMS…).
- Develop high-performance, low-power I/O devices.
- Optimize active and passive devices for analog and mixed-signal applications.

**Memory:**

- Develop novel non-charge-based non-volatile memory cells (ReRAM, FeRAM, MRAM…).
- Develop 3-D NAND flash with vertical string.
- Explore self-assembly materials and processes.
- Research SRAM and DRAM replacement solutions.

**Modeling and Simulation:**

- Develop advanced modeling tools and techniques for nano-scale materials, processes, and structures for memories.
- Develop advanced process and device modeling tools and techniques for CMOS devices.

**Compact Modeling:**

- Develop compact models for beyond-16-nm CMOS devices, including alternate device architectures.
- Develop compact models for analog devices, active and passive.
- Develop compact models for components of functional diversification.

## STRATEGIC ACTION PLAN

### Digital CMOS Technologies

- There is no core task currently. It is expected to get some core funding for 2011.
- Custom program is substantial in this thrust.

| | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| Advanced structure (FinFET) integration[1,2] | sustain | | | | |
| High-k dielectrics[1,2] | sustain | | | | |
| Contact and junction technology[1,2] | grow | sustain | | | |
| Reliability, variability, metrology[1,2] | decline | sustain | | | |

1,2 = ETAB,ITRS priority.

### NCR

- All core funding is put to support NCRC. The 2-year 2nd phase is completing June 2011. SACC will decide on the 3rd phase by ~August 2010.
- Look for leverage funding from outside sources.

| | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| III-V MOSFET, n-channel: Integration[1,2] | sustain | | | | |
| ,, : High-k oxide[1,2] | sustain | | | decline | sustain |
| ,, : Contact[1,2] | sustain | | | | |
| III-V MOSFET, p-channel[1,2] | sustain | | | | |
| Novel CMOS-like devices (FETs on nanowire, graphene…)[1,2] | | | | | start |

### Analog and Mixed-Signal Devices

- New cycle starts July 2011. This thrust is expected to grow further. Solicitation process starts September 2010.

| | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| Noise and isolation[1,2] | sustain | | | | |
| RF power[1,2] | sustain | | | | |
| Passives[1,2] | sustain | | | | |
| I/O devices[1,2] | start | sustain | | | |
| Functional-diversification components (sensors, MEMS…)[1,2] | sustain | | | | |

**Memory Technologies**

- New cycle starts August 2011. Solicitation process starts October 2010.
- High proportion of Custom program in this thrust.

| | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| Charge-based NVM (FG and CT)[1,2] | decline | sustain | | end | |
| Non-charge based NVM (ReRAM, FeRAM, MRAM…)[1,2] | sustain | | | | |
| 3-D structures[1,2] | start | sustain | | | |
| Self-assembly processes and devices[1,2] | | | | | start |
| DRAM/SRAM[1,2] | sustain | | | | |

**Modeling and Simulation**

- Funding roughly equal for device and process modeling.
- New cycle starts January 2012. Solicitation process starts March 2011.

| | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| Process simulations for CMOS & Memories[1,2] | sustain | | | | |
| Device simulations for CMOS[1,2] | sustain | | | | |

**Compact Modeling**

- New research cycle starts January 2013. No solicitation in near future.

| | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| Advanced CMOS (FinFET, multi-gate…)[1,2] | sustain | | | | |
| Analog & mixed-signal devices[1,2] | sustain | | | | |

| | | |
|---|---|---|
| Reliability & variability[1,2] | sustain | |
| Novel CMOS structures (III-V, nanowire…)[1,2] | | start |
| Functional-diversification components (sensor, energy…) [1,2] | sustain | grow |

## OVERVIEW

Science Area: Interconnect and Packaging Sciences
Director: Scott List

## MISSION

The IPS has three components of its mission:

- To create and explore advanced evolutionary, revolutionary, and transformative technologies for connecting elemental devices (transistors, capacitors, nanodevices, etc.) to each other and to the macro world targeting the 16nm node and beyond, including 3D and heterogeneous integration;
- To facilitate strong bridges and foster new ideas between the packaging and interconnnect communities and develop closer ties to the system and design communities in universities; and
- To educate talented professional staff in the areas of Interconnect and Packaging Science through sponsored, innovative university research.

## ENVIRONMENT AND TRENDS

In general the progress on Cu/low k replacements such as CNTs, graphene, optical interconnect has not been sufficient to warrant the integration of these options into the IPS portfolio. Over the past few years, research on CNTs and other "alternate interconnects" have shown that it will be harder to replace Cu-low k than anticipated at first glance. CNTs have severe limitations concerning controlled growth, high density, chirality control, contact resistance and kinetic inductance. Optical interconnects currently use too much power and area for nearly all on die interconnects and molecular interconnects are too slow. In addition, any new choice for local interconnect must be chosen to interface well with any new technology chosen for the next switch. These Cu/low k replacement options will continue to be generally delegated to the IFC for research.

There has also been an increasing trend to both increased functionality and functional diversification. This diversification has manifested itself differently in the various member companies. Specific emerging applications include sensors, energy harvesting, bio-compatible electronics, extreme miniaturization, multi-cores and memory. These applications drive a new need for 3D packaging, 3D interconnect, MEMs, board level interconnect, a better interface with design and system, bio-compatible packaging, extreme bandwidth to memory solutions and new, interconnect centric memory research.

The continued push for integrating new materials into smaller dimensions has generated an increased need for improved metrology and modeling for both the BEP and PKG thrusts. With current metrologies, structures and interfaces are no longer clearly resolved and there is an increasing need to image in three dimensions with atomic resolution for buried interfaces. As structures become smaller and more complex, current models are both more difficult to converge and validate.

In addition to the technological trends described above, there have been two major environmental factors affecting the IPS area which have had a substantial impact on the formulation and execution of the 2010 strategic plan. These factors are the potential instability in sources of matching state funding and a shift in funding from the BEP to the PKG thrust.

Given the very difficult budgetary constraints of many state governments during the economic downturn of the last two years, commitments of continued state funding are increasingly difficult to secure. In

particular, we experienced a substantial reduction in our state matching funding commitments for 2010 which had potentially profound impacts on our portfolio. In response to these reductions, we explored both contract to grant conversions as well as the identification of additional sources of matching funding to offset such reductions. For 2010, we were fortunately able to secure new sources of matching funding to supplement specific losses with the creation of another research center. In particular, the Center for Electronic Material Processing and Integration (CEPMI) was formed in 2010 at the University of North Texas. Its current focus includes both low k materials and plasma processing. In the future, its focus may expand to include both 3D and packaging initiatives if additional state or corporate funding becomes available. In the future, we need to proactively explore new sources of matching funding as well as other contract to grant conversion solutions to ensure continuity in funding to our researchers.

Due to the decrease in emphasis of fab related processing of several of our members, there has been a continuous shift in the relative priority between funding for BEP and PKG tasks. This has resulted in a substantial, approximately 20%, relative reduction in the BEP budget and a proportionate increase in the PKG budget over the last two years. Coupled with an overall budget cut to the science area, the BEP thrust has had to significantly streamline their research portfolio to focus on core Cu / low k extendibility issues.

## PRIORITIES

The current strategy for IPS is to continue to emphasize specific features of the BEP and Packaging thrust portfolios while at the same time addressing the inter-thrust issues through the clearly defined interface area. The IPS is targeting the 16 nm node and beyond. BEP emphasis continues to be ensuring the viability and reliability of Cu / low k interconnects. There are increased interactions with design to better define the needs and potential for different interconnect solutions. There is also an increased emphasis on predictive modeling, nanometrology capabilities and interconnect centric memory research. Packaging research continues to push thermal management and control, I/O, power delivery and fundamentals of lead-free solder. There is also a growing need to explore interactions between biological systems and electronic packages among other applications to accommodate the functional diversifications needs of the industry. The interface area focuses on 3D, die/package mechanical interactions, passive integration, thermal management and functional diversification. In general the IPS research priorities span the twelve ETAB priorities described below, listed in descending order of collective prioritization:

- Development of novel 3D IC processes and architectures
- Thermal, mechanical and electrical metrology / modeling for nanoscale materials and structures
- Reliable interconnects to 16nm and beyond
- Manufacturing options for reducing variability and enhancing reliability
- New materials and processes for interconnects and packaging
- Novel interconnect structures (including optical)
- Ideas to increase bandwidth and I/O
- Novel approaches for heat removal including novel packaging materials and advanced thermoelectric cooling structures
- Integration of passives and sensors in die or on package
- Compact modeling for interconnect system modeling, package modeling, chip-package power modeling and design
- Emerging materials and passives for analog and mixed signal applications

- ESH: Processes for interconnect technologies, consumables use and disposal, new material screening

## STRATEGIC ACTION PLAN

IPS

- Identify additional and more stable sources of matching funding for both BEP and PKG research
- Expand 3D and heterogeneous system in a package integration research within IPC
- Increase interaction with design to better define the needs and potential for different interconnect and thermal solutions
- Continue pursuing interface research on a voluntary basis within each thrust
- Pursue co-funding tasks with ICSS for interconnect/design optimizations
- Drive 3D research through both the IPC and CAIST centers
- Explore interactions between biological systems and electronic packages
- Interact with IFC technical programs and management through workshops and reviews to insure portfolio rationalization
- Continue joint funding with NSF of multi-core tasks
- Expand reliability and metrology initiative with NIST
- Explore expansions into interconnect centric memory applications
- Continue interactions with other science areas for collaborative work, particularly with ICSS and NMS.

BEP

- Extend the viability of Cu / low k interconnects to 16 nm and beyond
- Initiate interactions with NIST for collaborative research on metrology and reliability
- Solicit new programs evaluating interconnect schemes for beyond Cu low k, particularly from the functional diversification perspective
- Define future needs for interconnect centric memory, e.g. cross-point memory or HAR contacts

| BEP | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| **Cu Metal** | | | | | |
| Reduce R[1,2] | sustain | | | | decline |
| Plating[1,2] | sustain | | | | |
| CMP[1,2] | sustain | | | | |
| **Cu Barriers** | | | | | |
| Process Advances[1,2] | sustain | | | | |
| Minimal thickness Alternatives[1,2] | sustain | | | | |

| BEP | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| **Etch and Low k** | | | | | |
| Dielectric Materials[1,2] | sustain | | | | |
| Plasma Etch and Damage[1,2] | sustain | | | | |
| **Reliability** | | | | | |
| Dielectrics[1,2] | sustain | | | | |
| Cu[1,2] | grow | | sustain | | |

| BEP | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| **Modeling and Simulation** | | | | | |
| Cu / Low k Extendibility | end | | | | |
| Thermal, Mechanical[1,2] | sustain | | | | |
| Variability Effects[1,2] | start | grow | | | sustain |
| Radical Alternatives[1] | | | | start | grow |
| **Advanced Metrology** | | | | | |
| Interfaces[1,2] | sustain | | | | |
| Reliability Failure Analysis[1] | grow | | sustain | | |

| BEP | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| **Radical Alternatives** | | | | | |
| 3D[1,2] | grow | | | sustain | |
| Optical[1,2] | grow | | | | |
| Graphene, nanowires, spin[2] | | | | | start |
| **Functional Diversification** | | | | | |
| Interconnect Centric Memory[1,2] | start | grow | | | sustain |

PKG

- Continue to push near term focus on thermal management and control, I/O, power delivery and fundamentals of lead free solder
- Continue driving 3D and passive expansion through IPC and CAIST
- Explore potential bio-compatible, sensor and board level applications
- Ensure adequate emphasis on simulations and characterizations of overall system performance

| PKG | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| **Thermal Management** | | | | | |
| Hot Spot Solutions[1,2] | sustain | | | | |
| Thermal Interface Materials[1,2] | sustain | | decline | | end |
| Advanced Solid State Refrigeration[1,2] | grow | | sustain | | |
| Thermal Metrology[1] | grow | | sustain | | |
| Board level and 3D package[1] | start | grow | | sustain | |

| PKG | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| **Innovative Materials / Interfaces** | | | | | |
| Adhesion and debonding models[1,2] | sustain | | decline | | |
| Next generation Pb free solders[1,2] | decline | | end | | |
| Next generation active/passive integration on package[1,2] | grow | | sustain | | |
| Biocompatibility[2] | start | grow | | | sustain |

| PKG | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| **Global Interconnects** | | | | | |
| Novel global interconnect packaging[1,2] | start | grow | | sustain | |
| RF / analog / MS packaging[1,2] | sustain | | | | |
| Chip package interactions[1,2] | sustain | | | decline | |
| Power delivery modeling[1] | sustain | | | decline | |
| Predictive performance modeling[1,2] | grow | sustain | | | |

| PKG | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|
| **New Concepts** | | | | | |
| Radical low cost packaging and thermal solutions[1,2] | start | grow | sustain | | |
| Integration of package / die architecture with system and design inputs[1] | start | grow | sustain | | |
| Nano-materials and metrologies applied to packaging[1,2] | grow | sustain | | | |
| Chip in board packaging | grow | | sustain | | |

## OVERVIEW

Science Area: **Cross-Disciplinary Semiconductor Research**
Director: Victor Zhirnov

## MISSION

The GRC must continually review various scenarios of technologies and their applications. CSR looks for high risk or cross-disciplinary ideas, which may develop into unique research that may have a different, perhaps even shorter path to implementation than the FCRP or NRI. CSR is a seed grant program to encourage out-of-the-box proposals to address technology and application challenges in semiconductor research. Also CSR supports Forums, the development of new SRC initiatives, reviews the FCRP and NRI programs, as well as fund small projects to better define research programs of interest to the GRC.

## ENVIRONMENT AND TRENDS

The semiconductor industry appears to be trifurcating into three business models; IDM's, fabless, and foundries. CSR programs must address the interdisciplinary needs of each of these sectors by creating research initiatives that encourage out-of-the-box ideas that would radically advance semiconductor technology and its applications.

## PRIORITIES

- Bioelectronics
- Semiconductor/Energy technology convergence
- Prospective chip architectures
- New memory technologies
- Circuits for beyond-CMOS nanodevices
- Collective phenomena in materials and devices

## STRATEGIC ACTION PLAN

- Support efforts to develop a bioelectronic research agenda
- Conduct forums in Abu Dhabi on minimum energy electronic systems and advanced photovoltaics
- Conduct fundamental study on the performance projections of bioelectronic microsystems
- Develop an analysis of potential embedded memory technologies
- Support technology assessment activities
- Support Special Issue of Proc. IEEE on nanoelectronics
- Complete book on Nanomorphic Systems for Bioelectronics
- Conduct e-workshops on CSR research

# IV. SRC Supporting Operations

## OVERVIEW

Area: Value Infrastructure Management
Director: Michael D. Connelly

## MISSION

SRC's Value Infrastructure Management (VIM) group provides the people, processes and infrastructure necessary to proactively support and promote all aspects of SRC's value proposition. VIM's primary strategic role is to enable SRC's core value-based business services to adapt and evolve in support of SRC's strategic direction in a timely, efficient and effective manner. To address this challenge, the VIM group focuses on coordinated operations common across all SRC program entities including all student-related programs, events and initiatives, value management and delivery methodologies, proactive communication strategies and the myriad of information systems and technology initiatives and infrastructure critical to success. The premise behind VIM's mission is to enable SRC to optimally serve and collaborate with the global SRC community of researchers, students, government participants, sponsors and member company personnel.

## ENVIRONMENT AND TRENDS

In today's world, the Web plays an integral role in the delivery of value. Business must be Web centric: for value delivery, for supplier integration into the value chain, and to meet continuously evolving expectations. Information technology evolves, business requirements expand and new value-based opportunities are continuously presented. But so too do the associated costs, time, and complexity to implement, deploy and support. SRC recognizes this and has continued to address these challenges since the release of its first Web site in 1996. Today, SRC operates a complex Web presence covering all aspects of SRC and its multiple programs – GRC, FCRP, NRI, and the SRC Education Alliance and well as new and emerging research initiatives.

Successful value delivery, electronic or otherwise, demands a quality-centric focus on all aspects of value management along the value chain. The information produced and submitted by researchers, managed and utilized by SRC staff and residents, and delivered to member company personnel is of optimal value only when effectively captured, managed and made available in a timely, coordinated and intuitive manner. SRC excels at delivering this value by sustaining a cost-effective and extensible infrastructure integrating robust business processes with relational database and web-centric technology solutions to best serve the SRC community.

Balancing timely delivery of information of the highest quality against the cost of continuous growth and increasing complexity of the supporting information architecture and technology infrastructure requires constant diligence. While innovative technological opportunities abound, the operational resources required to develop, integrate, maintain and support them are daunting and must be continuously prioritized and assessed.

## CURRENT PROGRAMS

The current Value Infrastructure Management group is organized in three programmatic areas:

- Student Programs
- Value Management Programs
- Information Systems Architecture & Technology

The strategic focus of VIM efforts align across five critical components of the value chain:

- ***Student Programs*** which strives to support, manage and advocate for all aspects of student programs across all SRC program entities. The strategic nature of this area is of sufficient criticality to SRC's value proposition that it is documented independently in this report.
- ***Business Assessment*** focuses on continuous integration of new and changing business needs as they impact value management and delivery and assessed in terms of supporting processes, information systems and technology infrastructure required.
- ***Information Management*** establishes the information architecture, collection and management methodologies and support processes necessary to ensure timely and accurate capture, embodiment and utilization of information necessary to support SRC's value proposition.
- ***Information & Technology Infrastructure*** efforts establish sustainable and scalable technology applications that serve the needs of the wide and diverse SRC community with emphasis on ensuring efficient and effective SRC operations.
- ***Communications & Value Delivery*** strives to provide the right information to the right minds at the right time to ensure that knowledge and awareness is transferred as effectively as possible. These efforts encompass not only SRC's robust Web presence but all forms of coordinated communications and awareness efforts from branding, brochures and press releases to the SRC Corporate Annual report.

VIM strives to integrate efforts across all areas to better serve the SRC community in a manner consistent with the growth and capability of the supporting processes, infrastructure and technologies.

## STRATEGIC CHALLENGES AND ISSUES

As SRC evolves its value management infrastructure, so to must it address the myriad of complexities associated with promoting awareness of and access to all aspects of SRC's programmatic research efforts. While the intricacies of these programs may be complex, SRC's branding and communication message must not be. This is not only a challenge of value delivery technologies, but more importantly, of how SRC must leverage opportunities for communication and value delivery in a timely, targeted and coherent manner.

A key component of SRC's value proposition lies in its ability to manage and deliver information. In 2004, SRC initiated a multi-year strategic plan to enable a comprehensive redesign of its information management architecture that, once complete, would provide the basis for enabling substantial improvements and expansion of the SRC Web presence. Completed in 2006, the next step launched a comprehensive review and assessment of Web-based technologies to form the basis for a comprehensive redesigned SRC Web presence supporting all aspects of SRC research and programmatic efforts in a highly scalable, sustainable and adaptable manner. Throughout these efforts, an equally important challenge has been to ensure member company involvement in the identification and validation of requirements coupled with the formation and evolution of the new Web site design. Such efforts have been underway since 2007 with development complete in 2009 to support a full launch at the start of 2010.

## STRATEGIC ACTION PLAN

The following key strategic actions are deemed critical to the success of the Value Infrastructure Management efforts over the next five years:

- Fully integrate and evolve SRC's new Web site presence and underlying infrastructure in support of all SRC programs
- Adapt to evolving business requirements using enabling infrastructure and process improvements

- Proactively engage the SRC Value Chain advisory board and expand to enable interests and involvement of all SRC programs
- Leverage common SRC value management, communication and student program efforts across all SRC programs
- Increase awareness of the effectiveness of the GRC Liaison program and strive to leverage similarly successful programs across all programs
- Advocate for coordination and consistency in value management and delivery efforts across all SRC programs
- Leverage the new SRC Web site to improve information management efforts online and in real-time enabling more streamlined processes
- Continue to support and improve internal information systems and office technologies in support of SRC operations

## OVERVIEW

Area: SRC Student Programs
Manager: Virginia Wiggins

## MISSION

The mission for SRC Student Programs is to work in a strategic partnership with all SRC entity members, sponsors, faculty and students to improve the quality and facilitate the flow of relevantly-educated students for careers with SRC member companies and the basic research community.

## ENVIRONMENT AND TRENDS

The next five years present major challenges and opportunities for SRC Student Programs. Current programs are managed under the SRC umbrella for the various research entities and draw financial support directly from the research entities. The opportunity exists to leverage the SRC Education Alliance's status as a private foundation to expand funding sources while maintaining a strong connection to the research entities.

The expectation is that the downturn in hiring prevalent over the last two years will mitigate as the need for relevantly educated graduates will begin to trend upward in response to the demand for technical workforce by 2011. Concern continues over immigration issues and the difficulty in hiring many of the international graduates. Diversity of the student population, both ethnicity and gender, is also a major concern. The SRC environment includes many opportunities for student interactions, e.g., TECHCON, student/industry networking events, e-workshops, contract reviews, Industry Liaisons, and the web. These interfaces should continue to evolve to be more effective in meeting SRC member needs, but could also be restructured to better meet the needs of the entire SRC community including the international members. At the same time, the need for a pipeline of undergraduates with permanent right to work in the US into SRC's various graduate programs becomes more critical with a rapidly changing global environment, making support for the Undergraduate Research Opportunities program through the SRC Education Alliance of prime importance.

## CURRENT PROGRAM

The current student programs include: 1) cost-effective access to students and student information via the web, 2) student/industry interaction through a series of events, 3) programs to attract academically qualified students (Graduate Fellowship and Master's Scholarship Programs, Undergraduate Research Opportunities), 4) proactive involvement with member company staffing organizations, including international members, through the SR TAB, etc., and 4) proactive discussion of broader issues, e.g., immigration, diversity, and outsourcing, which affect the SRC student populations. These elements are currently managed primarily under the SRC research entities with some Fellowships and Scholarships and the URO Program managed under the SRC Education Alliance.

## STRATEGIC CHALLENGES AND ISSUES

The primary strategic challenge for SRC Student Programs is to accomplish its mission in light of SRC's evolving research structure. Strategies include: 1) implement integrated Student Programs management across all SRC research entities; 2) leverage the SRC Education Alliance's status as a private foundation, 3) continue to provide easy, cost-effect access to students and student information, 4) expand programs to attract an academically qualified and diverse student population, 5) enhance proactive involvement with member companies and company staffing organizations, including

international members, and 6) proactively participate in discussions of broader issues, e.g., immigration, diversity, and outsourcing.

## STRATEGIC ACTION PLAN

- Implement an **integrated SRC Student Programs management plan across all SRC research entities.** This includes managing all student information in one Student Center on the web and expanding the Graduate Fellowship and Master's Scholarship Programs to include all entities. It also includes the possibility of developing other programs across all entities and expanding the current Student Relations TAB to include members from all sponsoring organizations.
- **Leverage the SRC Education Alliance's status** as a private foundation. This would allow expansion of current student programs with outside funding as well as development of new initiatives, e.g., an SRC Alumni Association. It also opens doors for engaging potential new SRC members. A funding model that allows the Education Alliance to be self-sustaining is required; a business plan to engage/develop sponsors in corporate, government and philanthropic sectors, an Executive Director, and a Board of Directors aligned with Alliance goals are basic requirements.
- Provide **easy, cost-effective access to students and student information** for the members, including the international members. Events like TECHCON, TechConnects, CareerConnections Online, and FCRP and NRI networking events allow networking between students and the industry while providing opportunities to build bridges between the university community and the industry. These events will evolve to meet the changing needs of member companies, e.g., moving TECHCON to an annual event. Methods need to be explored to improve the quality of networking events, including combining some events to ensure a viable number of student participants. Web-based capabilities will continue to improve by implementing processes to ensure data integrity and increase companies' easy access to student information through a single Student Center. Efforts will continue to meet the needs of international companies and US-based companies seeking to hire SRC students in offshore facilities.
- Expand programs to **attract an academically qualified and diverse student population**. Methodologies to better balance the ratio of students with permanent right to work in the US to international students in US-based universities must be developed. The Graduate Fellowship and the Master's Scholarship Programs have the objective of attracting outstanding students with permanent right to work in the US and could be expanded to include all research programs. The Master's Scholarship Program also addresses diversity issues, targeting ethnic minorities and women. Development of undergraduate initiatives, e.g., the Undergraduate Research Opportunities program, as a feeder to the SRC graduate programs is critical. Outside sources of funding through the SRC Education Alliance could contribute significantly to the growth of the GFP, MSP, and undergraduate initiatives as well as allowing the development of other programs to positively impact the academic qualification and demographics of the SRC student population.
- **Enhance proactive involvement with member company staffing organizations so that SRC students are their first choice for hire**. The level of involvement of GRC Student Relations TAB members has increased significantly over the last few years with the addition of members who understand their company's strategy for hiring and developing technical talent. Efforts are being explored to expand the current SR TAB to include representation from all SRC research entities Understanding and meeting the specific hiring needs of international companies and US-based companies off-shore facilities also needs exploration.
- Proactively **participate in discussions of broader issues**, e.g., immigration and outsourcing, which affect the SRC student population. The Student Relations TAB must provide a forum for discussions that lead to a thorough understanding of the issues and explore reasonable solutions.

SRC must also support the efforts of other organizations, specifically SIA, to improve government policies on visas and other immigration issues related to students.

## OVERVIEW

Area: Contracts and Intellectual Properties
Director: Michael Phillips

## MISSION

Counsel and legal support for SRC, GRC, MARCO, NERC, TRC, TERC, NINECO, and Education Alliance contract and intellectual property matters: Contract Administration (Sponsored Research Agreements, Member License Agreements, Member and Participation Agreements, Operation Agreements); IP Asset Management (Discovering, evaluating, mining, procuring IP and Protection of Members' rights and interests

## ENVIRONMENT AND TRENDS

- Obtaining patent peace for Members.
- New strategic alliances between Members and non-Members are being forged through the TRC program, TERC, NINECO, and research consortia.
- University research foundations are required to exist as self-supporting entities with revenues obtained from IP licensing.
- The USPTO is granting fewer patent applications while prosecution costs are escalating.
- Research at global universities is increasingly attractive to SRC Members.

## CURRENT PROGRAM

- Provide SRA support across all entities.
- Process invention disclosures: Evaluate for value to Members, Determine likelihood of success as a patent application, Predict probable high prosecution costs
- Patent cost management and quality maintenance: Discontinue low probability of success applications, Expand qualification and selection of patent law firms, Rigorous invoice review and approval process
- Maintain and improve university relations issues.

## STRATEGIC CHALLENGES AND ISSUES

- Maintain relationships with universities while resisting changes to SRA terms and conditions.
- Managing an increasing number of BIP issues.
- Implement changes to SRC business processes, as necessary, to adapt to the current business environment.
- Support new business initiatives, collaborations, and research management objectives.
- Support all phases of SRC globalization (members and universities).

## STRATEGIC ACTION PLAN

- Continue to improve value provided to Members and transform relationships with universities from an adversarial to a partnership model.
- Aggressively seek to resolve potential BIP issues as early as possible.
- Make disclosures for qualified inventions promptly available to the IP Advisory Board for review and input, as appropriate.

- Communicate with the IP Advisory Board, as necessary, on issues of importance or interest to members.
- Monitor and, if necessary, revise newly implemented Export Compliance procedures.
- Provide annual training to SRC employees in connection with Export Compliance.
- Support the legal requirements of SRC's new business initiatives, specifically TRCs.
- Proactively identify legal requirements of SRC's growing Global Business Model.
- Manage SRC equity participation and royalty revenues from various licensing arrangements.